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System Monitor Aux

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System Monitor

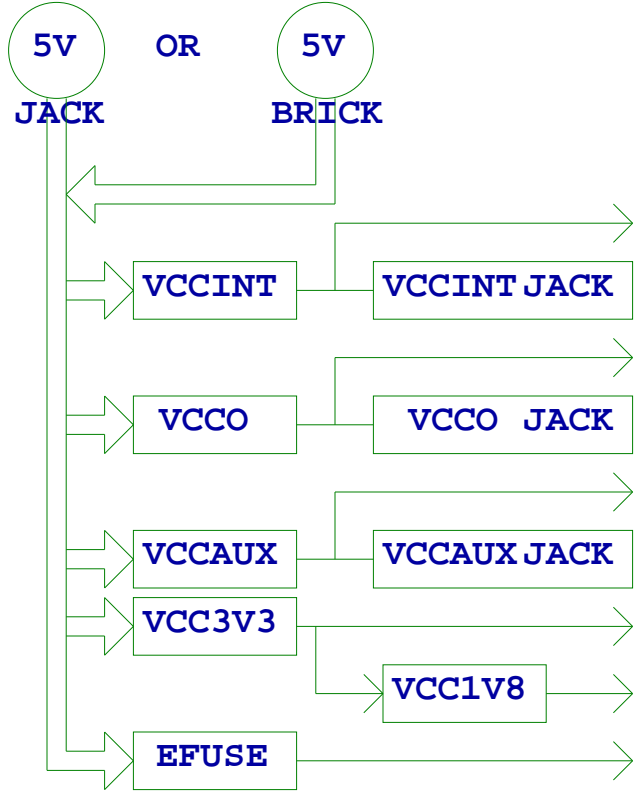
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Upstream

PAGE 2
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Socket Clocks
2X

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Differential
SMA Clocks
2X

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FF676
DUT

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ALL DUT I/O TEST POINTS

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JTAG

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Downstream

Downstream Connector

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Single Ended
Socket Clocks
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Differential
SMA Clocks
2X

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SCH P/N 0381226-01
ART P/N 0531584-01
FAB P/N 1280396-01

Title:
SCHEM, ROHS COMPLIANT, VIRTEX 5 FF676 DAUGHTER, 1280396

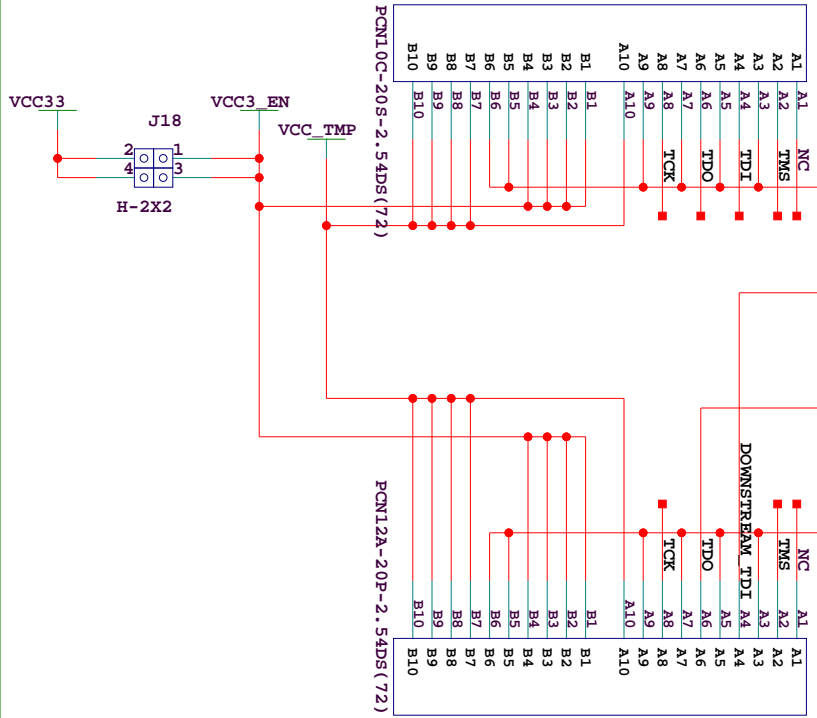
BLOCK DIAGRAM

Date: 1-11-2006_11:25 Ver: D

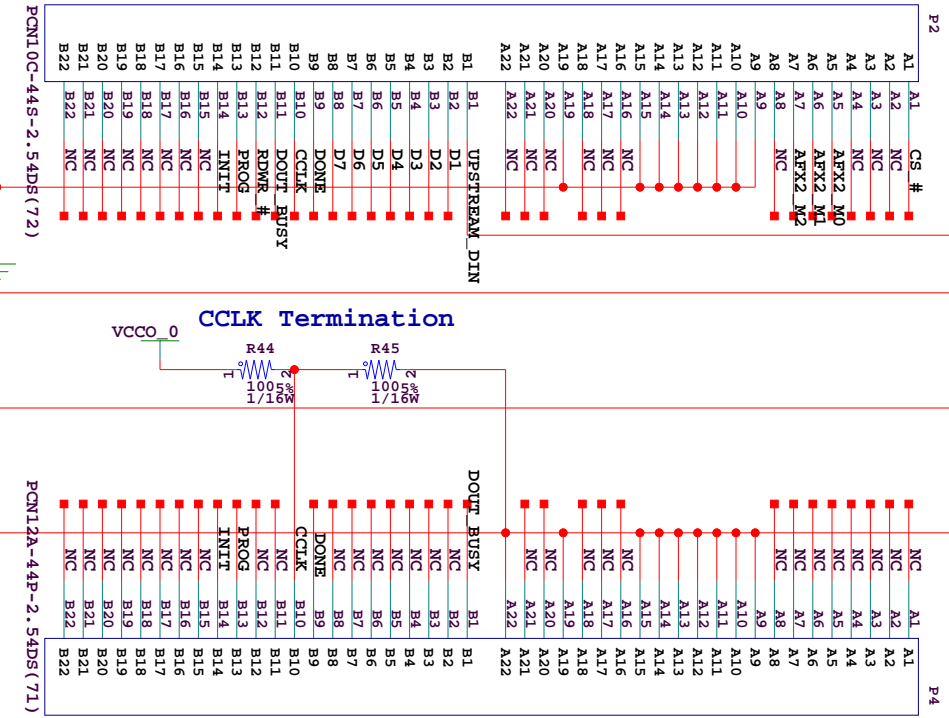
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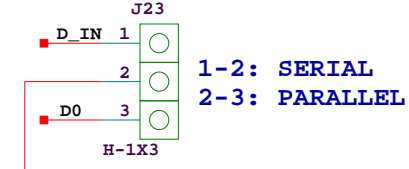
SYSTEM ACE UPSTREAM



UPSTREAM CONNECTORS

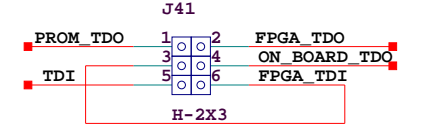


DOWNSTREAM CONFIG



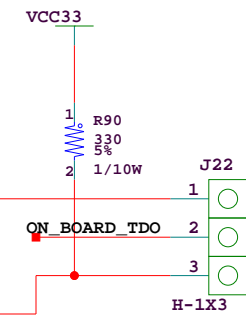
ON BOARD JTAG CHAIN SELECTION

PROM JTAG FPGA JTAG
 1-3: Enable 2-4: Enable
 3-5: Disable 4-6: Disable



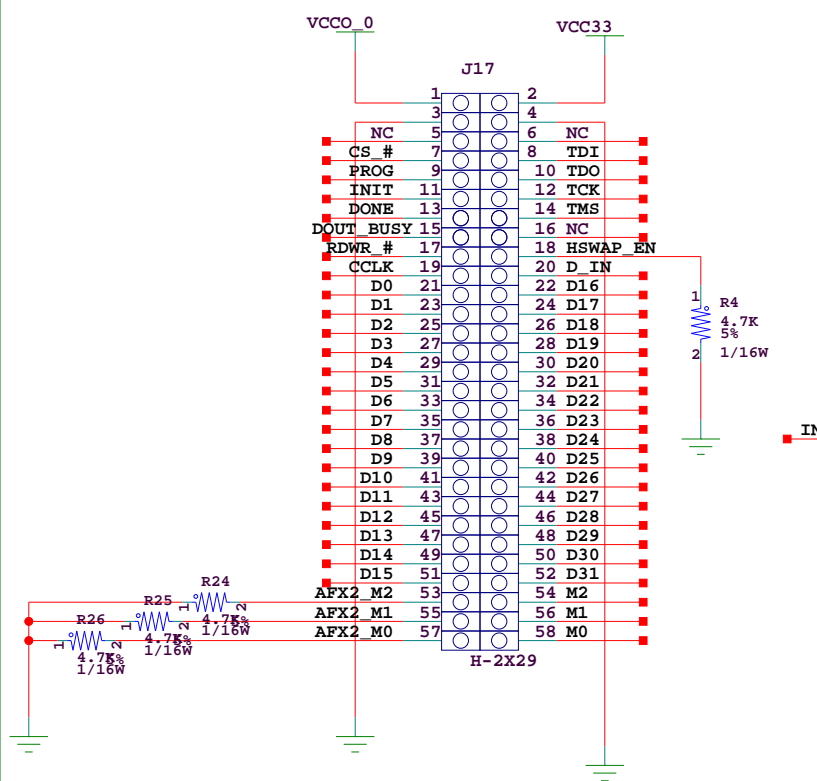
1-2: SERIAL CHAINING TO NEXT BOARD
 2-3: TERMINATION OF LAST BOARD IN THE CHAIN

JTAG JUMPER

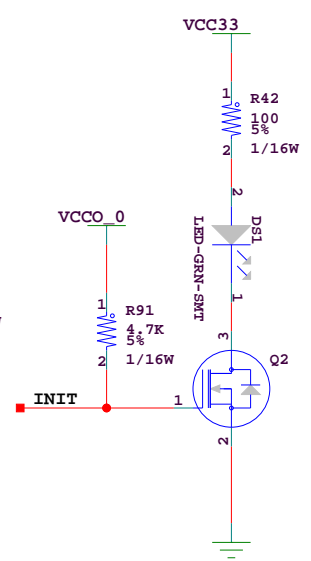


SYSTEM ACE DOWNSTREAM DOWNSTREAM CONNECTORS

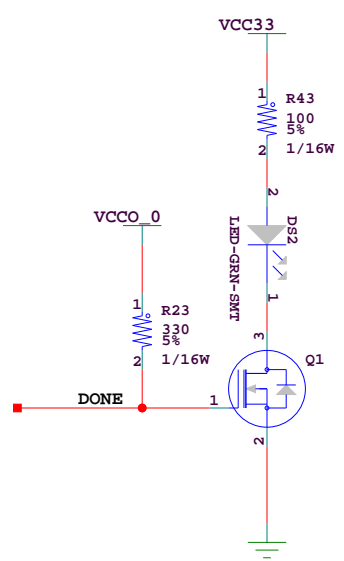
FLYING WIRE CONFIGURATION PORT



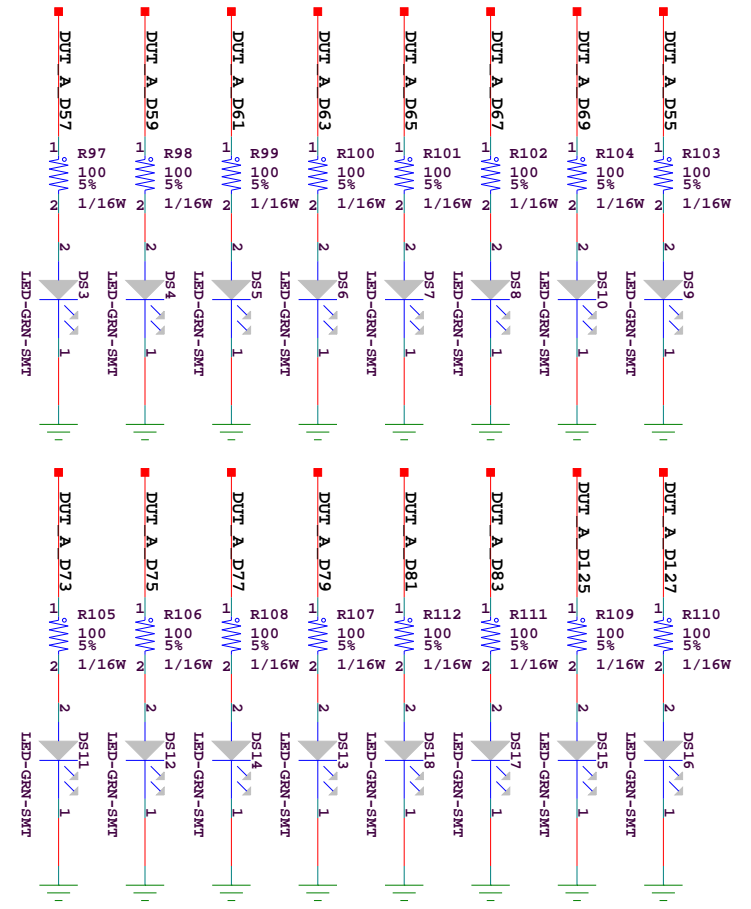
INIT LED



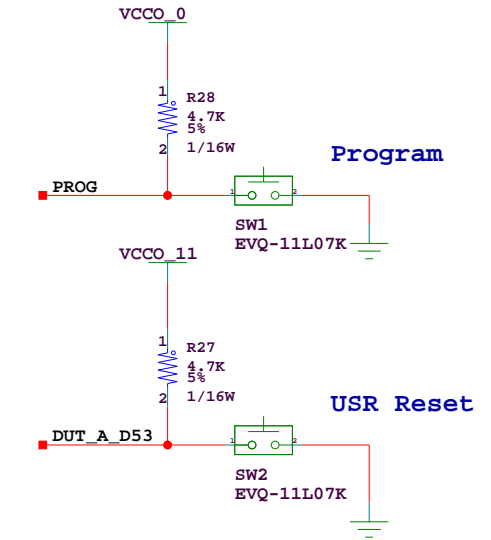
DONE LED



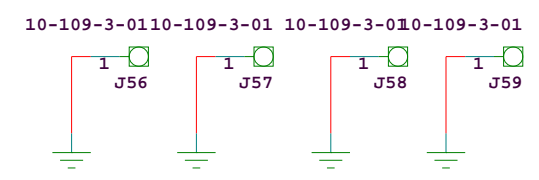
USER LED'S



SWITCHES



TEST POINTS

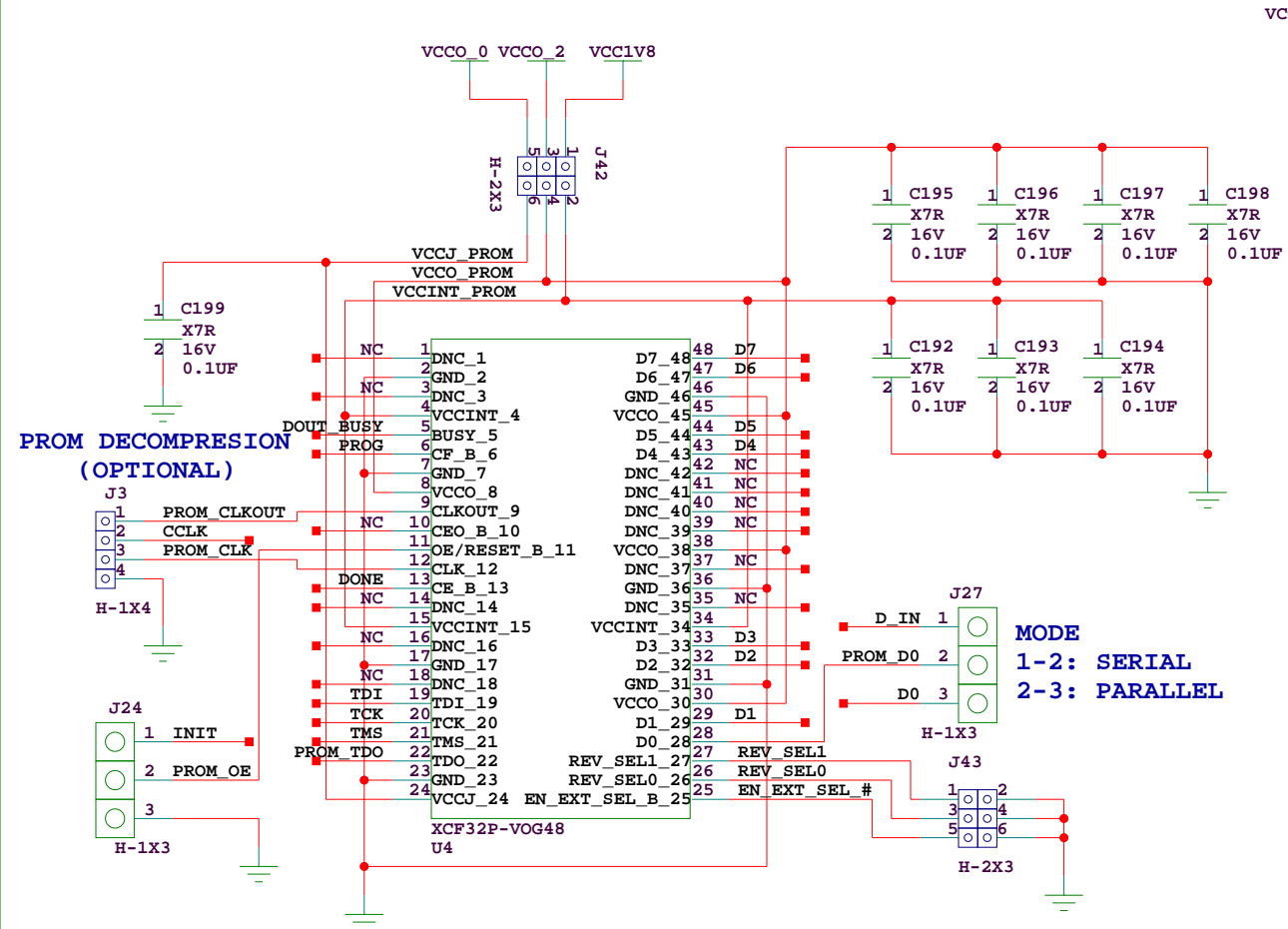


SCH P/N 0381226-01
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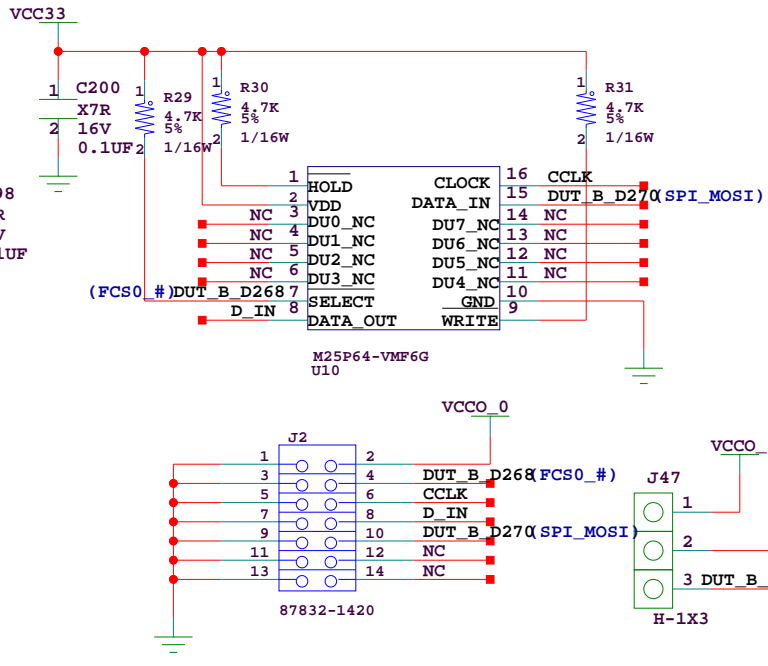
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF676 DAUGHTER, 1280396
 DIN CONN, PORTS, STATUS LEDS, SWITCHES

Date: 5-22-2006_14:17	Ver: D
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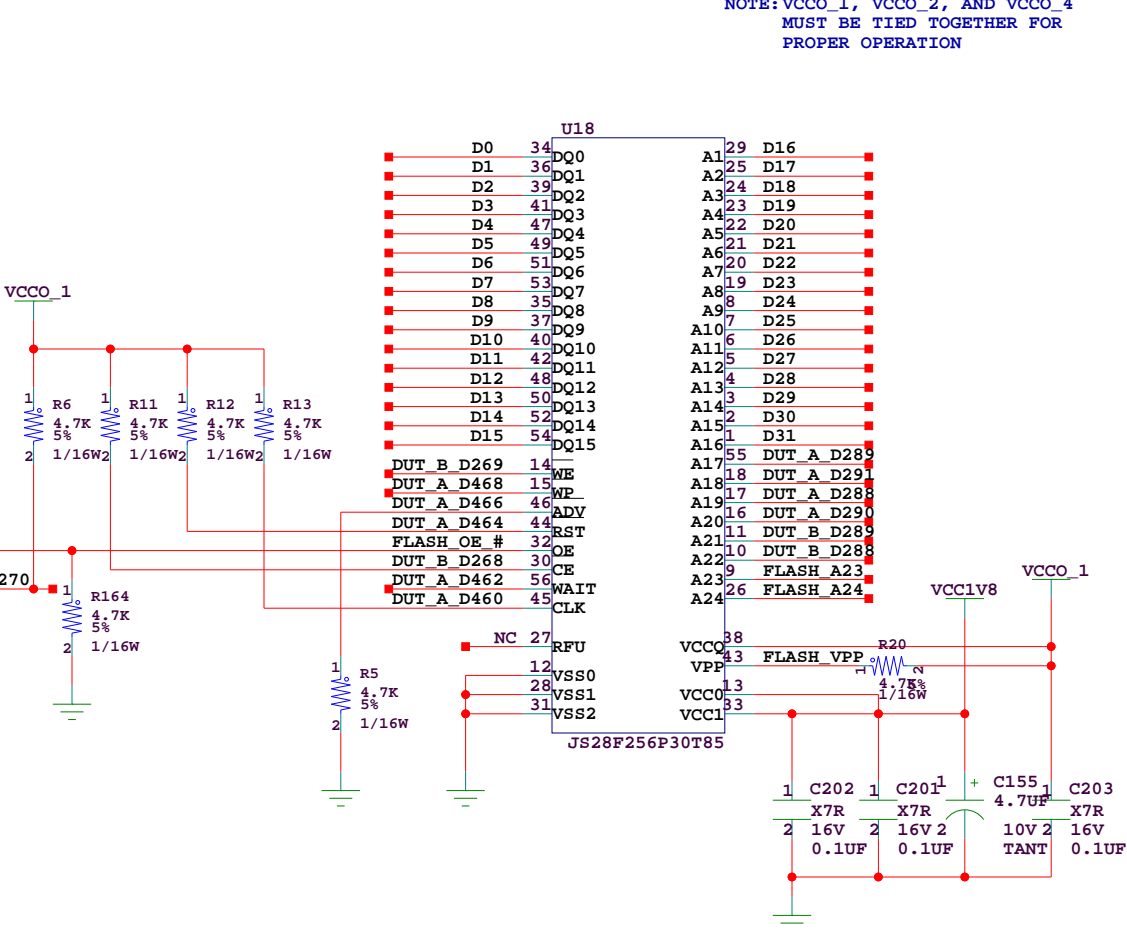
CONFIGURATION PROM



SPI INTERFACE

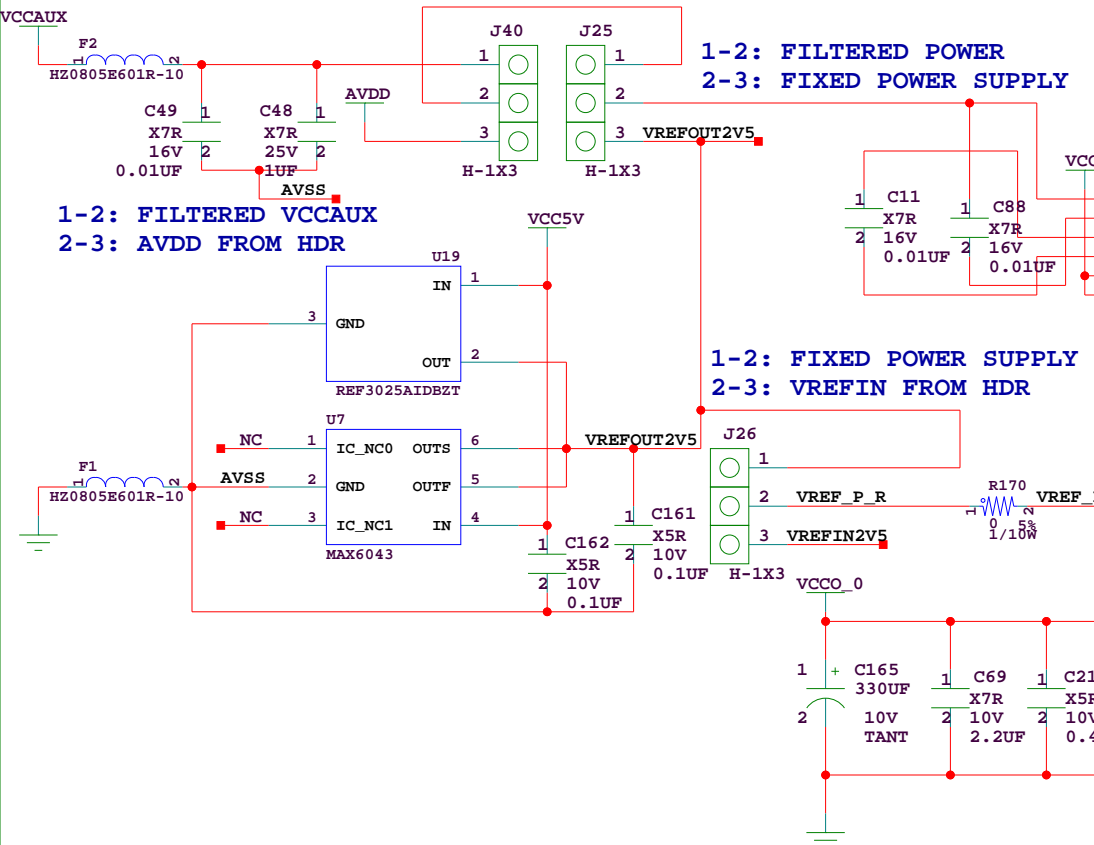


BPI INTERFACE

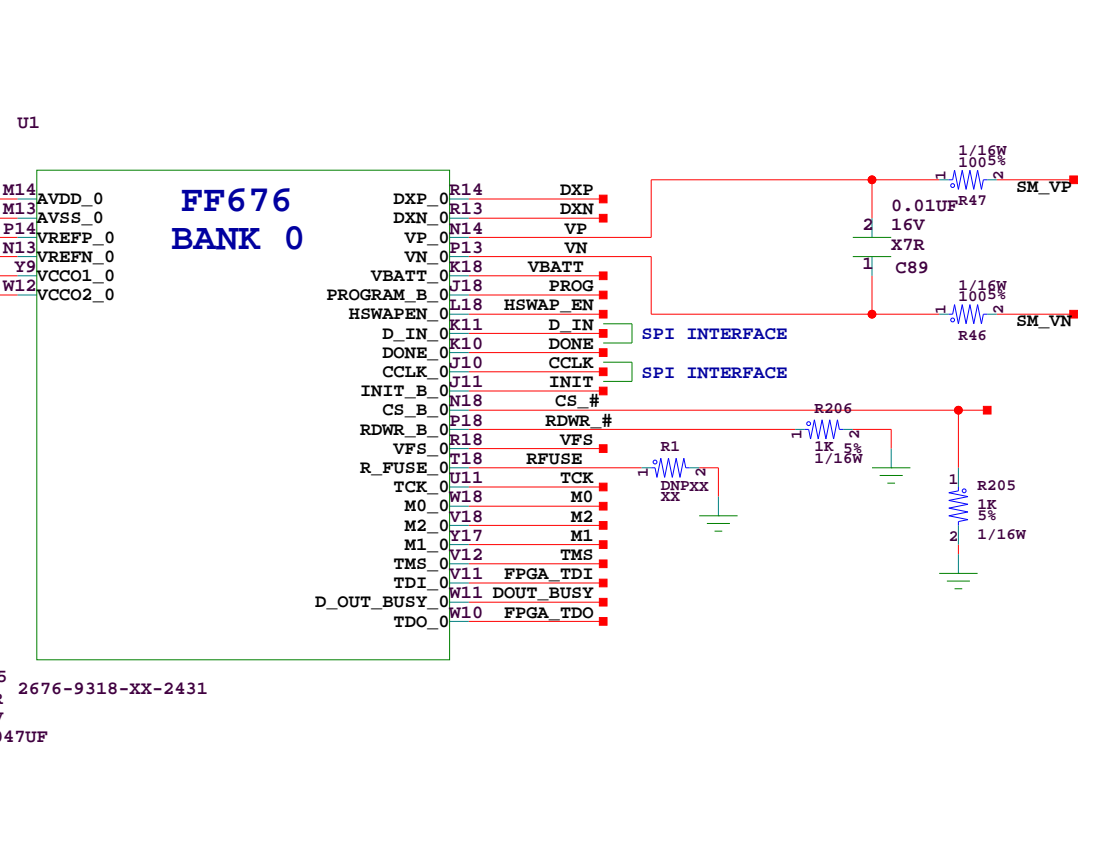


NOTE: VCC0_1, VCC0_2, AND VCC0_4 MUST BE TIED TOGETHER FOR PROPER OPERATION

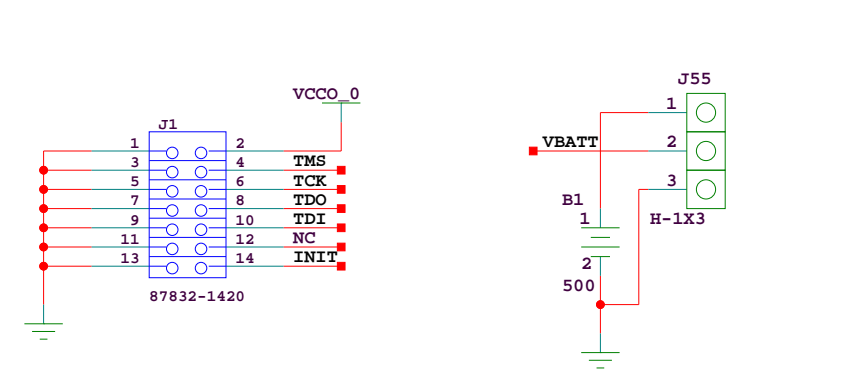
SYSTEM MONITOR SUPPLY



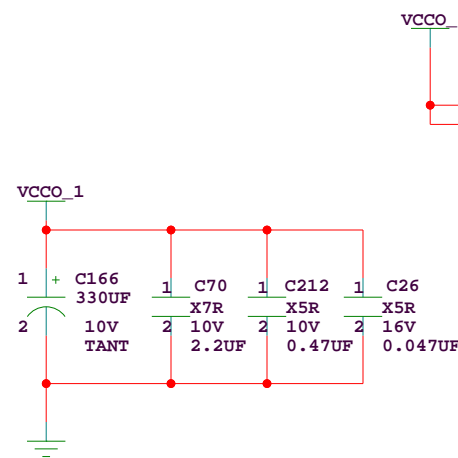
FPGA BANK0 CONFIGURATION



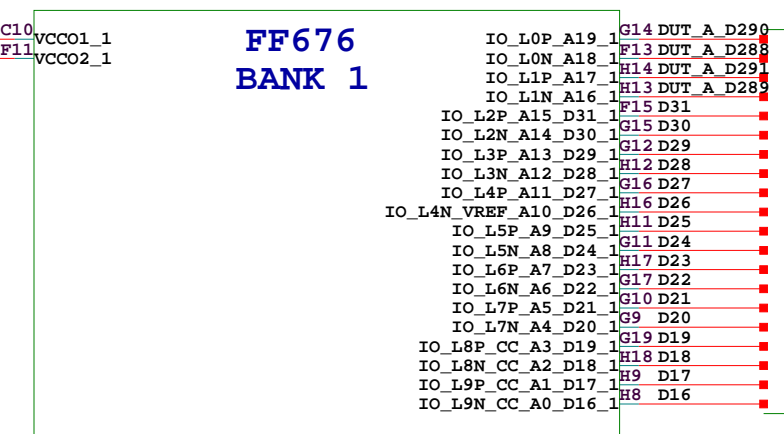
PARALLEL 4 CABLE CONNECTOR VBATT Supply



		SCH P/N	0381226-01
		ART P/N	0531584-01
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Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF676 DAUGHTER, 1280396			
CONFIGURATION			
Date:	5-22-2006_14:17	Ver:	D
Sheet Size:	B	Rev:	01
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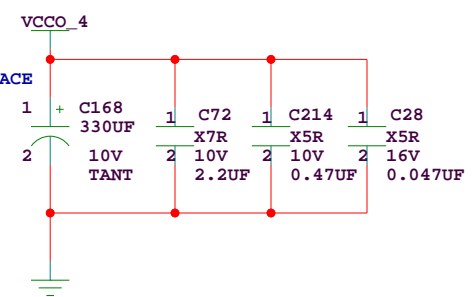


VCCO_1 U1

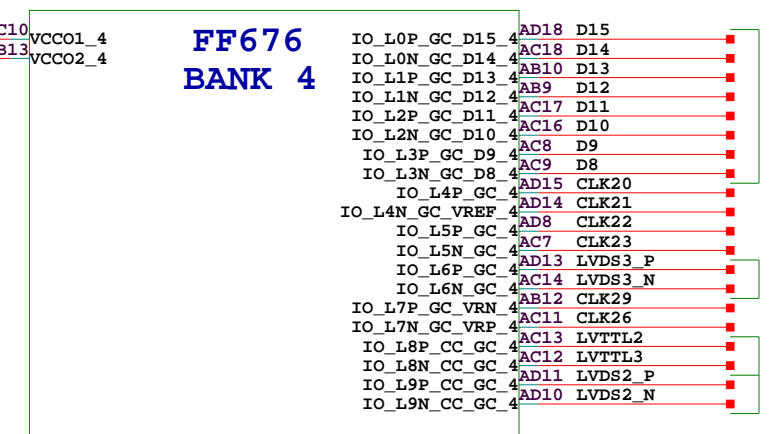


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BPI INTERFACE A1-A20



VCCO_4 U1



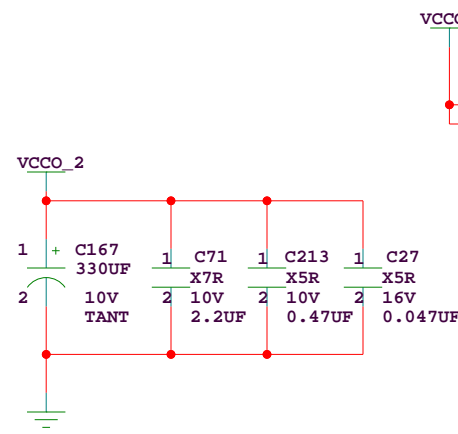
2676-9318-XX-2431

BPI INTERFACE DQ0-DQ7

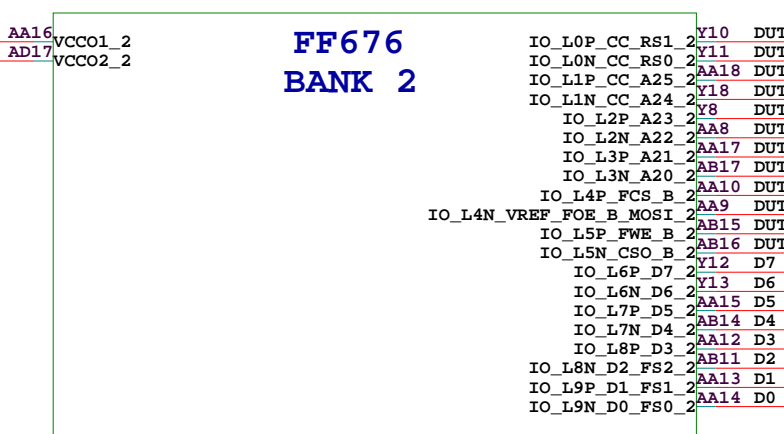
SMA CLOCKS

SOCKET CLOCKS

SMA CLOCKS



VCCO_2 U1

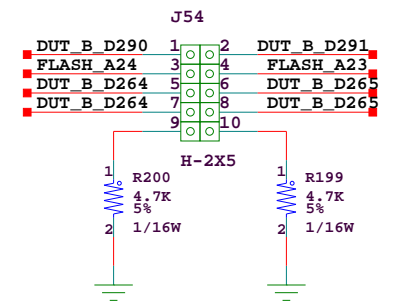


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BPI INTERFACE A21-A22
BPI FLASH_CE_# & SPI SELECT
BPI INTERFACE OE & SPI_MOSI
BPI INTERFACE FLASH_WE_#

BPI INTERFACE DQ0-DQ7

BPI REVISION SELECT PINS



- 1-3: Selects ADDR23 from FPGA to FLASH ADDR24
- 3-5: Selects RS1 from FPGA to FLASH ADDR24
- 7-9: Pulldown for RS applications
- 2-4: Selects ADDR22 from FPGA to FLASH ADDR23
- 4-6: Selects RS0 from FPGA to FLASH ADDR23
- 8-10: Pulldown for RS applications

SCH P/N 0381226-01
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FAB P/N 1280396-01

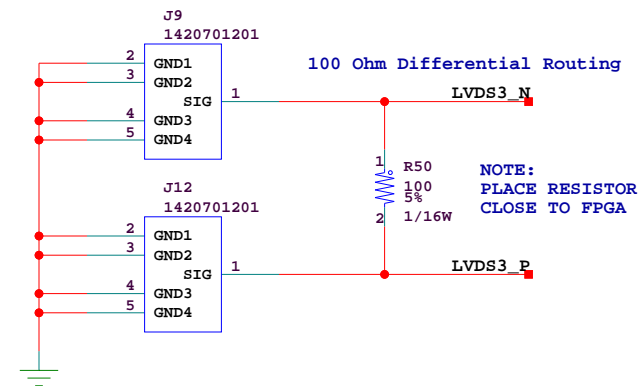
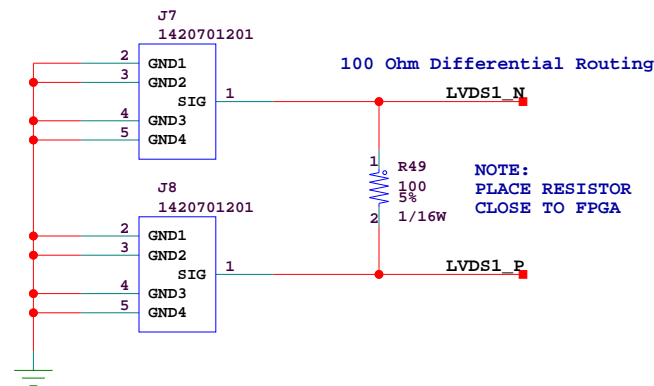
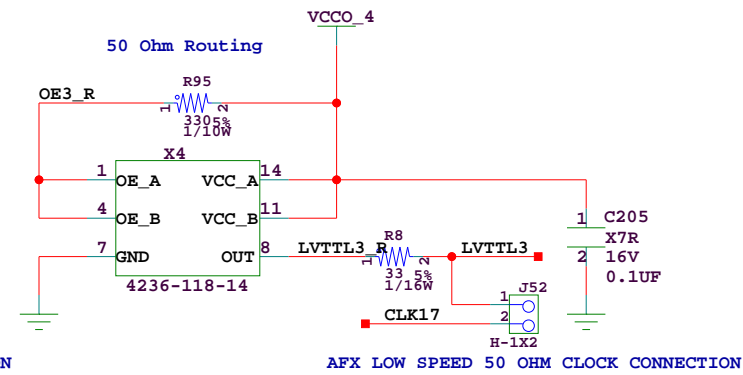
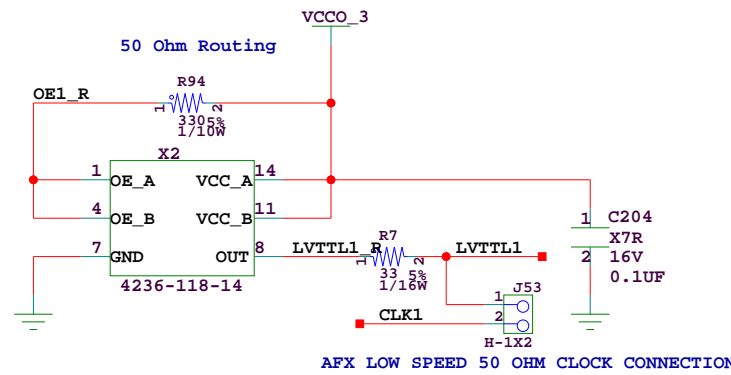
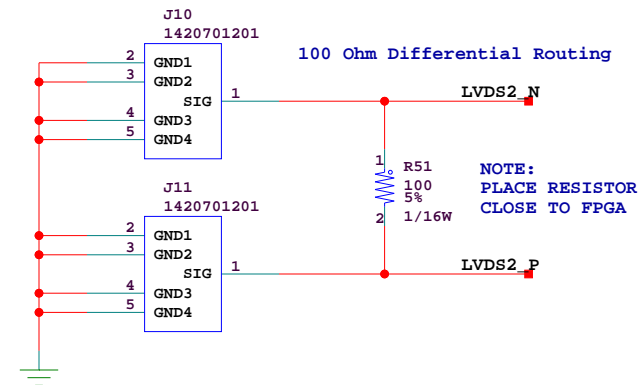
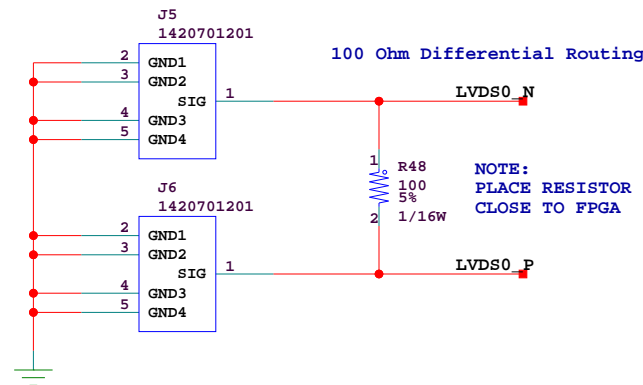
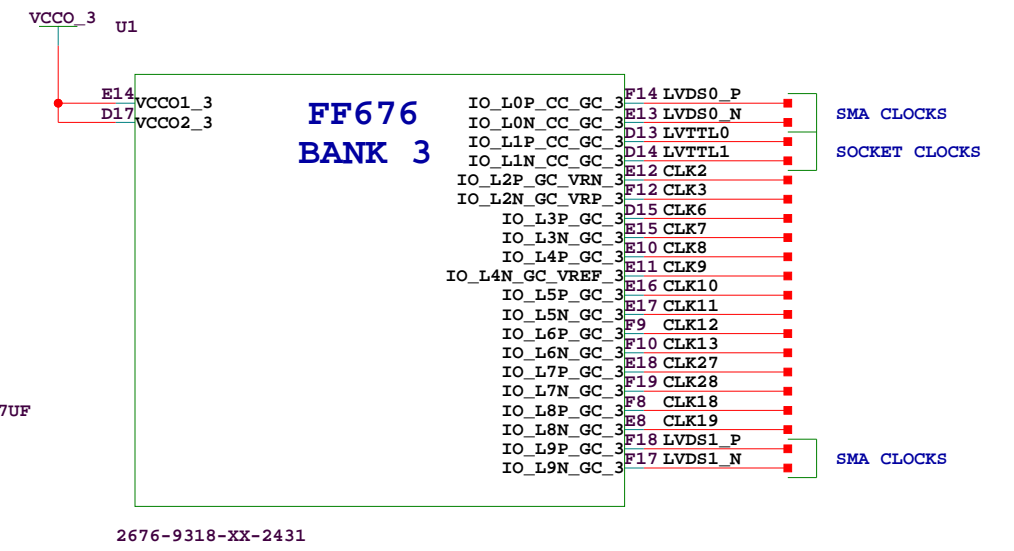
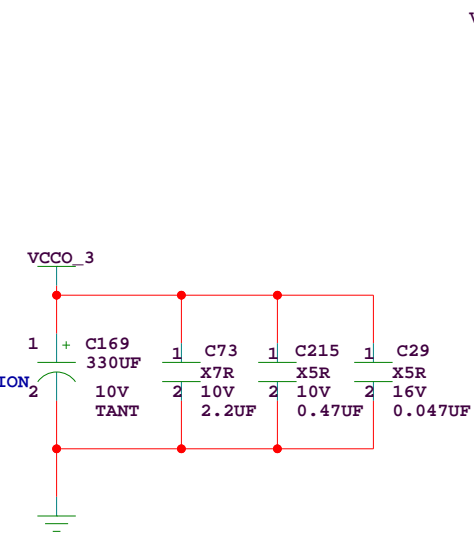
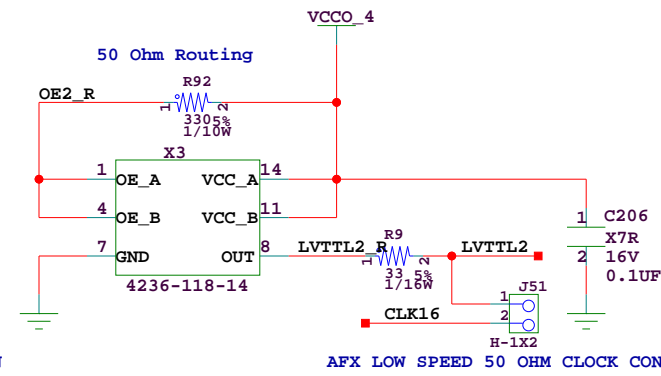
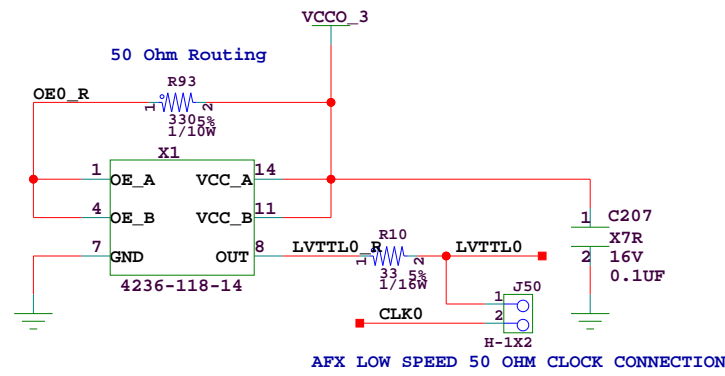
Title:
SCHEM, ROHS COMPLIANT, VIRTEX 5 FF676 DAUGHTER, 1280396

CONFIGURATION

Date: 5-22-2006_14:17 Ver: D
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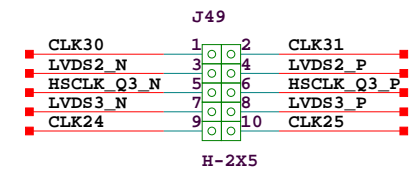
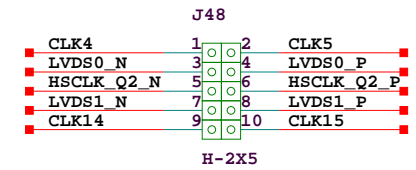
UPPER CLOCKS

BOTTOM CLOCKS



AFX CLOCK CONFIGURATION

1-3, 2-4: LOW SPEED 50 OHM CLOCK CONNECTION
 3-5, 4-6: HIGH SPEED 100 OHM DIFFERENTIAL CLOCK CONNECTION TO DIFFERENTIAL PAIR
 5-7, 6-8: HIGH SPEED 100 OHM DIFFERENTIAL CLOCK CONNECTION TO DIFFERENTIAL PAIR
 7-9, 8-10: LOW SPEED 50 OHM CLOCK CONNECTION



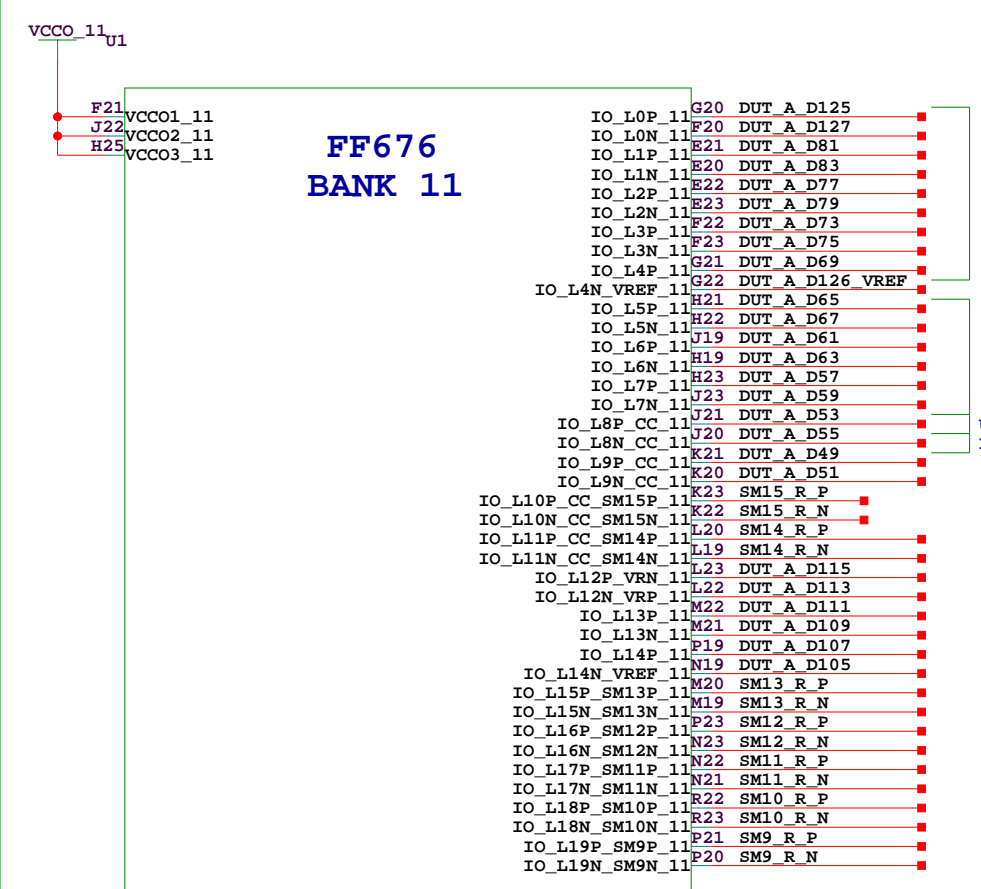
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SCH P/N 0381226-01
 ART P/N 0531584-01
 FAB P/N 1280396-01

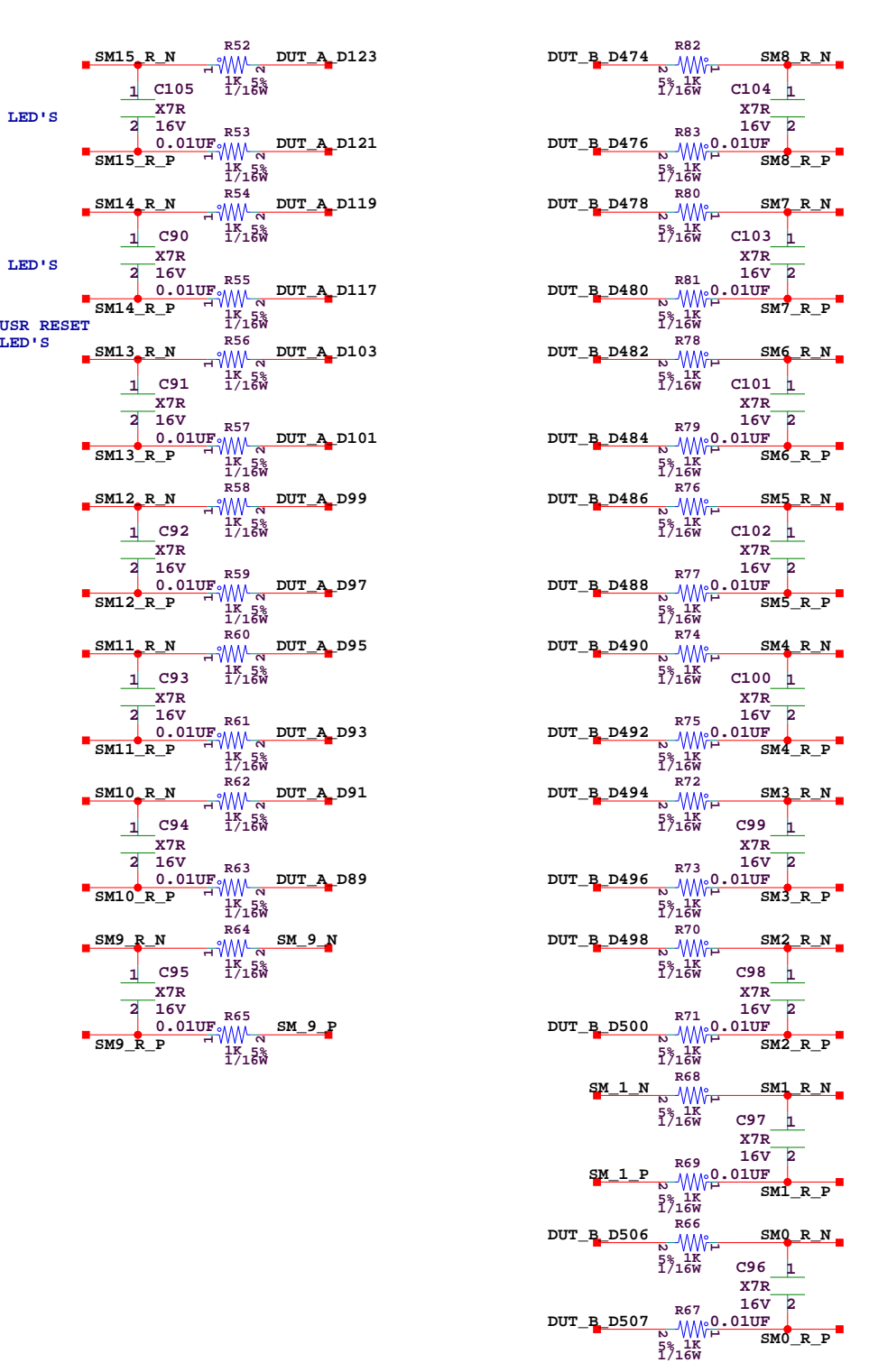
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF676 DAUGHTER, 1280396
 SOCKET CLOCKS, SMA DIFF CLOCKS

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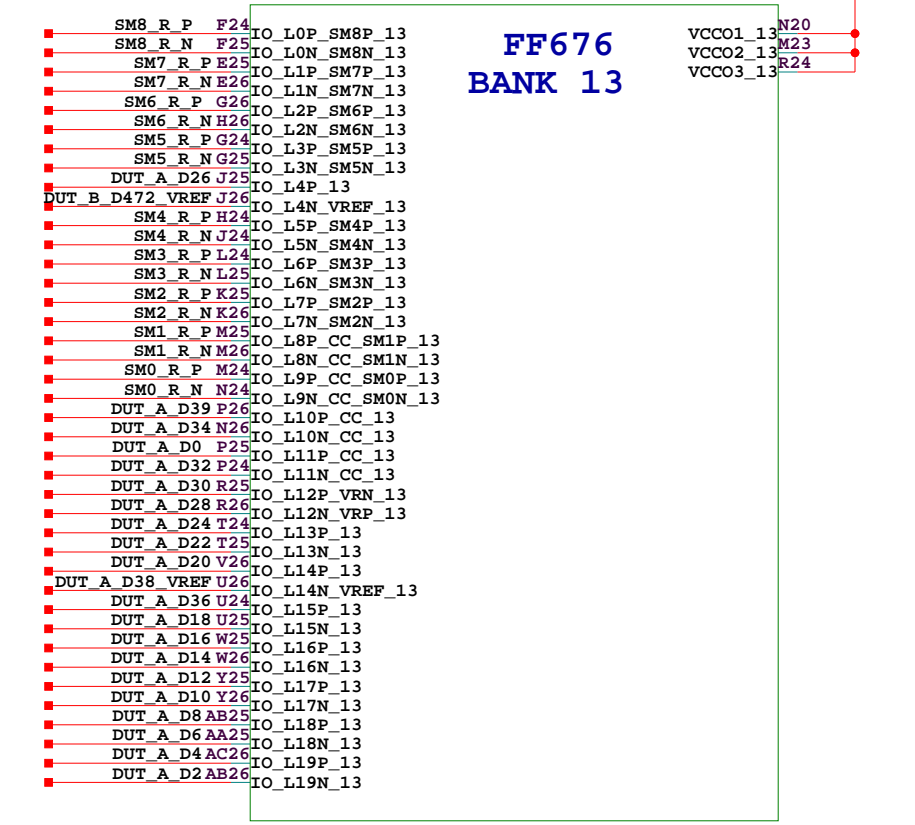
FF676 BANK 11



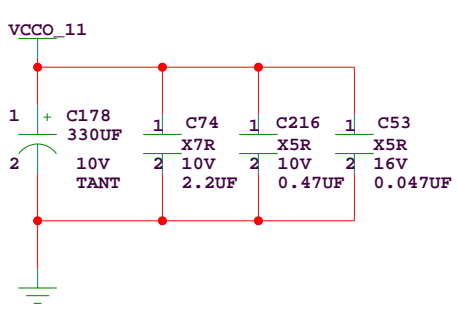
SYSTEM MONITOR FILTERS



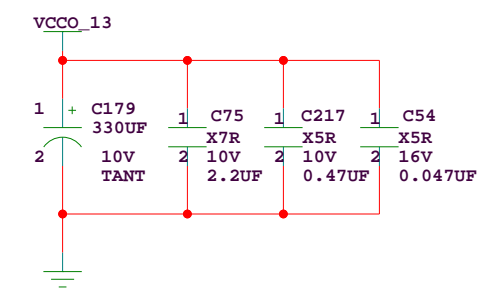
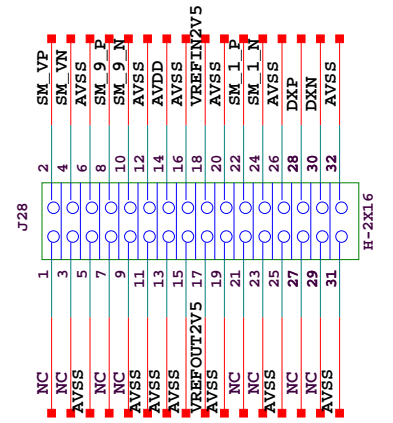
FF676 BANK 13



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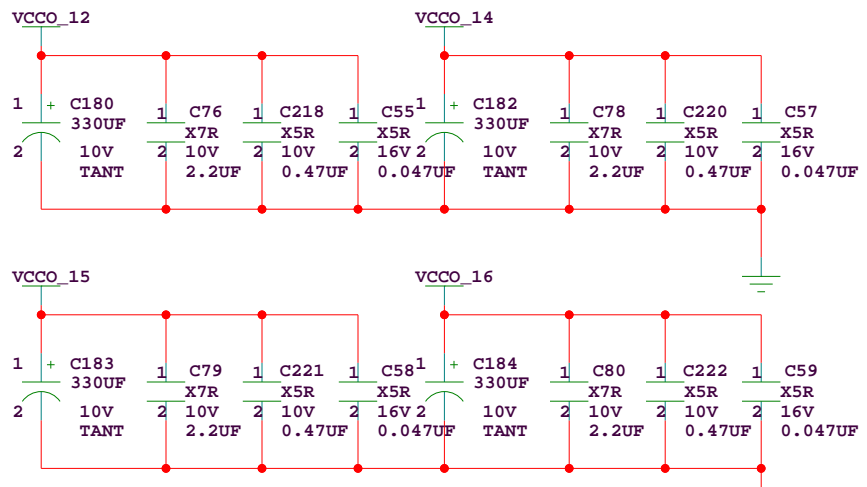
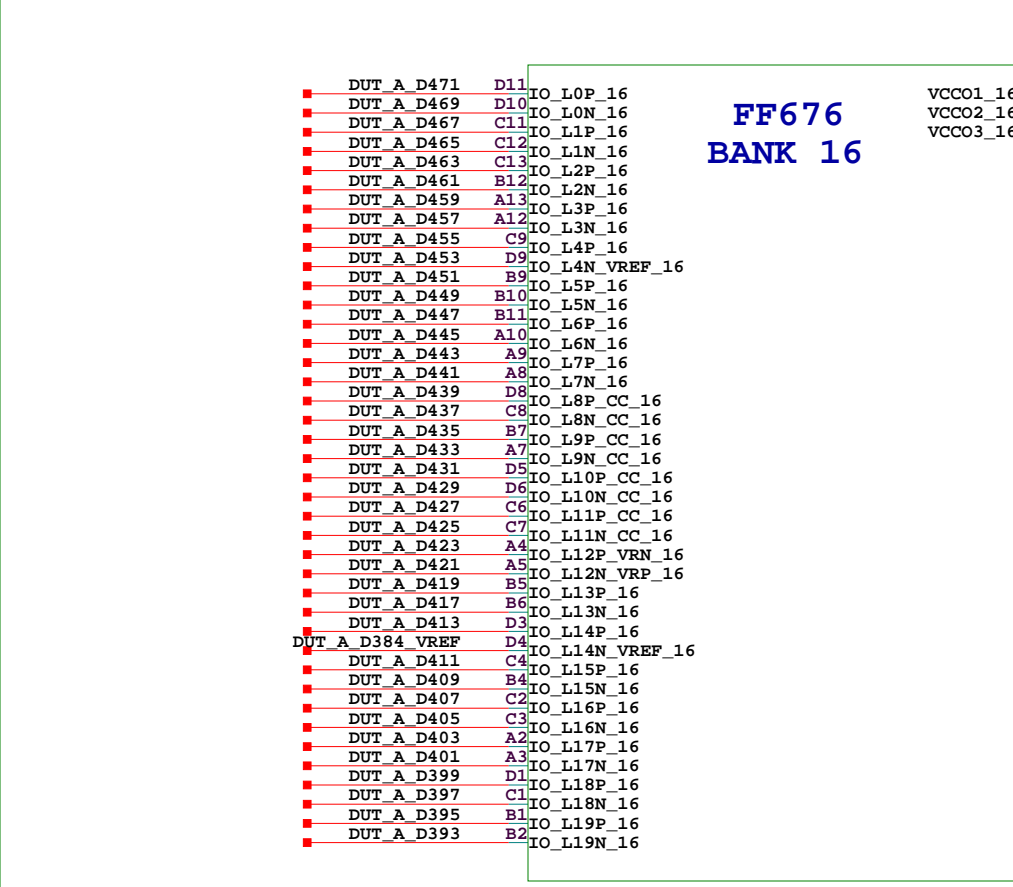
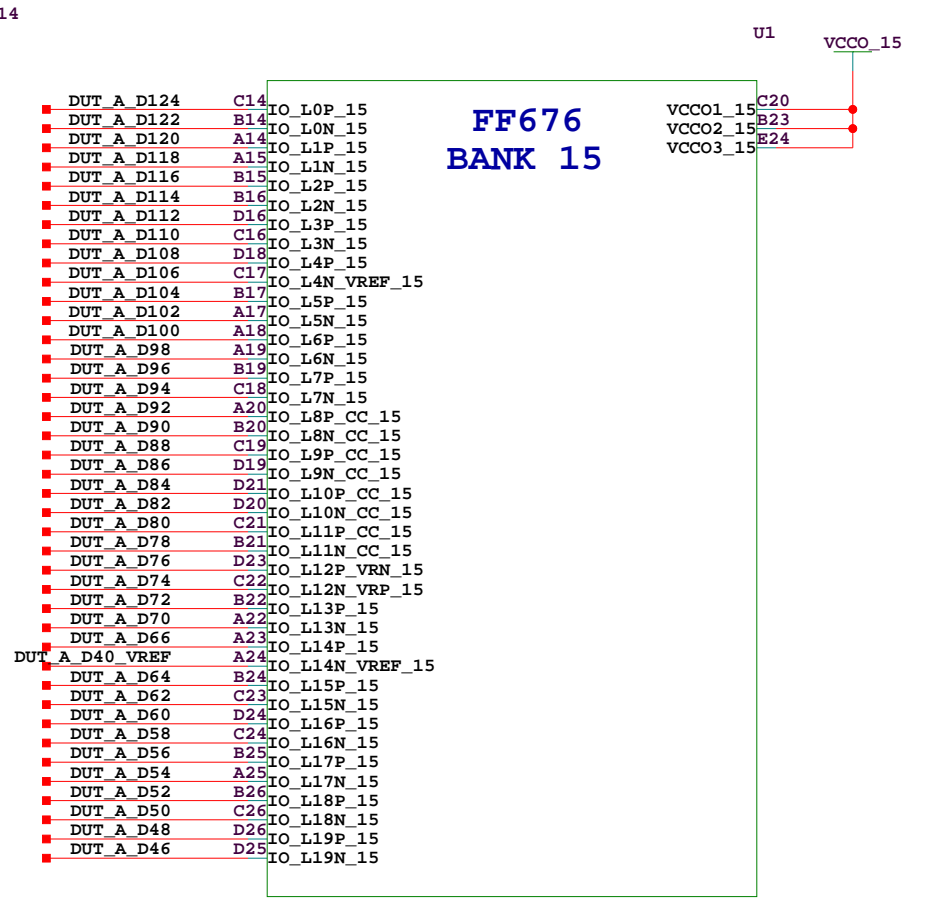
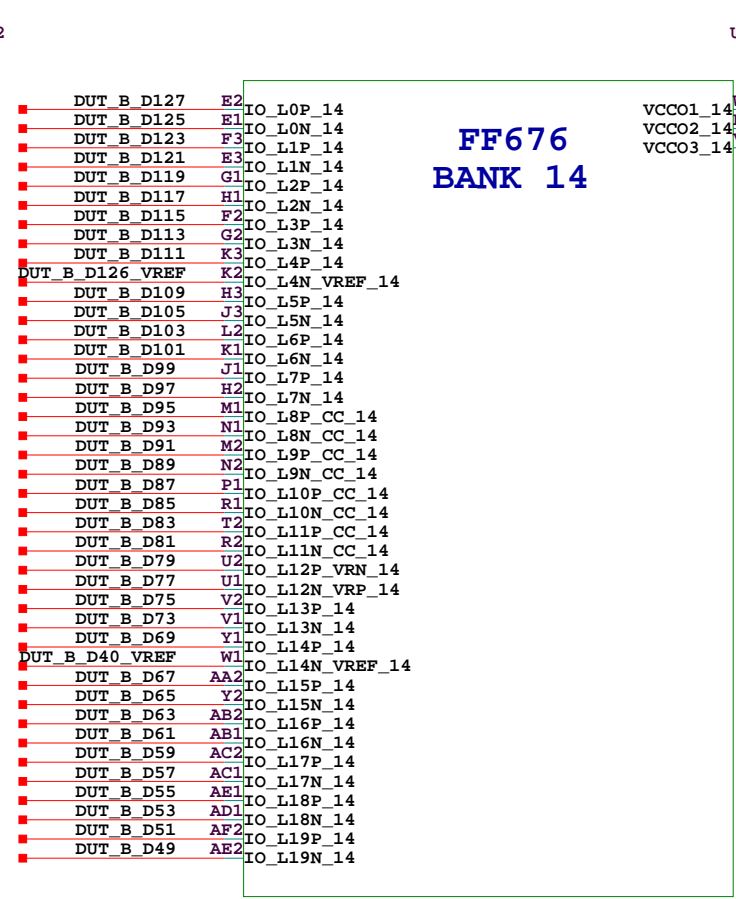
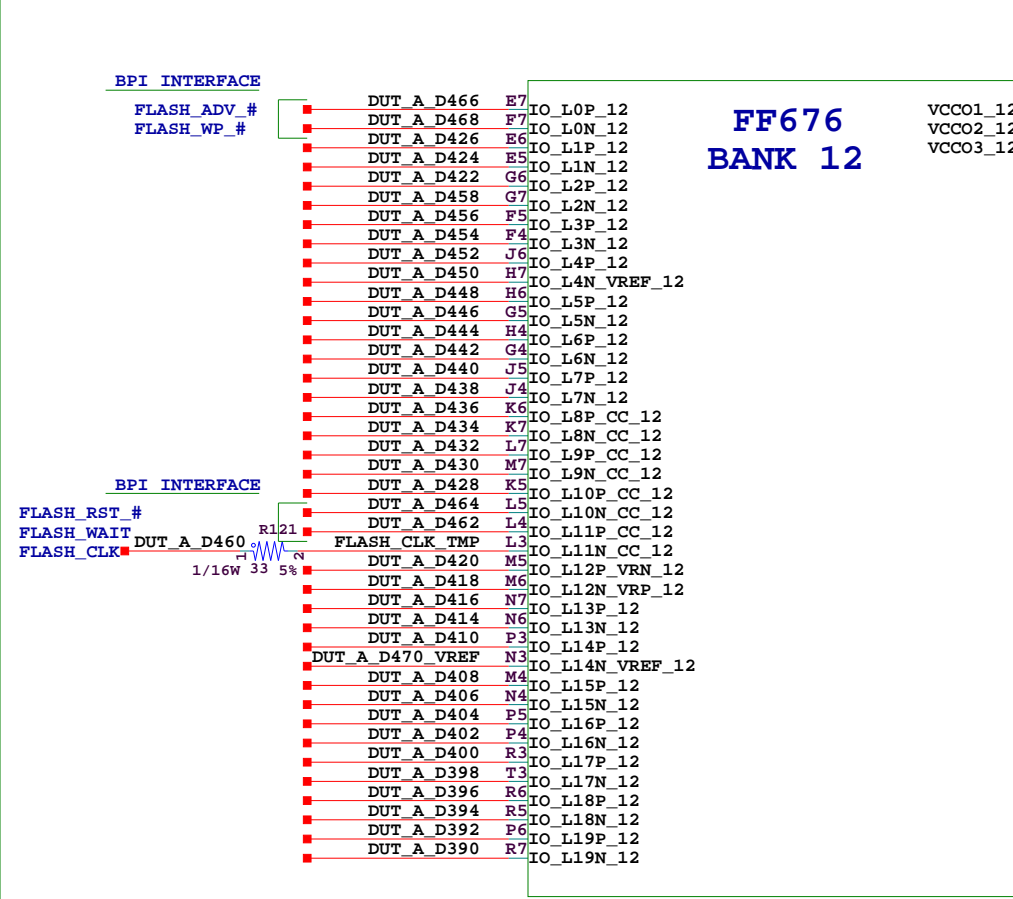


SYSTEM MONITOR MALE CONNECTOR



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		SCH P/N	0381226-01
		ART P/N	0531584-01
		FAB P/N	1280396-01
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF676 DAUGHTER, 1280396			
SYSTEM MONITOR			
Date:	5-22-2006_14:17	Ver:	D
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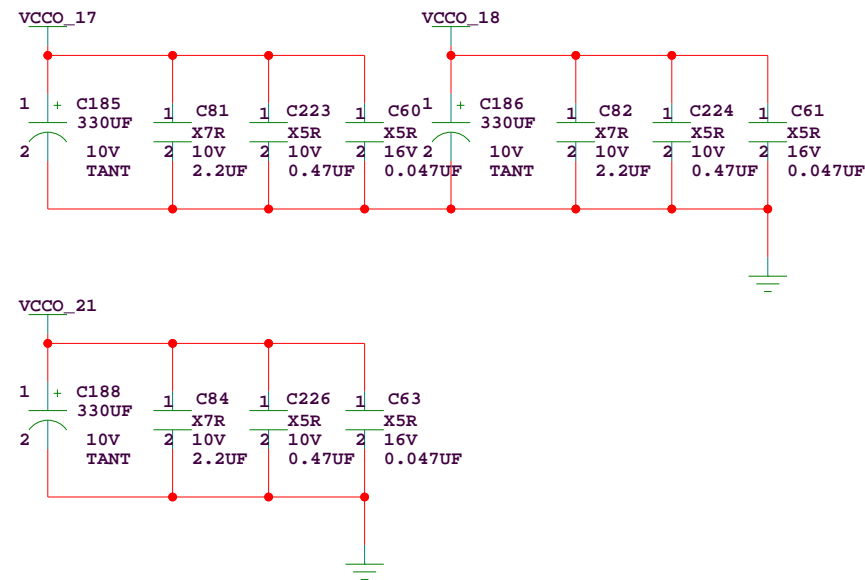
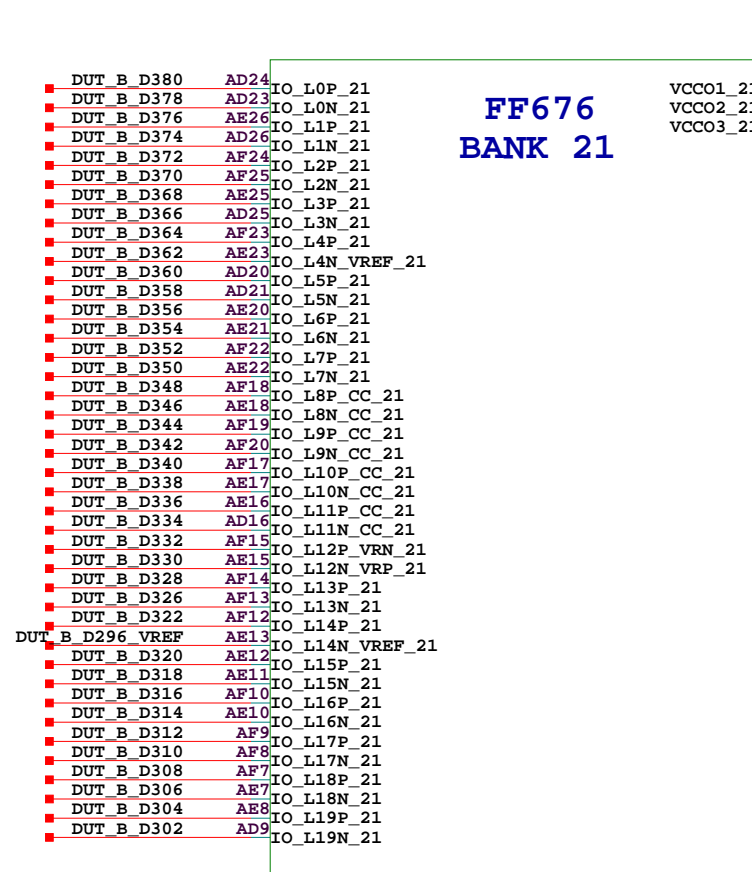
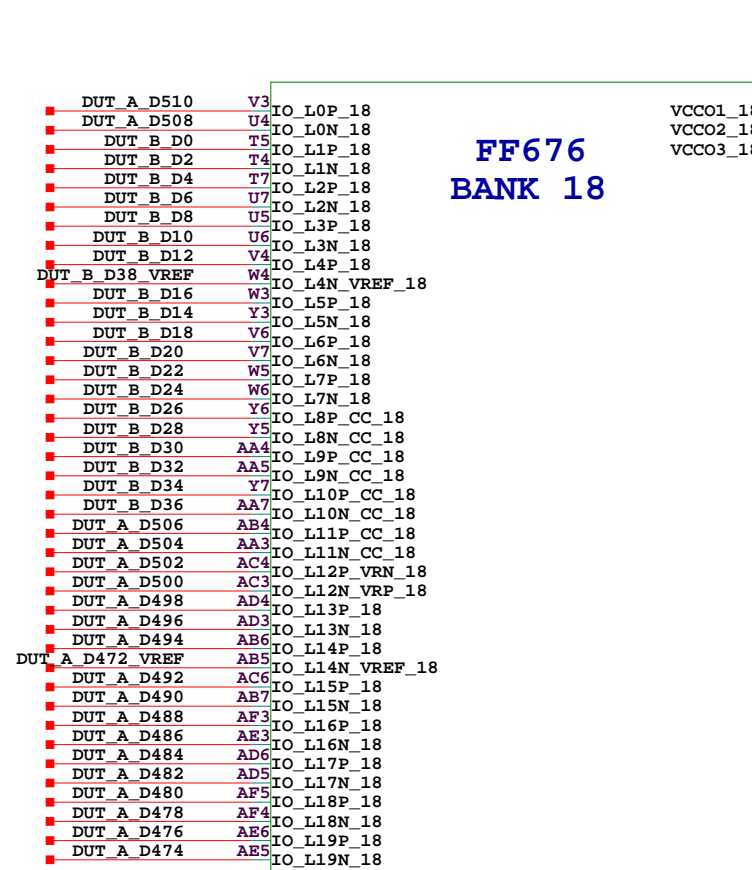
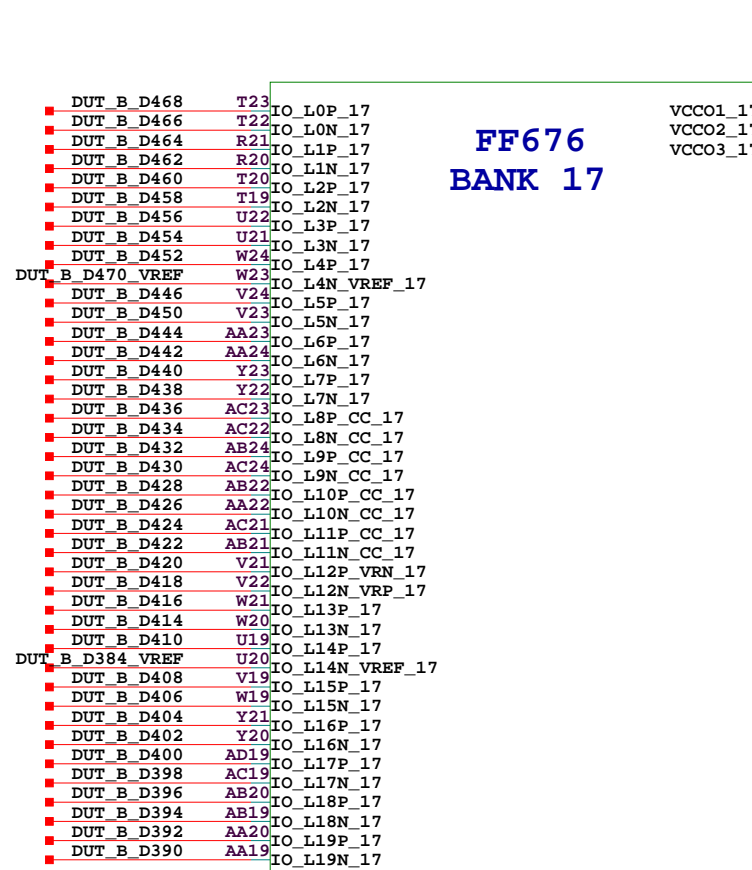
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SCH P/N 0381226-01
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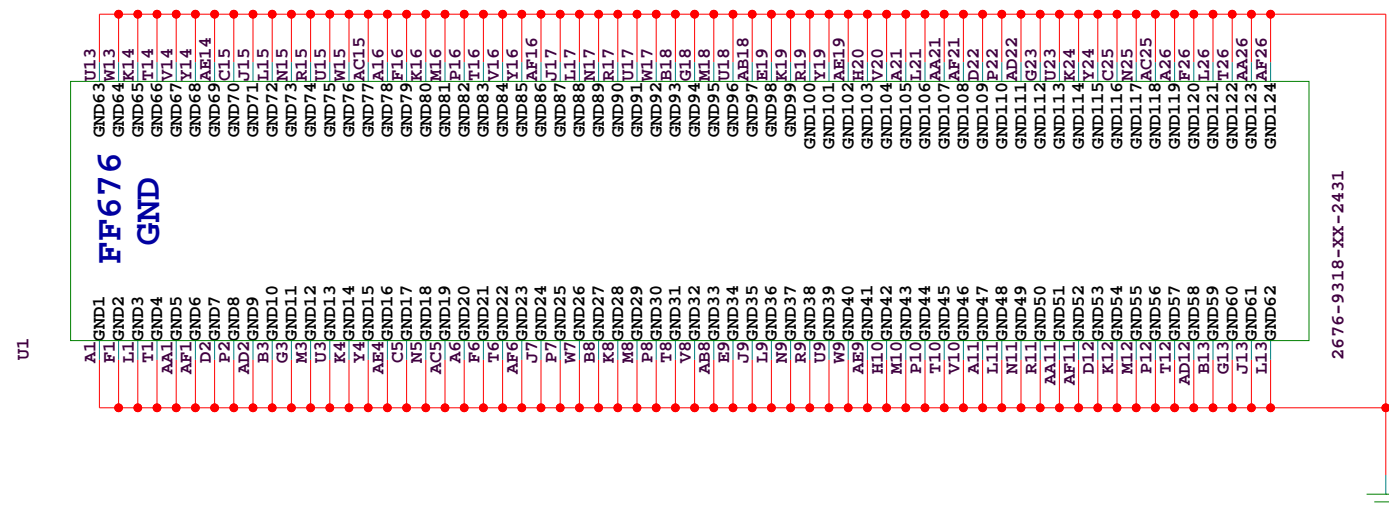
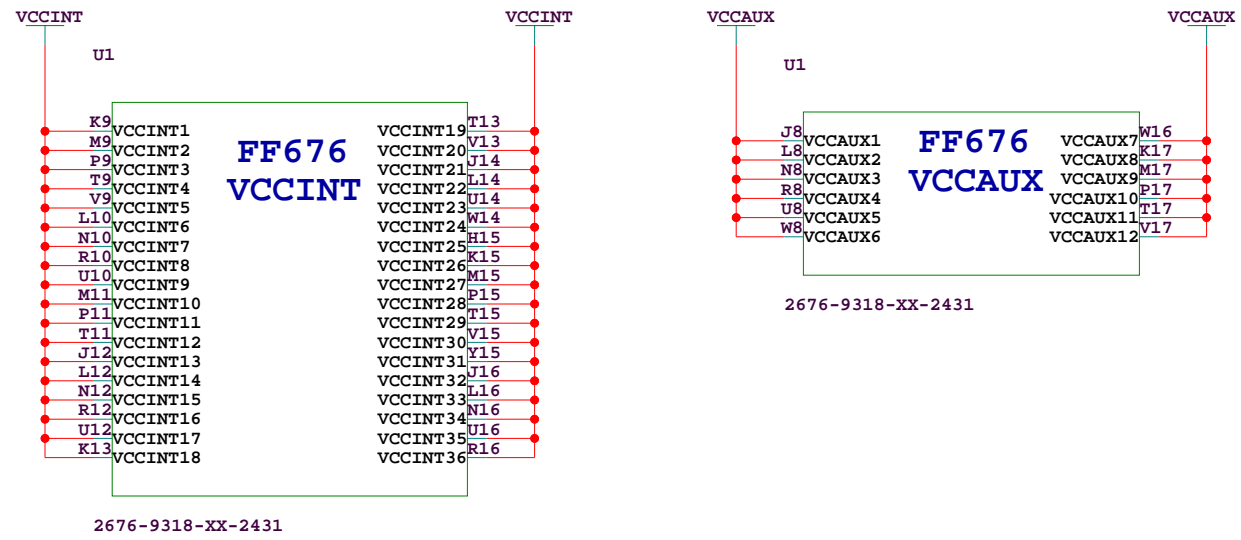
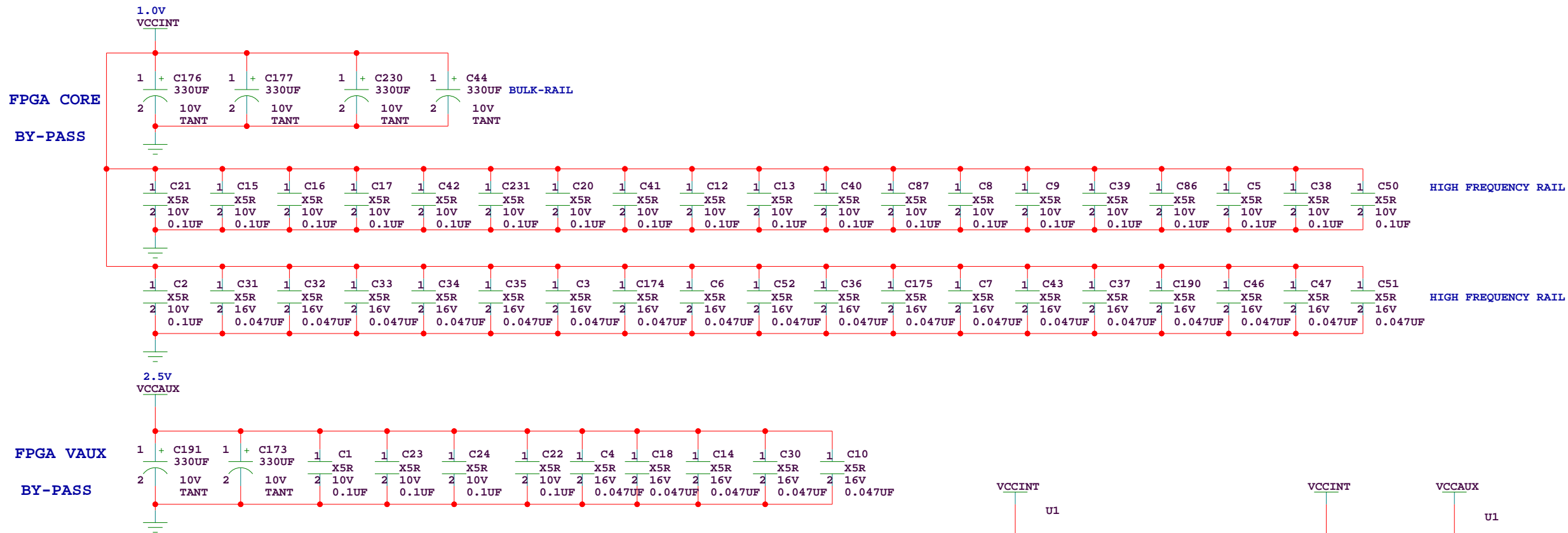
Title:
 SCHEM, ROHS COMPLIANT, VIRTEX 5 FF676 DAUGHTER, 1280396


DUT INTERFACE

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		SCH P/N	0381226-01
		ART P/N	0531584-01
		FAB P/N	1280396-01
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF676 DAUGHTER, 1280396			
DUT INTERFACE			
Date: 5-22-2006_14:17		Ver: D	
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		SCH P/N	0381226-01
		ART P/N	0531584-01
		FAB P/N	1280396-01
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF676 DAUGHTER, 1280396 FPGA DECOUPLING CAPACITORS			
Date: 5-22-2006_14:17		Ver: D	
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DXP R14 DXP_0
 DXN R13 DXN_0
 NC N14 VP_0
 NC P13 VN_0
 VBATT K18 VBATT_0
 PROG J18 PROGRAM_B_0
 HSWAP_EN L18 HSWAPEN_0
 D_IN K11 D_IN_0
 DONE K10 DONE_0
 CCLK J10 CCLK_0
 INIT J11 INIT_B_0
 CS # N18 CS_B_0
 RDWR # P18 RDWR_B_0
 VFS R18 VFS_0
 RFUSE T18 R_FUSE_0
 TCK U11 TCK_0
 M0 W18 MO_0
 M2 V18 M2_0
 M1 Y17 M1_0
 TMS V12 TMS_0
 FPGA_TDI V11 TDI_0
 DOUT_BUSY W11 D_OUT_BUSY_0
 FPGA_TDO W10 TDO_0

**FF676
BANK 0**

U1A
 VCCO_0
 AVDD M14 NC
 AVSS M13 NC
 VREFP_0 P14 NC
 VREFN_0 N13 NC
 VCCO1_0 Y9
 VCCO2_0 W12

DUT A D290 G14 IO L0P_A19_1
 DUT A D288 F13 IO L0N_A18_1
 DUT A D291 H14 IO L1P_A17_1
 DUT A D289 H13 IO L1N_A16_1
 D31 F15 IO L2P_A15_D31_1
 D30 G15 IO L2N_A14_D30_1
 D29 G12 IO L3P_A13_D29_1
 D28 H12 IO L3N_A12_D28_1
 D27 G16 IO L4P_A11_D27_1
 D26 H16 IO L4N_VREF_A10_D26_1
 D25 H11 IO L5P_A9_D25_1
 D24 G11 IO L5N_A8_D24_1
 D23 H17 IO L6P_A7_D23_1
 D22 G17 IO L6N_A6_D22_1
 D21 G10 IO L7P_A5_D21_1
 D20 G9 IO L7N_A4_D20_1
 D19 G19 IO L8P_CC_A3_D19_1
 D18 H18 IO L8N_CC_A2_D18_1
 D17 H9 IO L9P_CC_A1_D17_1
 D16 H8 IO L9N_CC_A0_D16_1

**FF676
BANK 1**

U1A
 VCCO_1
 VCCO1_1 C10
 VCCO2_1 F11

DUT B D264 Y10 IO L0P_CC_RS1_2
 DUT B D265 Y11 IO L0N_CC_RS0_2
 DUT B D266 AA18 IO L1P_CC_A25_2
 DUT B D267 Y18 IO L1N_CC_A24_2
 DUT B D290 Y8 IO L2P_A23_2
 DUT B D291 AA8 IO L2N_A22_2
 DUT B D288 AA17 IO L3P_A21_2
 DUT B D289 AB17 IO L3N_A20_2
 DUT B D268 AA10 IO L4P_FCS_B_2
 DUT B D270 AA9 IO L4N_VREF_FOE_B_MOSI_2
 DUT B D269 AB15 IO L5P_FWE_B_2
 DUT B D271 AB16 IO L5N_CS0_B_2
 D7 Y12 IO L6P_D7_2
 D6 Y13 IO L6N_D6_2
 D5 AA15 IO L7P_D5_2
 D4 AB14 IO L7N_D4_2
 D3 AA12 IO L8P_D3_2
 D2 AB11 IO L8N_D2_FS2_2
 D1 AA13 IO L9P_D1_FS1_2
 D0 AA14 IO L9N_D0_FS0_2

**FF676
BANK 2**

U1A
 VCCO_2
 VCCO1_2 AA16
 VCCO2_2 AD17

LVDS0_P F14 IO L0P_CC_GC_3
 LVDS0_N E13 IO L0N_CC_GC_3
 LVTTLO D13 IO L1P_CC_GC_3
 LVTTL1 D14 IO L1N_CC_GC_3
 CLK2 E12 IO L2P_GC_VRN_3
 CLK3 F12 IO L2N_GC_VRP_3
 CLK6 D15 IO L3P_GC_3
 CLK7 E15 IO L3N_GC_3
 CLK8 E10 IO L4P_GC_3
 CLK9 E11 IO L4N_GC_VREF_3
 CLK10 E16 IO L5P_GC_3
 CLK11 E17 IO L5N_GC_3
 CLK12 F9 IO L6P_GC_3
 CLK13 F10 IO L6N_GC_3
 CLK27 E18 IO L7P_GC_3
 CLK28 F19 IO L7N_GC_3
 CLK18 F8 IO L8P_GC_3
 CLK19 E8 IO L8N_GC_3
 LVDS1_P F18 IO L9P_GC_3
 LVDS1_N F17 IO L9N_GC_3

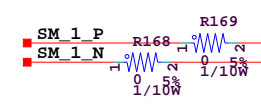
**FF676
BANK 3**

U1A
 VCCO_3
 HDR_FG676
 VCCO1_3 E14
 VCCO2_3 D17

D15 AD18 IO L0P_GC_D15_4
 D14 AC18 IO L0N_GC_D14_4
 D13 AB10 IO L1P_GC_D13_4
 D12 AB9 IO L1N_GC_D12_4
 D11 AC17 IO L2P_GC_D11_4
 D10 AC16 IO L2N_GC_D10_4
 D9 AC8 IO L3P_GC_D9_4
 D8 AC9 IO L3N_GC_D8_4
 CLK20 AD15 IO L4P_GC_4
 CLK21 AD14 IO L4N_GC_VREF_4
 CLK22 AD8 IO L5P_GC_4
 CLK23 AC7 IO L5N_GC_4
 LVDS3_PAD13 IO L6P_GC_4
 LVDS3_NAC14 IO L6N_GC_4
 CLK29 AB12 IO L7P_GC_VRN_4
 CLK26 AC11 IO L7N_GC_VRP_4
 LVTTL2 AC13 IO L8P_CC_GC_4
 LVTTL3 AC12 IO L8N_CC_GC_4
 LVDS2_PAD11 IO L9P_CC_GC_4
 LVDS2_NAD10 IO L9N_CC_GC_4

**FF676
BANK 4**

U1A HDR_FG676
 VCCO_4
 VCCO1_4 AC10
 VCCO2_4 AB13



DUT B D476 F24 IO L0P_SM8P_13
 DUT B D474 F25 IO L0N_SM8N_13
 DUT B D480 E25 IO L1P_SM7P_13
 DUT B D478 E26 IO L1N_SM7N_13
 DUT B D484 G26 IO L2P_SM6P_13
 DUT B D482 H26 IO L2N_SM6N_13
 DUT B D488 G24 IO L3P_SM5P_13
 DUT B D486 G25 IO L3N_SM5N_13
 DUT A D26 J25 IO L4P_13
 DUT B D472 VREFJ26 IO L4N_VREF_13
 DUT B D492 H24 IO L5P_SM4P_13
 DUT B D490 J24 IO L5N_SM4N_13
 DUT B D496 L24 IO L6P_SM3P_13
 DUT B D494 L25 IO L6N_SM3N_13
 DUT B D500 K25 IO L7P_SM2P_13
 DUT B D498 K26 IO L7N_SM2N_13
 DUT B D504 M25 IO L8P_CC_SM1P_13
 DUT B D502 M26 IO L8N_CC_SM1N_13
 DUT B D506 N24 IO L9P_CC_SM0P_13
 DUT A D39 P26 IO L9N_CC_SM0N_13
 DUT A D34 N26 IO L10P_CC_13
 DUT A D0 P25 IO L10N_CC_13
 DUT A D32 P24 IO L11P_CC_13
 DUT A D30 R25 IO L11N_CC_13
 DUT A D28 R26 IO L12P_VRN_13
 DUT A D24 T24 IO L12N_VRP_13
 DUT A D22 T25 IO L13P_13
 DUT A D20 V26 IO L13N_13
 DUT A D38 VREF U26 IO L14P_13
 DUT A D36 U24 IO L14N_VREF_13
 DUT A D18 U25 IO L15P_13
 DUT A D16 W25 IO L15N_13
 DUT A D14 W26 IO L16P_13
 DUT A D12 Y25 IO L16N_13
 DUT A D10 Y26 IO L17P_13
 DUT A D8 AB25 IO L17N_13
 DUT A D6 AA25 IO L18P_13
 DUT A D4 AC26 IO L18N_13
 DUT A D2 AB26 IO L19P_13

**FF676
BANK 13**

U1A HDR_FG676
 VCCO_13
 VCCO1_13 N20
 VCCO2_13 H23
 VCCO3_13 R24

DUT A D125 G20 IO L0P_11
 DUT A D127 F20 IO L0N_11
 DUT A D81 E21 IO L1P_11
 DUT A D83 E20 IO L1N_11
 DUT A D77 E22 IO L2P_11
 DUT A D79 E23 IO L2N_11
 DUT A D73 F22 IO L3P_11
 DUT A D75 F23 IO L3N_11
 DUT A D69 G21 IO L4P_11
 DUT A D126 VREF E22 IO L4N_VREF_11
 DUT A D65 H21 IO L5P_11
 DUT A D67 H22 IO L5N_11
 DUT A D61 J19 IO L6P_11
 DUT A D63 H19 IO L6N_11
 DUT A D57 H23 IO L7P_11
 DUT A D59 J23 IO L7N_11
 DUT A D53 J21 IO L8P_CC_11
 DUT A D55 J20 IO L8N_CC_11
 DUT A D49 K21 IO L9P_CC_11
 DUT A D51 K20 IO L9N_CC_11
 DUT A D121 K23 IO L10P_CC_SM15P_11
 DUT A D123 K22 IO L10N_CC_SM15N_11
 DUT A D117 L20 IO L11P_CC_SM14P_11
 DUT A D119 L19 IO L11N_CC_SM14N_11
 DUT A D115 L23 IO L12P_VRN_11
 DUT A D113 L22 IO L12N_VRP_11
 DUT A D111 M22 IO L13P_11
 DUT A D109 M21 IO L13N_11
 DUT A D107 P19 IO L14P_11
 DUT A D105 N19 IO L14N_VREF_11
 DUT A D101 M20 IO L15P_SM13P_11
 DUT A D103 M19 IO L15N_SM13N_11
 DUT A D97 P23 IO L16P_SM12P_11
 DUT A D99 N23 IO L16N_SM12N_11
 DUT A D93 N22 IO L17P_SM11P_11
 DUT A D95 N21 IO L17N_SM11N_11
 DUT A D89 R22 IO L18P_SM10P_11
 DUT A D91 R23 IO L18N_SM10N_11
 DUT A D85 P21 IO L19P_SM9P_11
 DUT A D87 P20 IO L19N_SM9N_11

**FF676
BANK 11**

U1A HDR_FG676
 VCCO_11
 VCCO1_11 F21
 VCCO2_11 J22
 VCCO3_11 H25

DUT A D466 E7 IO L0P_12
 DUT A D468 F7 IO L0N_12
 DUT A D426 E6 IO L1P_12
 DUT A D424 E5 IO L1N_12
 DUT A D422 G6 IO L2P_12
 DUT A D458 G7 IO L2N_12
 DUT A D456 F5 IO L3P_12
 DUT A D454 F4 IO L3N_12
 DUT A D452 J6 IO L4P_12
 DUT A D450 H7 IO L4N_VREF_12
 DUT A D448 H6 IO L5P_12
 DUT A D446 G5 IO L5N_12
 DUT A D444 H4 IO L6P_12
 DUT A D442 G4 IO L6N_12
 DUT A D440 J5 IO L7P_12
 DUT A D438 J4 IO L7N_12
 DUT A D436 K6 IO L8P_CC_12
 DUT A D434 K7 IO L8N_CC_12
 DUT A D432 L7 IO L9P_CC_12
 DUT A D430 M7 IO L9N_CC_12
 DUT A D428 K5 IO L10P_CC_12
 DUT A D464 L5 IO L10N_CC_12
 DUT A D462 L4 IO L11P_CC_12
 DUT A D460 L3 IO L11N_CC_12
 DUT A D420 M5 IO L12P_VRN_12
 DUT A D418 M6 IO L12N_VRP_12
 DUT A D416 N7 IO L13P_12
 DUT A D414 N6 IO L13N_12
 DUT A D410 P3 IO L14P_12
 DUT A D470 VREF N6 IO L14N_VREF_12
 DUT A D408 M4 IO L15P_12
 DUT A D406 N4 IO L15N_12
 DUT A D404 P5 IO L16P_12
 DUT A D402 P4 IO L16N_12
 DUT A D400 R3 IO L17P_12
 DUT A D398 T3 IO L17N_12
 DUT A D396 R6 IO L18P_12
 DUT A D394 R5 IO L18N_12
 DUT A D392 P6 IO L19P_12
 DUT A D390 R7 IO L19N_12

**FF676
BANK 12**

U1A HDR_FG676
 VCCO_12
 VCCO1_12 J2
 VCCO2_12 H5
 VCCO3_12 L6

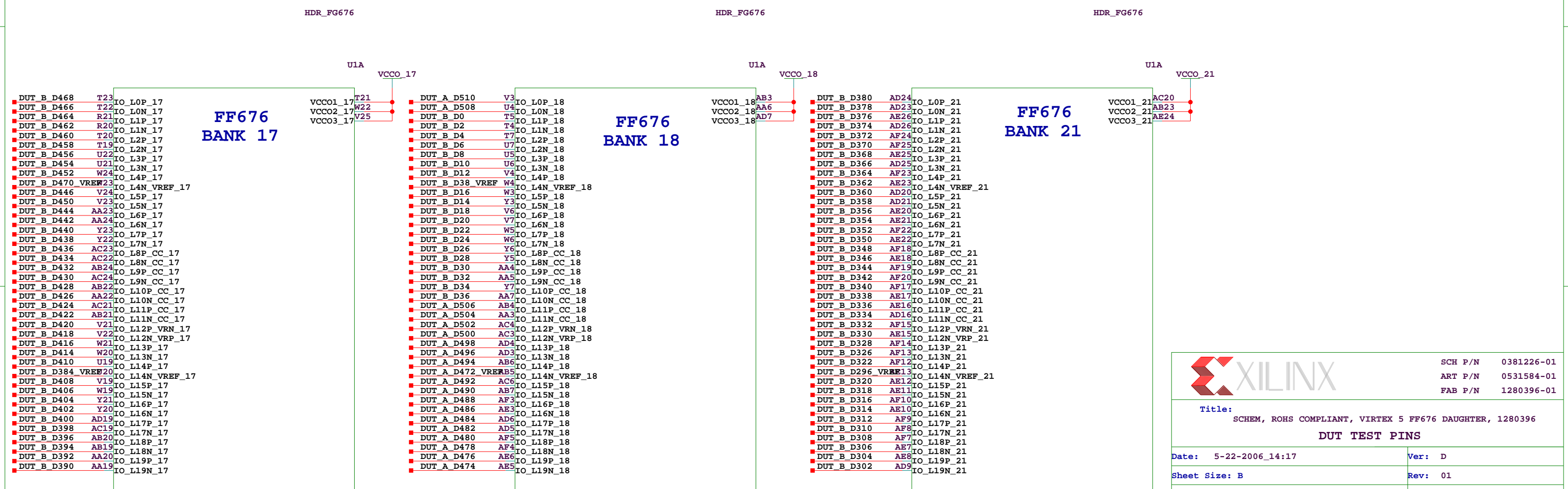
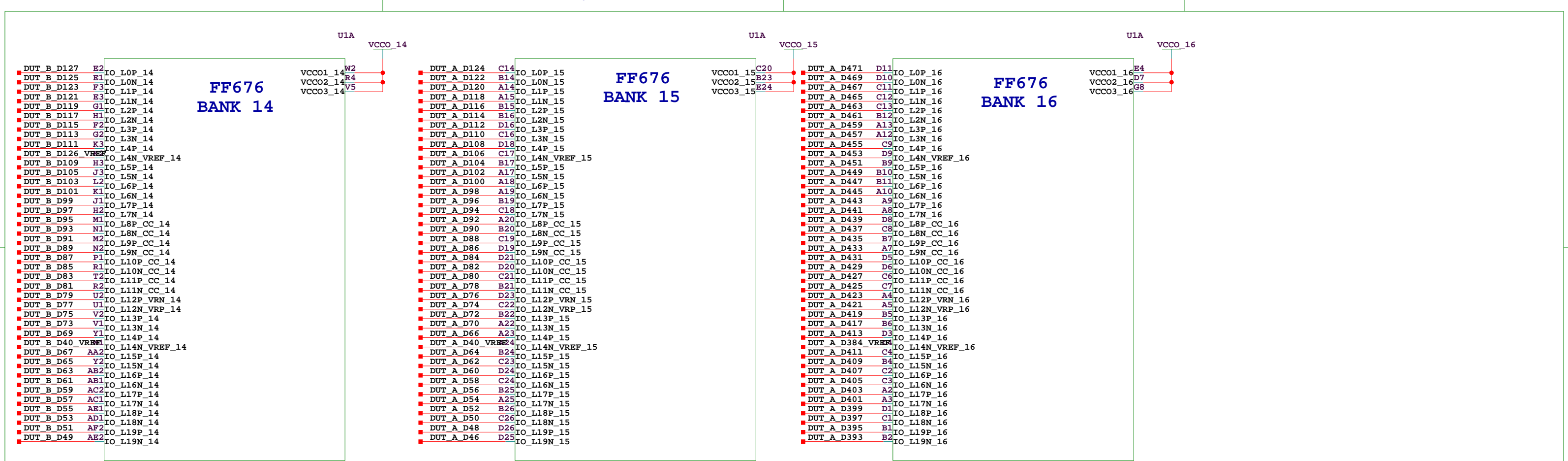



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 ART P/N 0531584-01
 FAB P/N 1280396-01

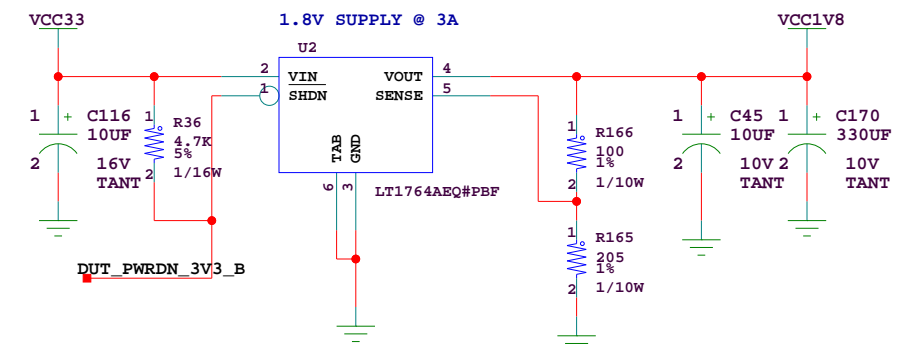
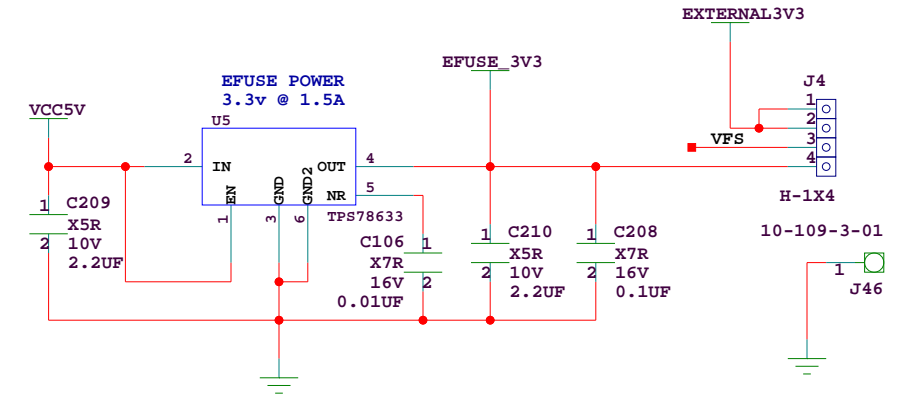
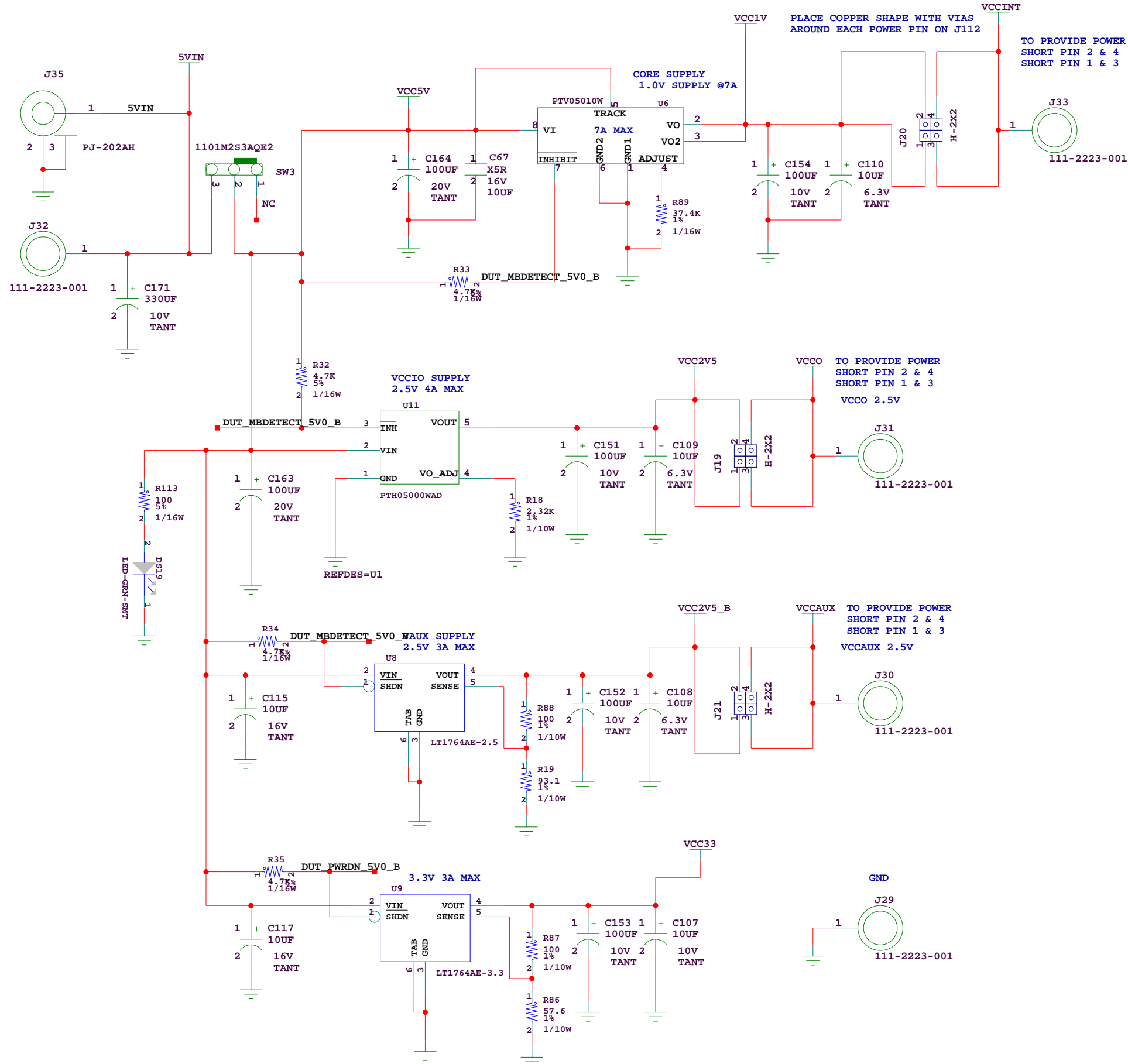
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DUT TEST PINS

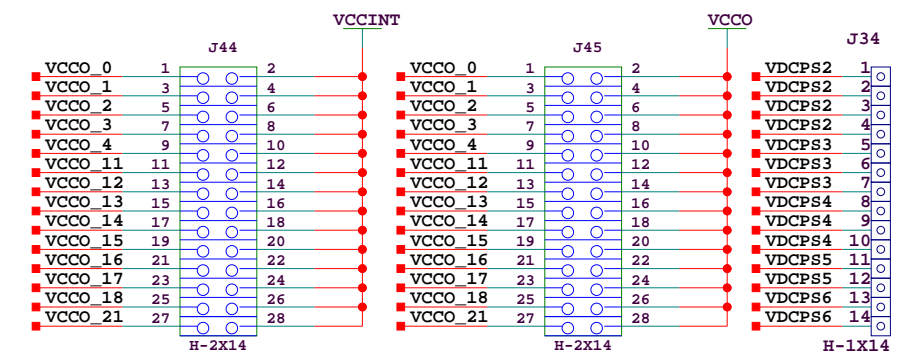
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		FAB P/N	1280396-01
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DUT TEST PINS			
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VCC I/O SELECTION

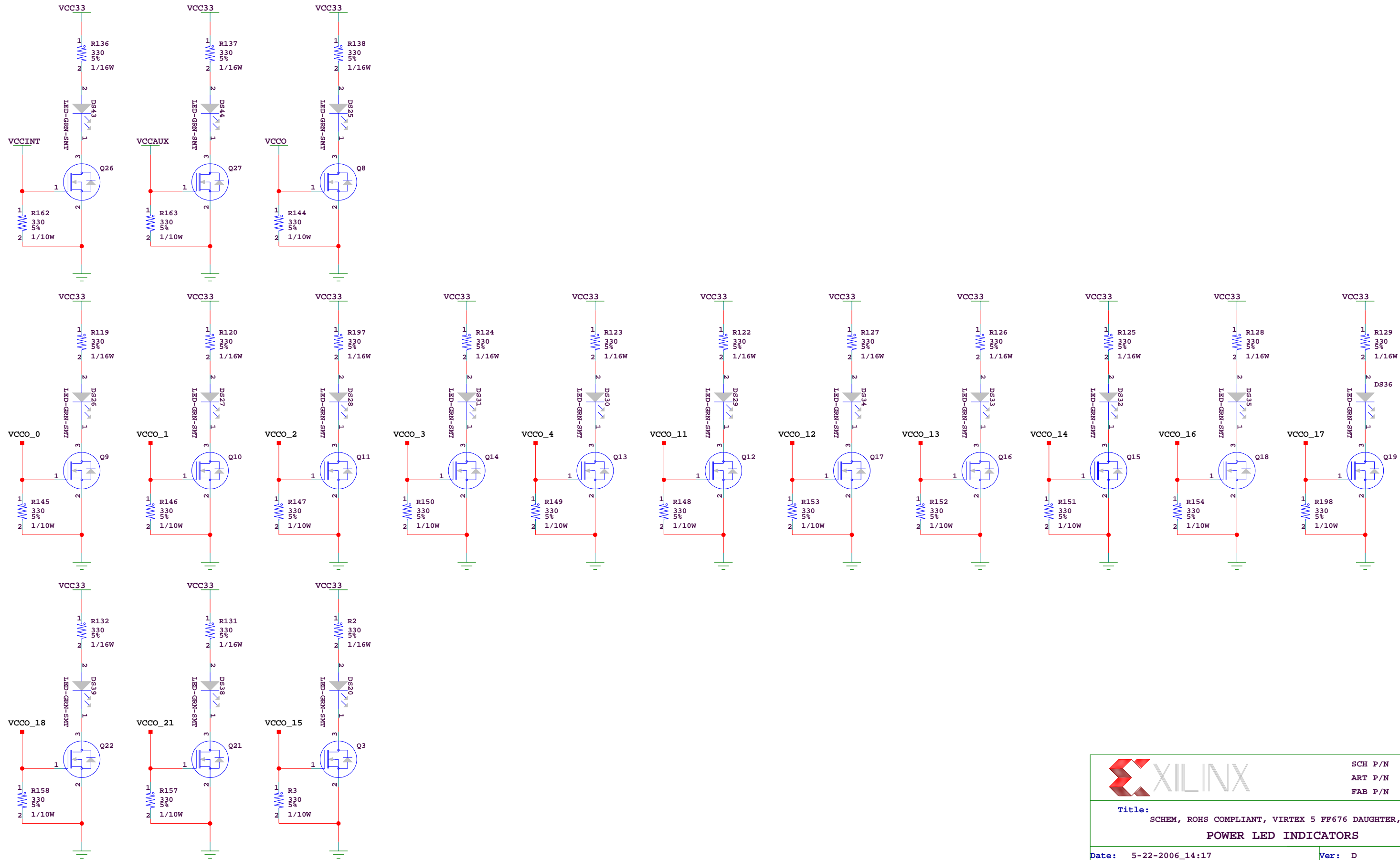



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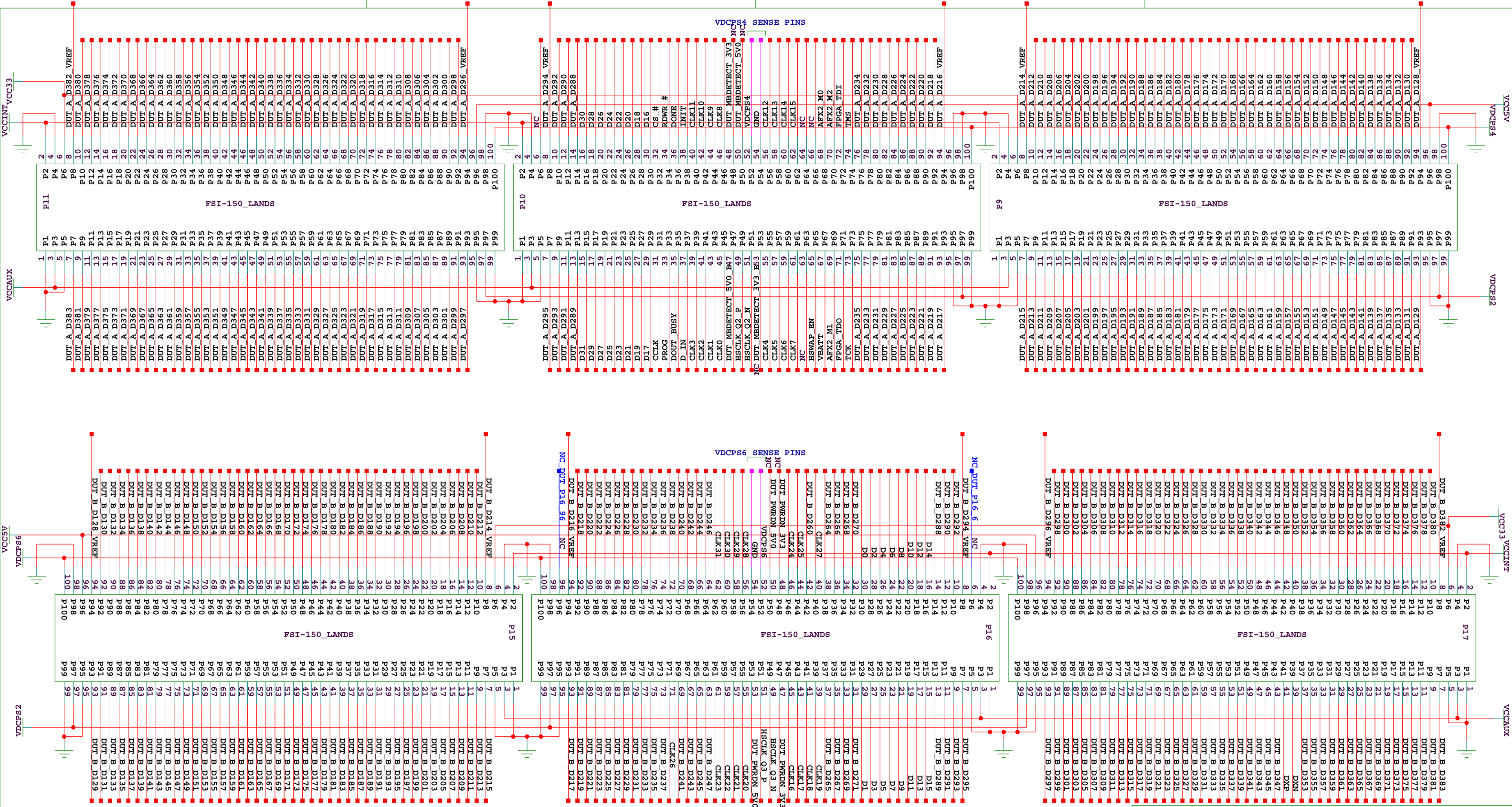
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 FAB P/N 1280396-01

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FPGA POWER SUPPLY, E-FUSE


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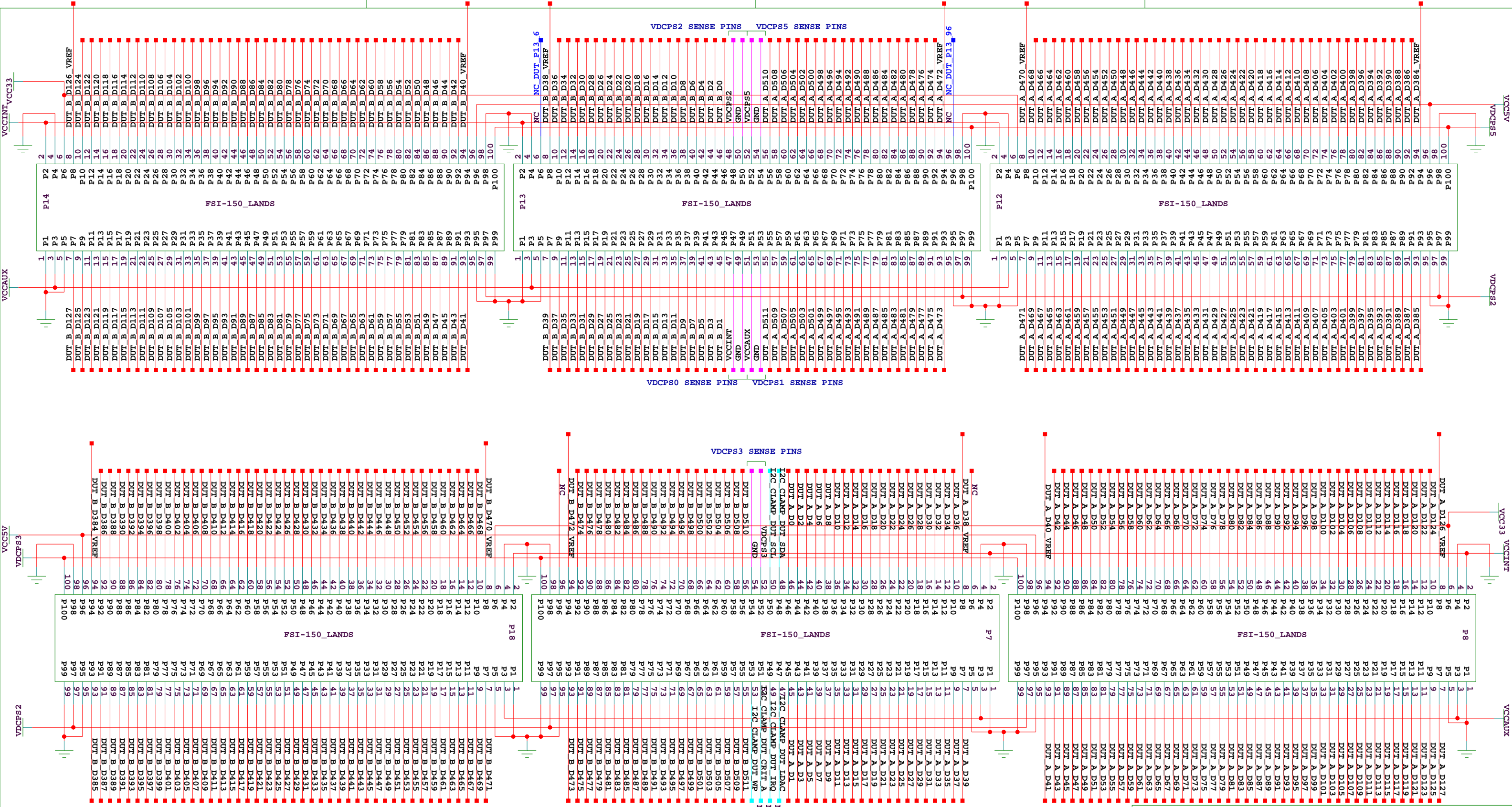


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FAB P/N	1280396-01

	
Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF676 DAUGHTER, 1280396	
AFX LANDINGS TOP AND BOTTOM	
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FAB P/N 1280396-01

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Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF676 DAUGHTER, 1280396

AFX LANDINGS LEFT AND RIGHT

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US4

US4

US4

AVDD_0	M14	AVDD_0
AVSS	M13	AVSS_0
VREF_P	P14	VREFP_0
AVSS	N13	VREFN_0
VCCO_0	Y9	VCCO1_0
VCCO_0	W12	VCCO2_0
DXP_0	R14	DXP
DXN_0	R13	DXN
VP_0	N14	VP
VP_0	P13	VN
VBATT_0	K18	VBATT
PROGRAM_B_0	J18	PROG
HSWAPEN_0	L18	HSWAP EN
D_IN_0	K11	D_IN
DONE_0	K10	DONE
CCLK_0	J10	CCLK
INIT_B_0	J11	INIT
CS_B_0	N18	CS #
RDWR_B_0	P18	RDWR #
VFS_0	R18	VFS
R_FUSE_0	T18	RFUSE
TCK_0	U11	TCK
M0_0	W18	M0
M2_0	V18	M2
M1_0	Y17	M1
TMS_0	W12	TMS
TDI_0	V11	FPGA TDI
D_OUT_BUSY_0	W11	DOUT BUSY
TDO_0	W10	FPGA TDO

FF676 BANK 0

FF676 BANK 1

FF676 BANK 2

VCCO_1	C10	VCCO1_1
VCCO_1	F11	VCCO2_1
IO_L0P_A19	G14	DUT A D290
IO_L0N_A18	F13	DUT A D288
IO_L1P_A17	H14	DUT A D291
IO_L1N_A16	H13	DUT A D289
IO_L2P_A15	D31	D31
IO_L2N_A14	D30	D30
IO_L3P_A13	D29	D29
IO_L3N_A12	D28	D28
IO_L4P_A11	D27	D27
IO_L4N_VREF_A10	D26	D26
IO_L5P_A9	D25	D25
IO_L5N_A8	D24	D24
IO_L6P_A7	D23	D23
IO_L6N_A6	D22	D22
IO_L7P_A5	D21	D21
IO_L7N_A4	D20	D20
IO_L8P_CC_A3	D19	D19
IO_L8N_CC_A2	D18	D18
IO_L9P_CC_A1	D17	D17
IO_L9N_CC_A0	D16	D16

IO_L0P_CC_RS1	Y10	DUT B D264
IO_L0N_CC_RS0	Y11	DUT B D265
IO_L1P_CC_A25	AA18	DUT B D266
IO_L1N_CC_A24	Y18	DUT B D267
IO_L2P_A23	V8	DUT B D290
IO_L2N_A22	AA8	DUT B D291
IO_L3P_A21	AA17	DUT B D288
IO_L3N_A20	AA17	DUT B D289
IO_L4P_FCS_B	AA10	DUT B D268
IO_L4N_VREF_FOE_B_MOSI	AA9	DUT B D270
IO_L5P_FWE_B	AB15	DUT B D269
IO_L5N_CSO_B	AB16	DUT B D271
IO_L6P_D7	Y12	D7
IO_L6N_D6	Y13	D6
IO_L7P_D5	AA15	D5
IO_L7N_D4	AB14	D4
IO_L8P_D3	AA12	D3
IO_L8N_D2_FS2	AB11	D2
IO_L9P_D1_FS1	AA13	D1
IO_L9N_D0_FS0	AA14	D0

FF676_SM

FF676_SM

FF676_SM

US4

US4

US4

VCCO_3	E14	VCCO1_3
VCCO_3	D17	VCCO2_3
IO_L0P_CC_GC	F14	LVDS0_P
IO_L0N_CC_GC	E13	LVDS0_N
IO_L1P_CC_GC	D13	LVTTL0
IO_L1N_CC_GC	D14	LVTTL1
IO_L2P_GC_VRN	E12	CLK2
IO_L2N_GC_VRP	F12	CLK3
IO_L3P_GC	D15	CLK6
IO_L3N_GC	E15	CLK7
IO_L4P_GC	E10	CLK8
IO_L4N_GC_VREF	E11	CLK9
IO_L5P_GC	E16	CLK10
IO_L5N_GC	E17	CLK11
IO_L6P_GC	F9	CLK12
IO_L6N_GC	F10	CLK13
IO_L7P_GC	F18	CLK27
IO_L7N_GC	F19	CLK28
IO_L8P_GC	F8	CLK18
IO_L8N_GC	E8	CLK19
IO_L9P_GC	F18	LVDS1_P
IO_L9N_GC	F17	LVDS1_N

FF676 BANK 3

FF676 BANK 11

FF676 BANK 12

VCCO_11	F21	VCCO1_11
VCCO_11	J22	VCCO2_11
VCCO_11	H25	VCCO3_11
IO_L0P_11	G20	DUT A D125
IO_L0N_11	F20	DUT A D127
IO_L1P_11	E21	DUT A D81
IO_L1N_11	E20	DUT A D83
IO_L2P_11	E22	DUT A D77
IO_L2N_11	E23	DUT A D79
IO_L3P_11	F22	DUT A D73
IO_L3N_11	F23	DUT A D75
IO_L4P_11	G21	DUT A D69
IO_L4N_VREF_11	G22	DUT A D126 VREF
IO_L5P_11	H21	DUT A D65
IO_L5N_11	H22	DUT A D67
IO_L6P_11	J19	DUT A D61
IO_L6N_11	H19	DUT A D63
IO_L7P_11	H23	DUT A D57
IO_L7N_11	J23	DUT A D59
IO_L8P_CC_11	J21	DUT A D53
IO_L8N_CC_11	J20	DUT A D55
IO_L9P_CC_11	K21	DUT A D49
IO_L9N_CC_11	K20	DUT A D51
IO_L10P_CC_SM15P_11	K22	SM15 R N
IO_L10N_CC_SM15N_11	L20	SM14 R P
IO_L11P_CC_SM14P_11	L19	SM14 R N
IO_L11N_CC_SM14N_11	L23	DUT A D115
IO_L12P_VRN_11	L22	DUT A D113
IO_L12N_VRP_11	M22	DUT A D111
IO_L13P_11	M21	DUT A D109
IO_L13N_11	P19	DUT A D107
IO_L14P_11	P19	DUT A D105
IO_L14N_VREF_11	M20	SM13 R P
IO_L15P_SM13P_11	M19	SM13 R N
IO_L15N_SM13N_11	P23	SM12 R P
IO_L16P_SM12P_11	N23	SM12 R N
IO_L16N_SM12N_11	N22	SM11 R P
IO_L17P_SM11P_11	N21	SM11 R N
IO_L17N_SM11N_11	R22	SM10 R P
IO_L18P_SM10P_11	R23	SM10 R N
IO_L18N_SM10N_11	P21	SM9 R P
IO_L19P_SM9P_11	P20	SM9 R N
IO_L19N_SM9N_11		


VCCO_4	AC10	VCCO1_4
VCCO_4	AB13	VCCO2_4
IO_L0P_GC_D15	AD18	D15
IO_L0N_GC_D14	AC18	D14
IO_L1P_GC_D13	AB10	D13
IO_L1N_GC_D12	AB9	D12
IO_L2P_GC_D11	AC17	D11
IO_L2N_GC_D10	AC16	D10
IO_L3P_GC_D9	AC8	D9
IO_L3N_GC_D8	AC9	D8
IO_L4P_GC	AD15	CLK20
IO_L4N_GC_VREF	AD14	CLK21
IO_L5P_GC	AD8	CLK22
IO_L5N_GC	AC7	CLK23
IO_L6P_GC	AD13	LVDS3_P
IO_L6N_GC	AC14	LVDS3_N
IO_L7P_GC_VRN	AB12	CLK29
IO_L7N_GC_VRP	AC11	CLK26
IO_L8P_CC_GC	AC13	LVTTL2
IO_L8N_CC_GC	AC12	LVTTL3
IO_L9P_CC_GC	AD11	LVDS2_P
IO_L9N_CC_GC	AD10	LVDS2_N

FF676 BANK 4

FF676_SM

FF676_SM

FF676_SM



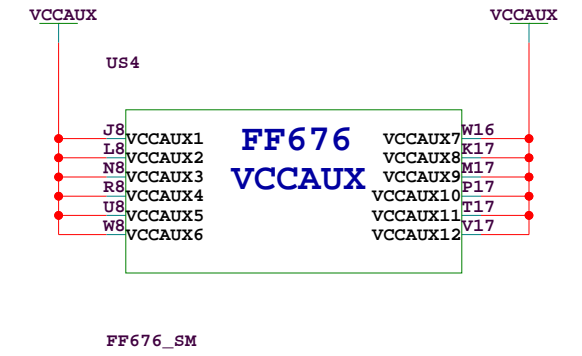
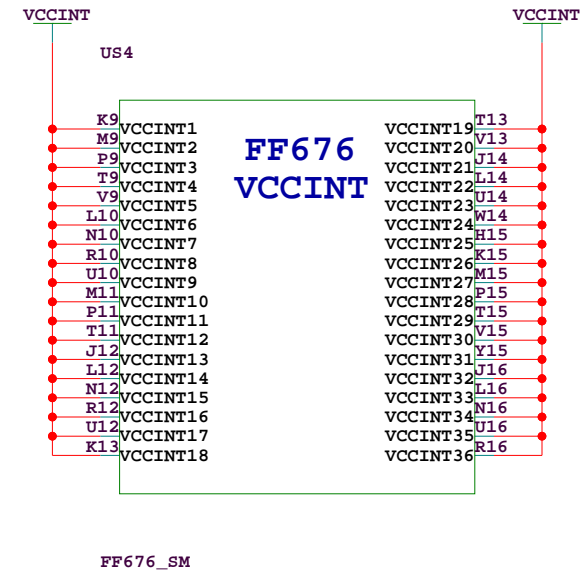
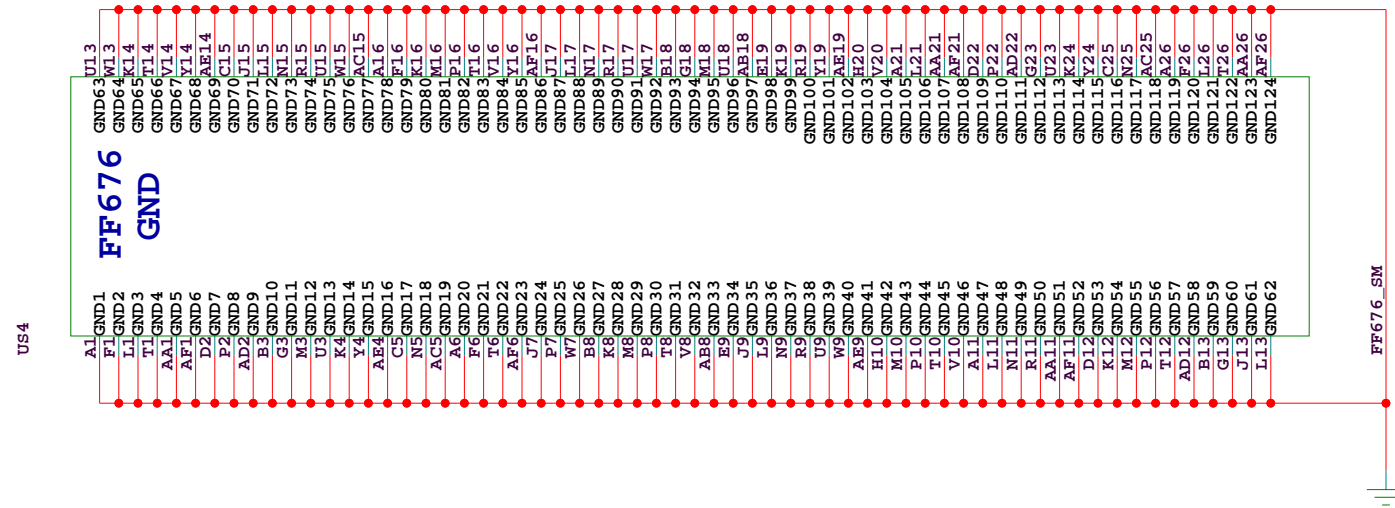
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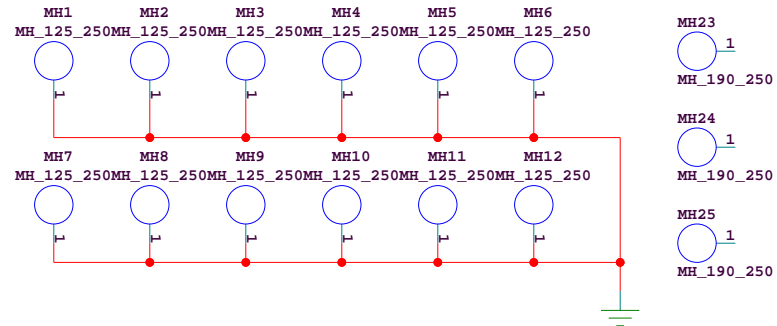


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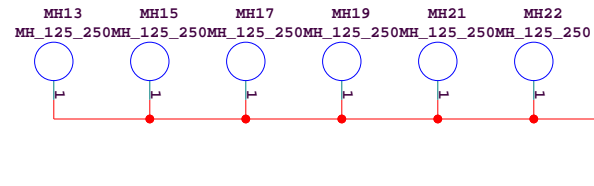
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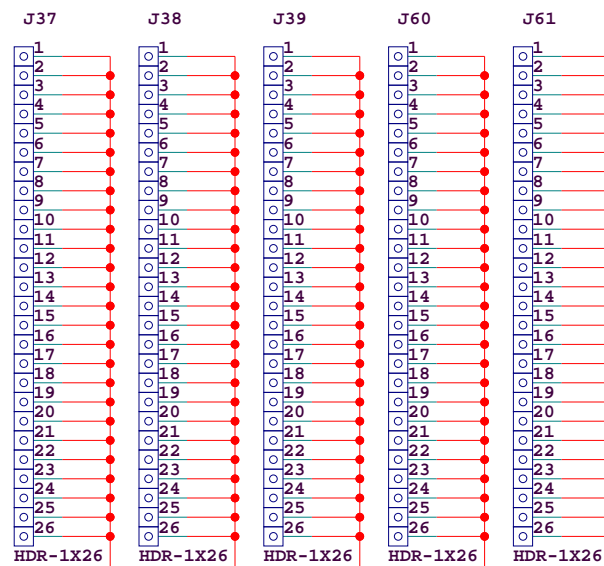
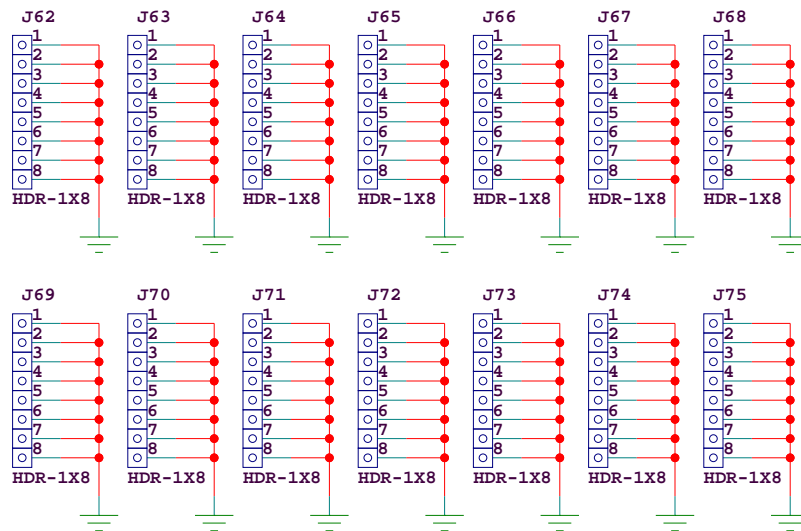
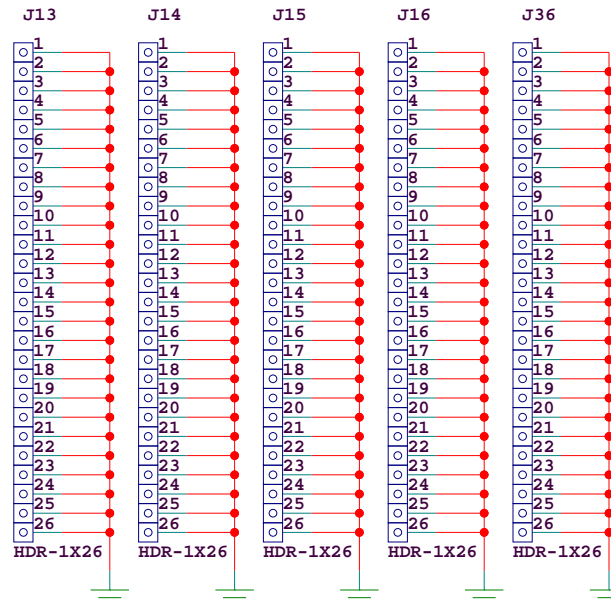
AFXII GUIDE HOLES



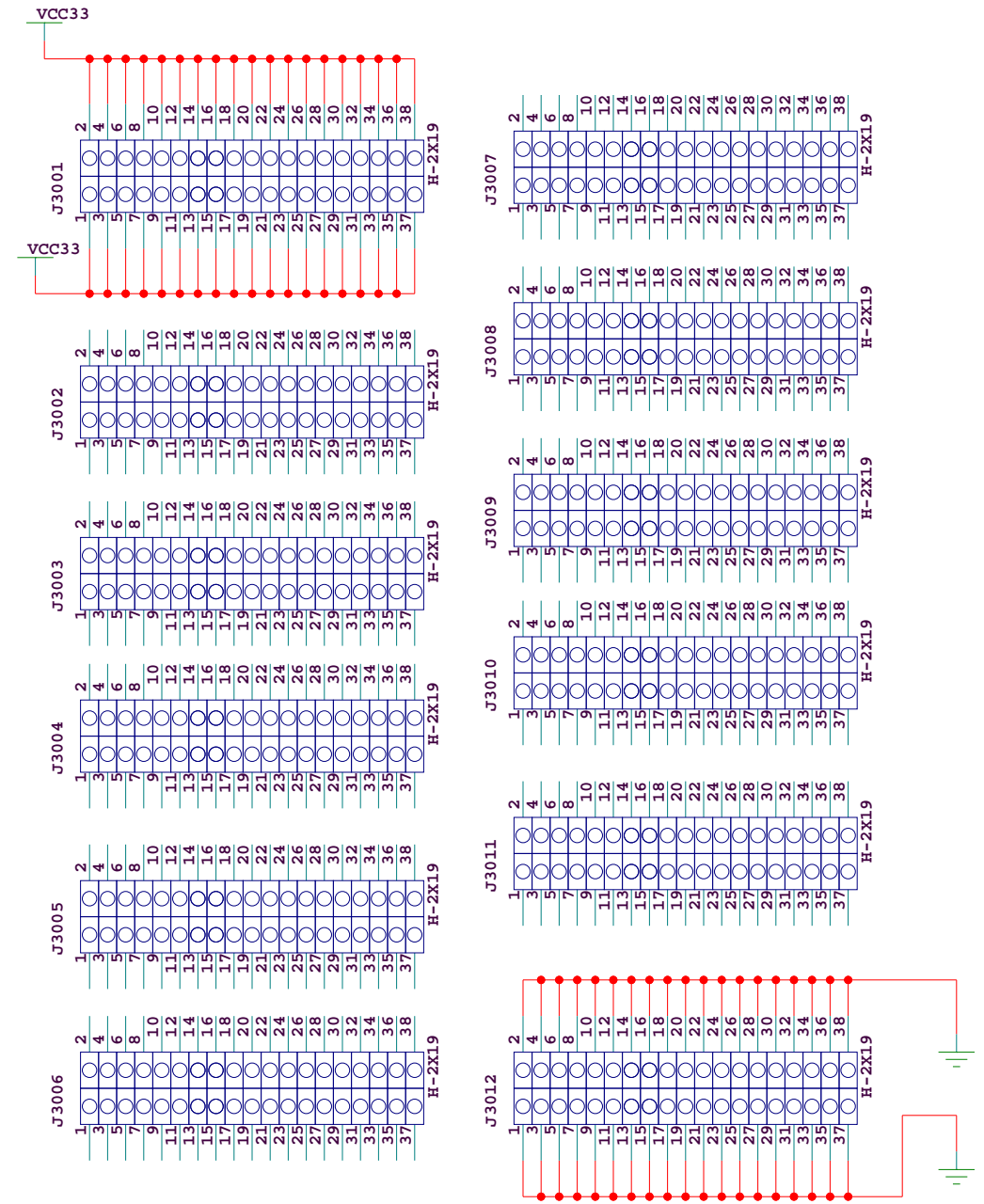
MOUNTING HOLES



DUT INTERLEAVE GND'S



BREADBOARD AREA



SCH P/N 0381226-01
ART P/N 0531584-01
FAB P/N 1280396-01

Title: SCHEM, ROHS COMPLIANT, VIRTEX 5 FF676 DAUGHTER, 1280396

HARDWARE AND BREADBOARD AREA

Date: 5-22-2006_14:17	Ver: D
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