

Figure 1: ML300 CPU  
Virtex-II Pro Based  
Block Diagram

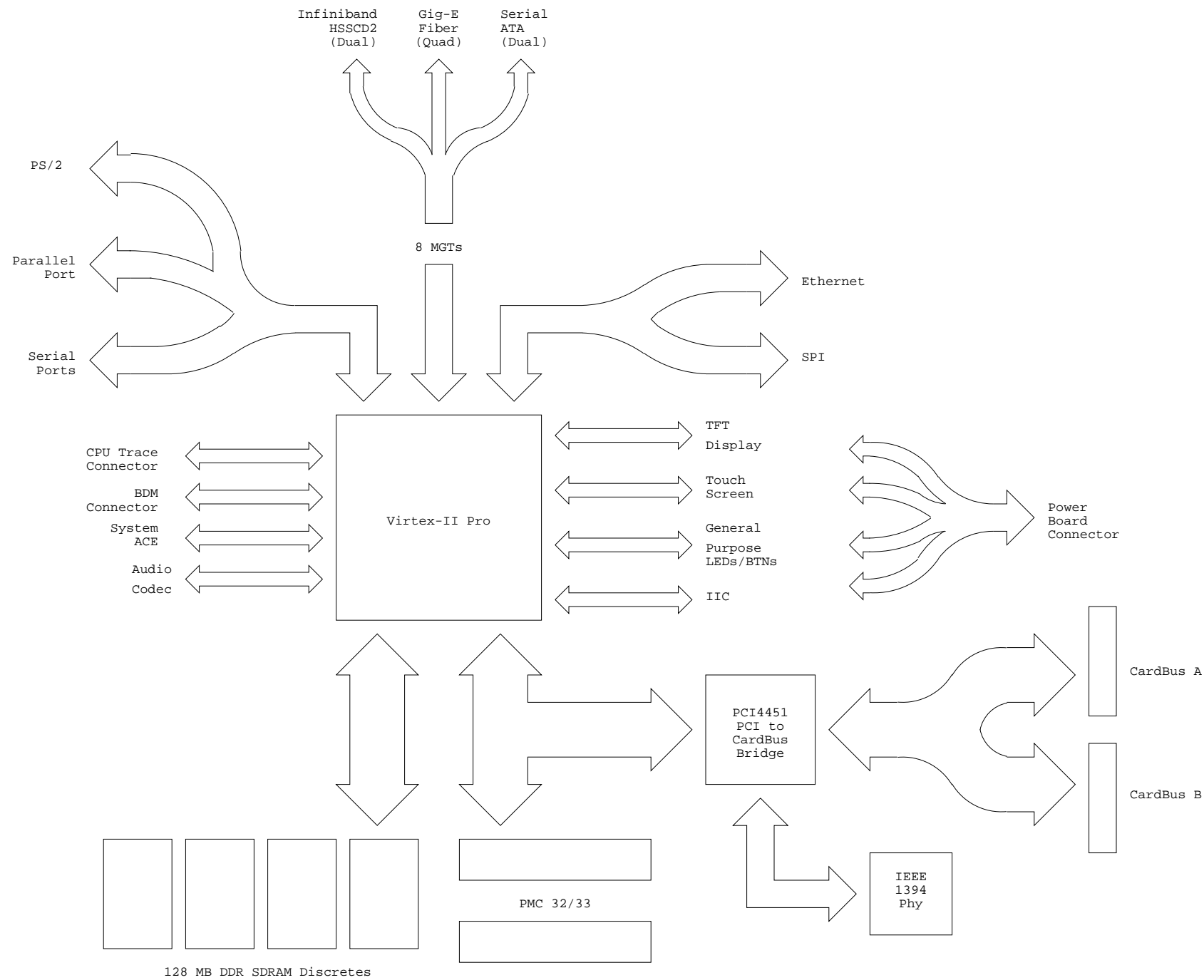


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Virtex-II Pro Based  
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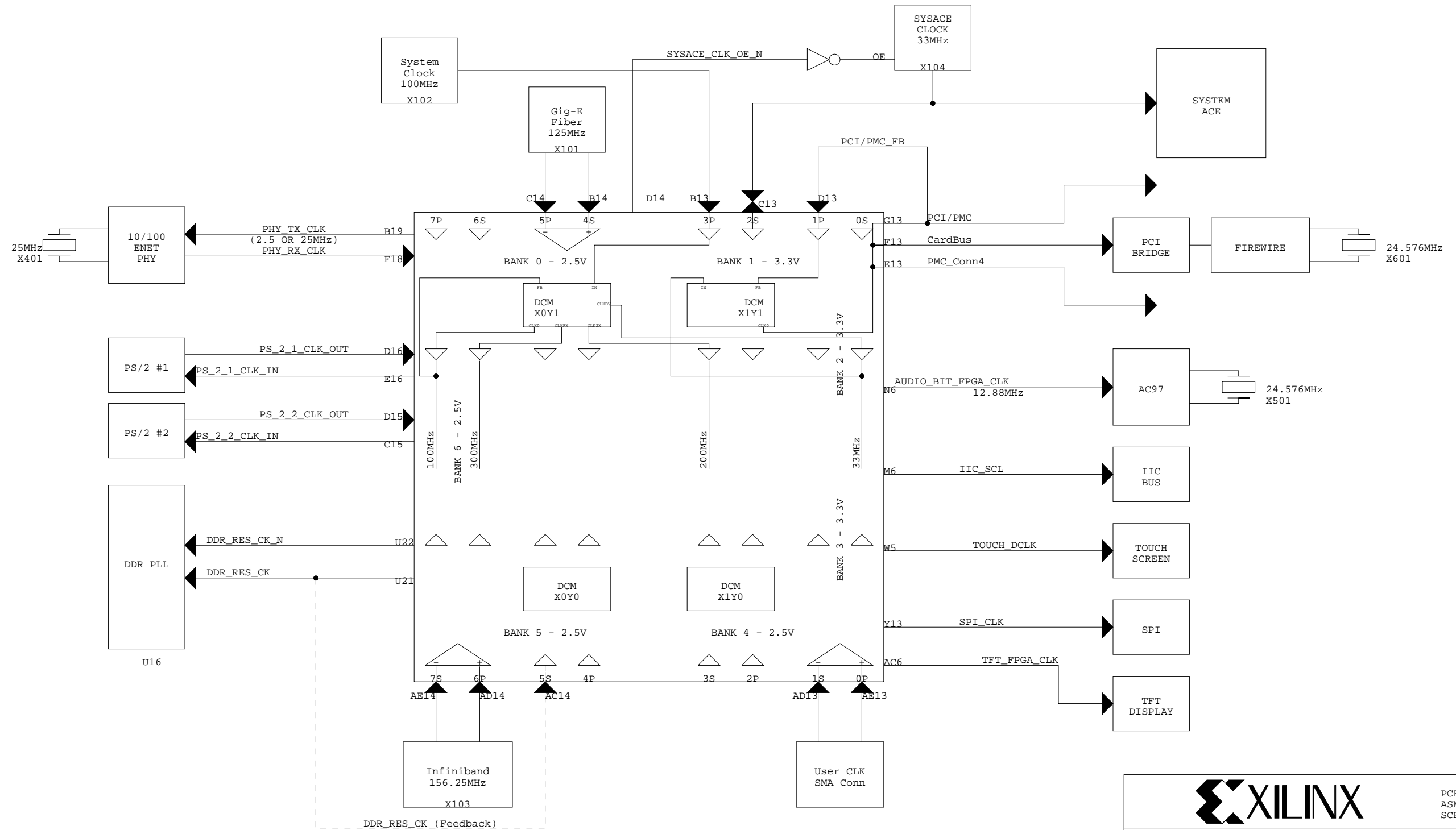


PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300\_CPU  
Board Block Diagram  
and Table of Contents

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Figure 2: ML300 CPU  
Virtex-II Pro Based  
Clocking Distribution Diagram



Notes:

1. Internal clocking structure is design dependent



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Clock Distribution Diagram

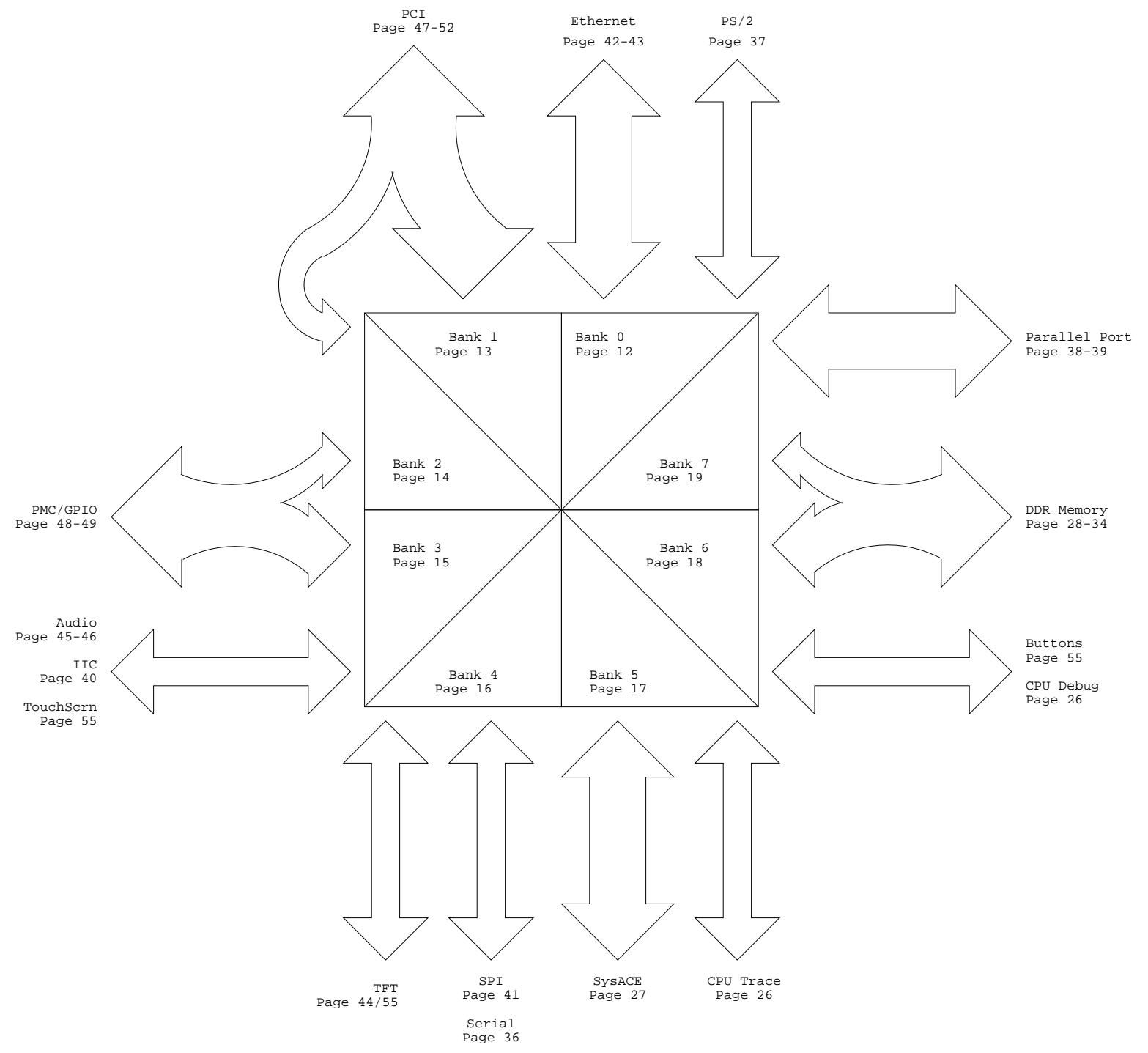
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Figure 4: ML300 CPU  
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 FPGA Bankout Diagram



MGT BLOCKS  
 Banks 0 and 1 - Page 22  
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MISC FPGA Pins  
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Table 2: ML300 CPU  
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Part Index

IC Index (U\*)

RefDes	Page	Description
U1	12-22	XC2VP7-FF672
U2	27	System ACE
U3	24	LT1963ES8 MGT VTT Linear Regulator
U4	13	PCI VCCO Linear Regulator
U6	30	HYB25D256800AT-7 DDR Chip
U7	30	HYB25D256800AT-7 DDR Chip
U8	30	HYB25D256800AT-7 DDR Chip
U9	30	HYB25D256800AT-7 DDR Chip
U14	29	SSTV16857 DDR Register
U15	29	SSTV16857 DDR Register
U16	28	CDCV857 DDR Clock Replicator
U19	37	74C914 PS/2 Buffer
U20	38	QS34XV245 Par Port Clamp Diode
U21	39	SN74LVCL161284DGGR Par Port XCVR
U22	39	SN74CBT16210DGGR Par Port LED Buf
U26	42	LXT971_LQFP64 Ethernet Phy
U27	44	74ALVC164245 TFT Level Shifter
U28	44	74ALVC164245 TFT Level Shifter
U50	47	QS32X2245 PCI Clamp Diode
U51	47	QS32X2245 PCI Clamp Diode
U52	47	QS32X2245 PCI Clamp Diode
U53	47	QS316211 PCI Clamp Diode
U58	53	TPS2216A PCMCIA Power Regulator
U59	54	TSB41AB1 IEI1394 (Firewire) Phy
U60	26	74ALVC157A JTAG/Trace MUX
U101	24	LT1963-25EQ MGT VCC Linear Reg
U251	40	MAX1617 FPGA IIC Temp Sensor
U252	40	LM76CNM_3 IIC Ambient Temp Sensor
U253	40	24LC32A IIC EEPROM
U254	41	25LC160_SN SPI EEPROM
U255	40	MAX6683 IIC Power Monitor
U256	40	MAX6652 IIC Power Monitor
U270	36	MAX3388E UART Transceiver
U271	36	MAX3388E UART Transceiver
U500	45	AD1885 Audio Codec
U501	46	LM4835 Audio Amplifier
U502	40	DS1845 IIC Audio Volume Trimpot
U601	50	PCI4451GFN PCMCIA to PCI Bridge
U802	48	QS32X2245 PMC Clamp Diode
U912	48	QS32X2245 PMC Clamp Diode
U913	48	QS32X2245 PMC Clamp Diode
U914	48	QS32X2245 PMC Clamp Diode
U1001	33	ML6554 DDR Switching Regulator

Diodes/Transistors (D\*/Q\*)

RefDes	Page	Description
D601	47	Clamp Diode VCC Diode
D602	47	Clamp Diode VCC Diode
D603	47	Clamp Diode VCC Diode
D604	47	Clamp Diode VCC Diode
D605	54	Fire Wire VCC Diode
D801	48	Clamp Diode VCC Diode
D901	48	Clamp Diode VCC Diode
D902	48	Clamp Diode VCC Diode
D903	48	Clamp Diode VCC Diode
Q101	20	Re-drive FPGA Done for LED
Q103	13	System ACE Clock OE FET
Q401	35	Re-drive Illum Signals for LEDs
Q402	35	Re-drive Illum Signals for LEDs
Q403	37	Dual FET for PS/2 Transceivers
Q404	37	Dual FET for PS/2 Transceivers
Q405	35	Re-drive Illum Signals for LEDs

Header Index (J\*)

RefDes	Page	Description
J1	16	SMA User Clock P-side
J2	16	SMA User Clock N-side
J101	55	HDR 2x32 Digital Connector #1
J102	55	HDR 2x32 Digital Connector #2
J103	55	HDR 2x25 Power Connector
J104	49	PMC Connector #1
J105	49	PMC Connector #2
J106	49	PMC Connector #4
J204	26	HDR 1x2 JTAG MUX Select
J505	46	Audio Left Speaker Jack
J506	46	Audio Right Speaker Jack

Port Index (P\*)

RefDes	Page	Description
P101	39	DB25 Parallel Port
P102	23	GIGE-R14K-ST11 Quad Fiber XCVR
P103	42	RJ45 Ethernet Port w/LEDs
P104	37	Shielded Minidin-6 PS/2 Port
P105	37	Shielded Minidin-6 PS/2 Port
P106	36	DB9 Serial Port
P107	36	DB9 Serial Port
P108	54	1394A Firewire Connector
P109	26	Trace/Debug Connector (Mictor-38)
P110	51	FCI71240-340CA Cardbus Top
P110	51	FCI71240-340CA Cardbus Bottom
P111	21	HSSCD2 (Infiniband) MGT Connector
P112	21	HSSCD2 (Infiniband) MGT Connector
P113	27	System ACE Compact Flash
P114	26	HDR 2x8 CPU Debug Connector
P115	26	HDR 2mm 2x7 JTAG Connector
P116	46	Stereo Jack Headphone/Line Out
P117	45	Stereo Jack Microphone In
P118	45	Stereo Jack Line In
P119	21	Serial ATA Connector (Host)
P120	21	Serial ATA Connector (Device)

LED Index (DS\*)

RefDes	Page	Description
DS101	20	LED0603 Blue Done LED
DS102	35	Dual LED OPB Bus Error
DS103	35	Dual LED PLB Bus Error
DS201	27	LED0603 Red System ACE Error
DS202	27	LED0603 Green System ACE Status
DS203	27	LED0603 Red INIT LED
DS401	35	Round LED Blue Illumination
DS402	35	Round LED Blue Illumination
DS403	35	Round LED Blue Illumination
DS404	35	Round LED Blue Illumination
DS405	35	Round LED Blue Illumination
DS406	35	Round LED Blue Illumination
DS407	39	LED0603 Yellow Par Port Direction
DS408	39	LED0603 Yellow Par Port User Def 3
DS409	39	LED0603 Yellow Par Port User Def 1
DS410	39	LED0603 Yellow Par Port NWait
DS411	39	LED0603 Yellow Par Port Interrupt
DS412	39	LED0603 Green Par Port Data0
DS413	39	LED0603 Yellow Par Port NASTrobe
DS414	39	LED0603 Yellow Par Port Ninit
DS415	39	LED0603 Yellow Par Port User Def 2
DS416	39	LED0603 Yellow Par Port NDStrobe
DS417	39	LED0603 Yellow Par Port Nwrite
DS418	39	LED0603 Yellow Par Port High Drain
DS419	39	LED0603 Green Par Port Data1
DS420	39	LED0603 Green Par Port Data2
DS421	39	LED0603 Green Par Port Data3
DS422	39	LED0603 Green Par Port Data4
DS423	39	LED0603 Green Par Port Data5
DS424	39	LED0603 Green Par Port Data6
DS425	39	LED0603 Green Par Port Data7
DS426	42	LED0603 Green Ethernet Link Speed
DS427	35	Round LED Blue Illumination
DS428	35	Round LED Blue Illumination
DS429	35	Round LED Blue Illumination
DS430	35	Round LED Blue Illumination

Oscillator Index (X\*)

RefDes	Page	Description
X101	12	EG2121/LV1145B Gig-E Clock 125MHz
X102	13	Half Size Osc System Clock 100MHz
X103	17	EG2121/LV1145B S-ATA/HSSCD2 Clock 156.25MHz
X104	13	Half Size Osc SysACE Clock 33MHz
X401	42	MA506 Ethernet Clock 25MHz
X501	45	MA506 Audio Clock 24.576MHz
X601	54	MA506 Firewire Clock 24.576 MHz



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SEMICONDUCTORS

QTY	REFDES	PKG	MANUFACTURE PN	MANUFACTURE	DESCRIPTION
8	D601,D602,D603,D604,D801,D901,D902,D903	SOD-323	LN4148WS-7	Diodes Inc	Diode, SMD
1	D605	MELF	LN5819M-13	Diodes Inc	Diode, SMD
11	DS101,DS401,DS402,DS403,DS404,DS405,DS406,DS427,DS428,DS429,DS430	0603	LTST-C190CBKT	Lite-On	LED, BLUE, SMD
2	DS102,DS103	LED_DUAL	LNJ115W8PRA	Panasonic	LED, Dual Red/Green, SMD
2	DS201,DS203	0603	SML-LX0603IW-TR	Lumex	LED, Red, SMD
10	DS202,DS412,DS419,DS420,DS421,DS422,DS423,DS424,DS425,DS426	0603	SML-LX0603GW-TR	Lumex	LED, Green, SMD
11	DS407,DS408,DS409,DS410,DS411,DS413,DS414,DS415,DS416,DS417,DS418	0603	SML-LX0603YW-TR	Lumex	LED, Yellow, SMD
5	Q101,Q103,Q401,Q402,Q405	SOT23	BSS138	Fairchild	Diode, SMD
2	Q403,Q404	SOT363	MMDT3904-7	Diodes Inc	Transistor, Dual NPN
1	U1	FP672	XC2VP7-6FP672C	Xilinx	IC, FPGA, XC2VP7-6FP672C
1	U2	TQFP144	XCCACE-TQ144I	Xilinx	IC, Logic, SystemACE
1	U3	LINEAR_SO8	LT1963ES8	Linear Tech	IC, Linear, Voltage Reg, 1.5A, Adjustable, LDO
1	U4	LINEAR_SO8	LT1763CS8	Linear Tech	IC, Linear, Voltage Reg, 500mA, Adjustable, LDO
4	U6,U7,U8,U9	TSOP_66	HYB25D256800AT-7	Infineon	IC, Memory, DDR SDRAM, 256Mbit
2	U14,U15	TVSOP48	SN74ASSTV16857DGVR	TI	IC, Logic, 14 bit register, SSTL2, Dual Phase Clock
1	U16	TSSOP48	CDCV857DGGR	TI	IC, Analog, Phase Lock Loop
1	U19	SOIC14	DM74AS1034AM	National	IC, Logic, Hex Driver
1	U20	MILLIPAQ80	QS34XV245Q3	IDT	IC, Logic, Quickswitch, 32 bit
1	U21	TSSOP48	SN74LVC161284DGGR	TI	IC, Logic, IEEE-1284 Driver & Level Translator
1	U22	TSSOP48	SN74CBTD16210DGGR	TI	IC, Logic, Bus Switch, 20 bit, Level Translator
1	U26	LQFP64	DJLXT971ALCA4834105	Intel	IC, Logic, Ethernet PHY
2	U27,U28	TSSOP48	SN74ALVC164245DGGR	TI	IC, Logic, Transceiver, 16 bit
7	U50,U51,U52,U802,U912,U913,U914	QVSOP40	QS32X2245Q2	IDT	IC, Logic, Quickswitch, 16 bit
1	U53	TSSOP56	QS316211PA	IDT	IC, Logic, Quickswitch, 24 bit
1	U58	DAP32	TPS2216ADAP	TI	IC, Analog, Power Switch for PCMCIA
1	U59	S-PQFP-G48	TSB41AB1PHP	TI	IC, Logic, IEEE-1394a PHY
1	U60	TSSOP16	SN74LVC157APWR	TI	IC QUAD, 2-1 DATA SEL/MUX
1	U101	5-DD	LT1963EQ-25	Linear Tech	IC, Linear, Voltage Reg, 1.5A, 2.5V, LDO
1	U251	QSOP16	MAX1617AMEE	Maxim	IC, Linear, IIC Remote Diode Temperature Sensor
1	U252	SOP8	LM76CNM-3	National	IC, Linear, IIC Temperature Sensor
1	U253	SOIC8	24LC32A/SN	Microchip	IC, Memory, IIC EPROM, 32K
1	U254	SOIC8	25LC160/SN	Microchip	IC, Memory, SPI EPROM, 16K
1	U255	10_UMAX	MAX6683AUB	Maxim	IC, Logic, System Monitor, 1.8V, 2.5V, 5V
1	U256	10_UMAX	MAX6652AUB	Maxim	IC, Logic, System Monitor, 12V, 2.5V, 3.3V
2	U270,U271	TSSOP24	MAX3388ECUG	Maxim	IC, Analog, RS-232 Level Translator
1	U500	LQFP48	AD1885JST	Analog	IC, Logic, AC97 Audio Codec, SMD
1	U501	TSSOP28	LM4835MTE	National	IC, Analog, Audio Amplified, 1W
1	U502	TSSOP14	DS1845E-010/T&R	Dallas Semi	IC, Analog, Potentiometer, IIC controlled, dual
1	U601	S-PBGA-N256	PCI4451GFN	TI	IC, Logic, PCI to PCMCIA / CardBus Bridge
1	P102		R14K-ST11	Stratos Lightwave	IC, Optical Transceiver, Gigabit Etherent, 4X

OSCILLATORS / CRYSTALS

QTY	REFDES	FREQUENCY	MANUFACTURE PN	MANUFACT	DESCRIPTION
1	X101	125.000 MHZ	LV11B003-125.0M	Pletronics	Oscillator, SMT
1	X102	100.000 MHZ	EH1325HSTS-100.000M	Ecliptek	Oscillator, TH, Half Size
1	X103	156.250 MHZ	LV11B004-156.25M	Pletronics	Oscillator, SMT
1	X104	33.000 MHZ	EH1325HSTS-33.000M	Ecliptek	Oscillator, TH, Half Size
1	X401	25.000 MHZ	MA-506 25.000M-C0	Epson	Crystal, 25.000 MHz, MA_506
2	X501,X601	24.576 MHZ	MA-506 24.576M-C0	Epson	Crystal, 24.576 MHz, MA_506

ML300 CPU - BOM

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CAPACITORS

QTY	REFDES	VALUE	TOL	VOLT	KIND	PKG	MANUFACTURE PN	MANUFACTURE
2	C542,C543	220UF	10%	10V	TANT	X	T491X227K010AS	Kemet
5	C1001,C1002,C1003,C1008,C1009	220UF	20%	6.3V	TANT	D	EEJ-L0JD227R	Panasonic
1	C191	100UF	20%	10V	TANT	D	ECS-T1AD107R	Panasonic
8	C787,C788,C789,C790,C791,C792,C793,C794	47UF	20%	6.3V	TANT	B	ECS-T0JX476R	Panasonic
6	C188,C192,C197,C673,C675,C795	33UF	20%	10V	TANT	B	ECS-T1AX336R	Panasonic
1	C356	22UF	20%	6.3V	TANT	A	ECS-T0JY226R	Panasonic
3	C674,C796,C797	10UF	20%	20V	TANT	C	ECS-T1DC106R	Panasonic
5	C512,C519,C522,C528,C537	10UF	20%	16V	TANT	B	ECS-T1CX106R	Panasonic
23	C16,C18,C21,C189,C230,C231,C317,C318,C319,C320,C321,C322,C323,C324,C335,C336,C337,C338,C339,C340,C346,C352,C1028	10UF	20%	10V	TANT	A	ECS-T1AY106R	Panasonic
2	C103,C106	10UF	+80/-20	6.3V	CERAMIC	0805	ECJ-2FF0J106Z	Panasonic
8	C180,C181,C182,C183,C184,C185,C186,C187	22UF	12%	6.3V	CERAMIC	1206	C1206C226Z9VACTU	Kemet
12	C775,C776,C777,C778,C779,C780,C781,C783,C784,C785,C786,C1012	4.7UF	10%	16V	TANT	A	T491A475K016AS	Kemet
7	C516,C517,C525,C526,C527,C534,C538	1UF	10%	20V	TANT	A	T491A105K020AS	Kemet
2	C10,C19	1UF	+80/-20	10V	CERAMIC	0603	ECJ-1VF1A105Z	Panasonic
2	C532,C533	0.33UF	10%	35V	TANT	A	T491A334K035AS	Kemet
5	C501,C502,C503,C504,C506	0.33UF	10%	16V	CERAMIC	0805	ECJ-2YB1C334K	Panasonic
32	C120,C121,C122,C123,C124,C125,C126,C127,C128,C129,C130,C131,C132,C133,C134,C135,C140,C141,C142,C143,C144,C145,C146,C147,C148,C149,C150,C151,C152,C153,C154,C155	0.22UF	10%	25V	CERAMIC	0805	ECJ-2YB1E224K	Panasonic
12	C270,C271,C272,C273,C274,C275,C276,C277,C278,C279,C678,C682	0.22UF	10%	10V	CERAMIC	0603	ECJ-1VB1A224K	Panasonic
205	C9,C11,C12,C13,C17,C20,C22,C23,C102,C105,C193,C194,C195,C196,C215,C216,C217,C218,C219,C220,C221,C222,C223,C224,C225,C226,C227,C228,C229,C250,C252,C253,C254,C255,C280,C281,C301,C302,C303,C304,C305,C306,C307,C308,C309,C310,C311,C312,C313,C314,C315,C325,C326,C327,C328,C329,C330,C331,C332,C333,C334,C341,C342,C343,C344,C345,C347,C348,C349,C350,C351,C353,C354,C355,C357,C358,C359,C360,C361,C362,C363,C364,C365,C511,C513,C520,C521,C523,C524,C529,C530,C531,C535,C536,C541,C676,C677,C679,C680,C681,C690,C693,C697,C698,C701,C702,C703,C704,C705,C706,C707,C708,C709,C710,C711,C712,C713,C714,C715,C716,C717,C718,C719,C720,C721,C722,C723,C724,C725,C726,C727,C728,C729,C730,C731,C732,C733,C734,C735,C736,C737,C738,C739,C740,C741,C742,C743,C744,C745,C746,C747,C748,C749,C750,C751,C752,C753,C754,C755,C756,C757,C758,C759,C760,C761,C762,C763,C764,C765,C766,C767,C768,C769,C770,C771,C772,C773,C774,C801,C802,C803,C804,C805,C806,C807,C808,C809,C1004,C1005,C1011,C1013,C1014,C1015,C1016,C1017,C1018,C1019,C1020,C1021,C1022,C1023,C1024,C1025,C1026,C1027	0.1UF	+80/-20	16V	CERAMIC	0402	ECJ-0EF1C104Z	Panasonic
31	C5,C26,C112,C113,C114,C115,C116,C117,C118,C119,C156,C157,C158,C159,C160,C161,C164,C165,C166,C167,C168,C169,C172,C173,C176,C177,C686,C688,C689,C691,C696	0.01UF	10%	16V	CERAMIC	0402	C0402C103K4RACTU	Kemet
2	C539,C540	68000PF	10%	10V	CERAMIC	0402	ECJ-0EB1A683K	Panasonic
1	C518	47000PF	10%	10V	CERAMIC	0402	ECJ-0EB1A473K	Panasonic
1	C251	2200PF	10%	25V	CERAMIC	0402	C0402C222K3RACTU	Kemet
3	C1,C2,C3	1000PF	10%	2000V	CERAMIC	1812	1808B102K202NT	Novacap
11	C14,C15,C24,C25,C101,C104,C687,C692,C694,C695,C1010	1000PF	10%	50V	CERAMIC	0402	ECJ-0EB1H102K	Panasonic
2	C507,C508	470PF	10%	25V	CERAMIC	0402	ECJ-0EB1E471K	Panasonic
4	C4,C6,C514,C515	270PF	5%	50V	CERAMIC	0603	ECJ-1VC1H271J	Panasonic
1	C685	220PF	5%	50V	CERAMIC	0402	ECJ-0EC1H221J	Panasonic
2	C1006,C1007	30PF	5%	50V	CERAMIC	0402	ECU-E1H300JCQ	Panasonic
2	C509,C510	22PF	5%	50V	CERAMIC	0402	ECJ-0EC1H220J	Panasonic
2	C7,C8	18PF	5%	50V	CERAMIC	0402	ECJ-0EC1H180J	Panasonic
2	C683,C684	12PF	5%	50V	CERAMIC	0402	ECJ-0EC1H120J	Panasonic
1	C366	10PF	5%	50V	CERAMIC	0402	ECJ-0EC1H100D	Panasonic

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RESISTORS

QTY	REFDES	VALUE	TOL	WATT	PKG	MANUFACTURE PN	MANUFACTURE
2	R512,R633	1M	5%	1/16W	0402	ERJ-2GEJ105X	Panasonic
1	R634	402K	1%	1/16W	0402	ERJ-2RKF4023X	Panasonic
4	R538,R539,R1002,R1005	100K	1%	1/16W	0402	ERJ-2RKF1003X	Panasonic
3	R514,R515,R516	47.0K	1%	1/16W	0402	9C04021A4702FLHF3	Yageo America
1	R676	43.0K	1%	1/16W	0402	9C04021A4302FLHF3	Yageo America
1	R450	22.1K	1%	1/16W	0402	ERJ-2RKF2212X	Panasonic
10	R518,R519,R520,R521,R523,R524,R525,R526,R527,R528	20.0K	1%	1/16W	0402	ERJ-2RKF2002X	Panasonic
25	R170,R222,R223,R224,R225,R250,R251,R252,R254,R255,R407,R408,R415,R418,R513,R619,R620,R621,R622,R641,R642,R833,R945,R946,R947	10.0K	1%	1/16W	0402	ERJ-2RKF1002X	Panasonic
1	R501	6.80K	1%	1/16W	0402	9C04021A6801FLHF3	Phycomp
1	R637	6.34K	1%	1/16W	0402	ERJ-2RKF6341X	Panasonic
1	R632	5.10K	1%	1/16W	0402	9C04021A5101FLHF3	Yageo America
46	R125,R129,R133,R180,R208,R209,R210,R211,R212,R217,R218,R221,R260,R261,R262,R263,R264,R409,R410,R411,R414,R439,R444,R462,R463,R464,R465,R491,R495,R496,R498,R499,R503,R504,R505,R506,R507,R508,R509,R624,R628,R647,R659,R675,R702,R1006	4.7K	5%	1/16W	0402	ERJ-2GEJ472X	Panasonic
1	R510	2.00K	1%	1/16W	0402	ERJ-2RKF2001X	Panasonic
4	R412,R413,R416,R417	1.80K	1%	1/16W	0402	9C04021A1801FLHF3	Yageo America
15	R167,R213,R214,R215,R216,R269,R535,R536,R629,R638,R639,R643,R644,R645,R1001	1.00K	1%	1/16W	0402	ERJ-2RKF1001X	Panasonic
1	R166	487R	1%	1/16W	0402	ERJ-2RKF4870X	Panasonic
1	R171	330R	1%	1/16W	0402	9C04021A3300FLHF3	Yageo America
3	R253,R441,R443	200R	1%	1/16W	0402	ERJ-2RKF2000X	Panasonic
8	R146,R147,R148,R149,R150,R151,R152,R153	180R	1%	1/16W	0402	9C04021A1800FLHF3	Yageo America
23	R105,R106,R113,R114,R419,R420,R421,R422,R423,R424,R425,R426,R427,R428,R429,R430,R431,R432,R433,R434,R435,R436,R437	130R	1%	1/16W	0402	ERJ-2RKF1300X	Panasonic
16	R107,R119,R120,R121,R122,R123,R124,R169,R174,R175,R176,R179,R265,R266,R1003,R1004	100R	1%	1/16W	0402	ERJ-2RKF1000X	Panasonic
11	R127,R401,R402,R403,R404,R405,R406,R466,R467,R468,R469	64.9R	1%	1/16W	0402	ERJ-2RKF64R9X	Panasonic
7	R183,R185,R268,R630,R631,R635,R636	56.2R	1%	1/16W	0402	ERJ-2RKF56R2X	Panasonic
5	R184,R186,R220,R625,R626	51.1R	1%	1/16W	0402	ERJ-2RKF51R1X	Panasonic
16	R302,R303,R304,R305,R309,R310,R315,R316,R317,R318,R440,R442,R445,R446,R447,R448	49.9R	1%	1/16W	0402	ERJ-2RKF49R9X	Panasonic
1	R182	38.3R	1%	1/8W	0805	9C08052A38R3FKHFT	Yageo America
1	R181	26.1R	1%	1/8W	0805	9C08052A26R1FKHFT	Yageo America
8	R108,R172,R173,R219,R307,R308,R438,R1007	25.5R	1%	1/16W	0402	ERJ-2RKF25R5X	Panasonic
7	R301,R306,R311,R312,R313,R314,R319	22.1R	1%	1/16W	0402	ERJ-2RKF22R1X	Panasonic
11	R449,R452,R453,R454,R455,R456,R457,R458,R459,R460,R461	20.0R	1%	1/16W	0402	ERJ-2RKF20R0X	Panasonic
2	R533,R534	0R	5%	1/10W	0805	ERJ-6GEY0R00V	Panasonic
15	R134,R135,R136,R137,R138,R139,R140,R141,R168,R226,R227,R451,R623,R627,R640	0R	5%	1/16W	0402	ERJ-2GE0R00X	Panasonic
35	RP302,RP303,RP304,RP308,RP311,RP315,RP316,RP317,RP318,RP319,RP320,RP321,RP322,RP323,RP324,RP325,RP326,RP327,RP328,RP332,RP347,RP348,RP350,RP351,RP353,RP354,RP356,RP357,RP359,RP360,RP361,RP362,RP363,RP910,RP914	22R	5%	1/16W	8PIN	742C083220JTR	CTS
17	RP329,RP330,RP331,RP336,RP338,RP339,RP340,RP341,RP344,RP345,RP346,RP349,RP352,RP355,RP358,RP365,RP603	47R	5%	1/16W	8PIN	EXB-E10C470J	Panasonic
2	RP401,RP402	4.7K	5%	1/16W	8PIN	742C083472JTR	CTS
5	RP601,RP602,RP604,RP605,RP606	4.7K	5%	1/16W	8PIN	EXB-E10C472J	Panasonic

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OTHER						
QTY	REFDES	VALUE	TOL	PKG	MANUFACTURE PN	MANUFACTURE
1	F601	1.1A		2920	SMD100-2	RayChem Fuse, 1.1A, SMD, Self Healing
33	FB101,FB102,FB103,FB104,FB105,FB106,FB107,FB108,FB109,FB110,FB111,FB112,FB113,FB114,FB115,FB116,FB117,FB118,FB119,FB120,FB121,FB122,FB123,FB124,FB125,FB126,FB127,FB128,FB129,FB130,FB131,FB132,FB601	1000_OHM		0805	BLM21AH102SN1D	Murata Ferrite Bead, SMD
8	FB133,FB134,FB135,FB136,FB137,FB138,FB139,FB140	47UH	10%	1210	ELJ-PA470KF	Panasonic Inductor, SMD
8	FB141,FB403,FB405,FB406,FB501,FB502,FB603,FB605	125_OHM		1812	CTCB1812-125S	CTParts Ferrite Bead, SMD
8	FB301,FB302,FB402,FB404,FB602,FB604,FB606,FB607	60_OHM		1210	CTCB1210-600S	CTParts Ferrite Bead, SMD
1	L1001	3.3UH		DO3316	DO3316P-332	Coilcraft Inductor, SMD
1	T401			SOIC16	TG110-S050N2	Halo Transformer, Ethernet Pulse
1	PCB1					Ambitech ML300_CPU Printed Circuit Board
1	PCB1b					Axiom ML300_CPU Printed Circuit Board Assembly
1	ML300_SERNUM_LABEL					Axiom Label, Polyimide, ML300 Serial Number
1	ML300_MACID_LABEL					Axiom Label, Polyimide, MAC BASE ADDR

HARDWARE				DO NOT POPULATE PARTS			
QTY	DESCRIPTION	MANU PN	MANU	QTY	REFDES	STATE	PKG
6	Hardware, Screw, 4-40 x 3/8, Pan Head, SS	MS51957-15	Olander	2	R531,R532	DNP	805
4	Hardware, Screw, 2-56 x 3/4, Pan Head, SS	2C75PPMS	Olander	8	R130,R256,R257,R258,R259,R267,R502,R649	DNP	402
2	Hardware, Screw, 2-56 x 3/8, Pan Head, SS	2C37PPMS	Olander	2	J505,J506	DNP	SIP2
12	Hardware, Washer, Flat 4-40 SS	620C4L	Olander	3	E601,E603,E605	DNP	BOWTIE_OPEN
6	Hardware, Washer, Lock, 4-40 SS	4NSLWS	Olander	3	E602,E604,E606	DNP	BOWTIE_CLOSED
6	Hardware, Nut, 4-40, SS	4CHNTS	Olander	6	MH1,MH2,MH3,MH4,MH5,MH6	DNP	JACK_109_280
6	Hardware, Washer, Lock 2-56 SS	2NSLWS	Olander	4	MH7,MH8,MH9,MH10	DNP	JACK_116_280
6	Hardware, Washer, Flat 2-56 SS	620C2	Olander	34	TP101,TP102,TP104,TP105,TP106,TP107,TP108,TP214,TP215,TP216,TP217,TP218,TP219,TP220,TP221,TP254,TP255,TP256,TP301,TP302,TP415,TP416,TP419,TP421,TP423,TP424,TP425,TP426,TP427,TP501,TP607,TP650,TP1001	DNP	TESTPOINT
6	Hardware, Nut, 2-56, SS, Small	2CSHNS	Olander				

CONNECTORS				
QTY	REFDES	MANUFACTURE PN	MANUFACTURE	DESCRIPTION
2	J1,J2	901-144-8RFX	Amphenol-RF Division	Connector, SMA, Straight
2	J101,J102	EW-32-11-G-D-400	Samtec	Connector, Through Hole, Male
1	J103	EW-25-11-G-D-400	Samtec	Connector, Through Hole, Male
3	J104,J105,J106	71439-2164	Molex	Connector, PCI Mezzanine, Main Board
1	J204	22-12-2024	Molex	Header, Right Angle, 2 pin
1	P101	745783-4	AMP	Connector, DB25, Female
1	P103	569564-1	AMP	Connector, RJ45, Thru-Hole
2	P104,P105	MD-60SM	CUI Inc	Connector, MiniDIN6, Shielded, P/S2
2	P106,P107	747250-4	AMP	Connector, DB9, Male
1	P108	53462-0611	Molex	Connector, IEEE-1394A
1	P109	67089-1	AMP	Connector, Mictor, Edge Launch, 38 pin
1	P110	71240-340CA	FCI	Connector, Assembly, Dual PCMCIA with Left side eject
2	P110a, P110b	73277-101000	FCI	Connector, PCMCIA SMT Connector
2	P111,P112	1364532-1	AMP	Connector, HSSDC2, SMD
1	P113	N7E50-7516HG-50	3M	Connector, Compact Flash, SMD
1	P113a	7E50-9316-04	3M	Ejector, Compact Flash
1	P114	PZC08DBAN	Sullins Electric	Header, 2x8, 100mil, right angle
1	P115	87333-1420	Molex	Header, 2X7, 2mm
3	P116,P117,P118	35RASMT4BHNTR	Switchcraft	Connector, Stereo Phone Jack
2	P119,P120	67490-9221	Molex	Connector, Serial ATA, SMD
3	TP1,TP2,TP3	10-109-3-1	Concord Electronics	Testpoint, Turret
2	X102a, X104a	1108800	Aries	Socket, 8 pin DIP

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```

NET_CLASS PCI_FPGA_CONN
{
NET PCI_FPGA_AD06
NET PCI_FPGA_AD04
NET PCI_FPGA_AD03
NET PCI_FPGA_AD01
NET PCI_FPGA_AD07
NET PCI_FPGA_CBE0
NET PCI_FPGA_AD05
NET PCI_FPGA_M66EN
NET PCI_FPGA_AD11
NET PCI_FPGA_AD12
NET PCI_FPGA_AD08
NET PCI_FPGA_AD13
NET PCI_FPGA_AD14
NET PCI_FPGA_AD15
NET PCI_FPGA_AD10
NET PCI_FPGA_AD19
NET PCI_FPGA_CBE2
NET PCI_FPGA_AD16
NET PCI_FPGA_AD17
NET PCI_FPGA_AD20
NET PCI_FPGA_AD21
NET PCI_FPGA_AD22
NET PCI_FPGA_AD18
NET PCI_FPGA_AD31
NET PCI_FPGA_AD26
NET PCI_FPGA_AD27
NET PCI_FPGA_AD28
NET PCI_FPGA_PMC_GNT
NET PCI_FPGA_PMC_REQ
NET PCI_FPGA_AD29
NET PCI_FPGA_AD30
NET PCI_FPGA_PRS2
NET PCI_FPGA_BM3
NET PCI_FPGA_BUS_RST
NET PCI_FPGA_BM4
NET PCI_FPGA_AD24
NET PCI_FPGA_AD25
NET PCI_FPGA_AD23
NET PCI_FPGA_CBE3
NET PCI_FPGA_INTC
NET PCI_FPGA_INTB
NET PCI_FPGA_PRS1
NET PCI_FPGA_INTD
NET PCI_FPGA_SBO
NET PCI_FPGA_SDONE
NET PCI_FPGA_CBE1
NET PCI_FPGA_PAR
NET PCI_FPGA_CB_GNT
NET PCI_FPGA_CB_REQ
NET PCI_FPGA_GBL_RST
NET PCI_FPGA_PMC_TRST
NET PCI_FPGA_PMC_TCK
NET PCI_FPGA_PMC_TDO
NET PCI_FPGA_PMC_TDI
NET PCI_FPGA_INTA
NET PCI_FPGA_PMC_TMS
NET PCI_FPGA_AD02
NET PCI_FPGA_ACK64
NET PCI_FPGA_AD00
NET PCI_FPGA_REQ64
NET PCI_FPGA_DEVSEL
NET PCI_FPGA_PERR
NET PCI_FPGA_LOCK
NET PCI_FPGA_SERR
NET PCI_FPGA_FRAME
NET PCI_FPGA_TRDY
NET PCI_FPGA_IRDY
NET PCI_FPGA_STOP
}
NET_CLASS CLK_27MHZ_COMP
{
NET FPGA_PMC_CONN4_IO61
NET PCI_PORT_CLK_PMC
NET PCI_PORT_CLK_CB
}
NET_CLASS CLK_27MHZ_FPGA
{
NET PCI_PORT_CLK_PMC
NET PCI_PORT_CLK_CB
}

```

```

NET_CLASS PCI_PORT_CONN
{
NET PCI_PORT_AD06
NET PCI_PORT_AD04
NET PCI_PORT_AD03
NET PCI_PORT_AD01
NET PCI_PORT_AD07
NET PCI_PORT_CBE0
NET PCI_PORT_AD05
NET PCI_PORT_M66EN
NET PCI_PORT_AD11
NET PCI_PORT_AD12
NET PCI_PORT_AD08
NET PCI_PORT_AD13
NET PCI_PORT_AD14
NET PCI_PORT_AD15
NET PCI_PORT_AD10
NET PCI_PORT_AD19
NET PCI_PORT_CBE2
NET PCI_PORT_AD16
NET PCI_PORT_AD17
NET PCI_PORT_AD20
NET PCI_PORT_AD21
NET PCI_PORT_AD22
NET PCI_PORT_AD18
NET PCI_PORT_AD31
NET PCI_PORT_AD26
NET PCI_PORT_AD27
NET PCI_PORT_AD28
NET PCI_PORT_PMC_GNT
NET PCI_PORT_PMC_REQ
NET PCI_PORT_AD29
NET PCI_PORT_AD30
NET PCI_PORT_PRS2
NET PCI_PORT_BM3
NET PCI_PORT_BUS_RST
NET PCI_PORT_BM4
NET PCI_PORT_AD24
NET PCI_PORT_AD25
NET PCI_PORT_AD23
NET PCI_PORT_CBE3
NET PCI_PORT_INTC
NET PCI_PORT_INTB
NET PCI_PORT_PRS1
NET PCI_PORT_INTD
NET PCI_PORT_SBO
NET PCI_PORT_SDONE
NET PCI_PORT_CBE1
NET PCI_PORT_PAR
NET PCI_PORT_CB_GNT
NET PCI_PORT_CB_REQ
NET PCI_PORT_GBL_RST
NET PCI_PORT_PMC_TRST
NET PCI_PORT_PMC_TCK
NET PCI_PORT_PMC_TDO
NET PCI_PORT_PMC_TDI
NET PCI_PORT_INTA
NET PCI_PORT_PMC_TMS
NET PCI_PORT_AD02
NET PCI_PORT_ACK64
NET PCI_PORT_AD00
NET PCI_PORT_REQ64
NET PCI_PORT_DEVSEL
NET PCI_PORT_PERR
NET PCI_PORT_LOCK
NET PCI_PORT_SERR
NET PCI_PORT_FRAME
NET PCI_PORT_TRDY
NET PCI_PORT_IRDY
NET PCI_PORT_STOP
}
NET_CLASS ENET_PHY_COMP
{
NET PHY_TX_ER_TMP
NET PHY_TX_CLK_TMP
NET PHY_COL_TMP
NET PHY_CRS_TMP
NET PHY_RXD3_TMP
NET PHY_RXD2_TMP
NET PHY_RXD1_TMP
NET PHY_RXD0_TMP
NET PHY_RX_DV_TMP
NET PHY_RX_CLK_TMP
NET PHY_RX_ER_TMP
}

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NET_CLASS ENET_PHY
{
NET PHY_RXD3
NET PHY_RXD2
NET PHY_RXD1
NET PHY_RXD0
NET PHY_RX_DV
NET PHY_RX_CLK
NET PHY_RX_ER
NET PHY_SLEEP
NET PHY_PAUSE
NET PHY_PWRDN
NET PHY_MDIO
NET PHY_MDC
NET PHY_COL
NET PHY_CRS
NET PHY_MDINT
NET PHY_RESET
NET PHY_SLW0
NET PHY_SLW1
NET PHY_TX_ER
NET PHY_TX_CLK
NET PHY_TX_ER
NET PHY_TXD0
NET PHY_TXD1
NET PHY_TXD2
NET PHY_TXD3
}
NET_CLASS PMC_PMC_CONN4
{
NET PMC_CONN4_IO21
NET PMC_CONN4_IO19
NET PMC_CONN4_IO17
NET PMC_CONN4_IO15
NET PMC_CONN4_IO22
NET PMC_CONN4_IO20
NET PMC_CONN4_IO18
NET PMC_CONN4_IO16
NET PMC_CONN4_IO29
NET PMC_CONN4_IO27
NET PMC_CONN4_IO25
NET PMC_CONN4_IO23
NET PMC_CONN4_IO30
NET PMC_CONN4_IO28
NET PMC_CONN4_IO26
NET PMC_CONN4_IO24
NET PMC_CONN4_IO37
NET PMC_CONN4_IO35
NET PMC_CONN4_IO33
NET PMC_CONN4_IO31
NET PMC_CONN4_IO38
NET PMC_CONN4_IO36
NET PMC_CONN4_IO34
NET PMC_CONN4_IO32
NET PMC_CONN4_IO45
NET PMC_CONN4_IO43
NET PMC_CONN4_IO41
NET PMC_CONN4_IO39
NET PMC_CONN4_IO46
NET PMC_CONN4_IO44
NET PMC_CONN4_IO42
NET PMC_CONN4_IO40
NET PMC_CONN4_IO53
NET PMC_CONN4_IO51
NET PMC_CONN4_IO49
NET PMC_CONN4_IO47
NET PMC_CONN4_IO54
NET PMC_CONN4_IO52
NET PMC_CONN4_IO50
NET PMC_CONN4_IO48
NET PMC_CONN4_IO61
NET PMC_CONN4_IO59
NET PMC_CONN4_IO57
NET PMC_CONN4_IO55
NET PMC_CONN4_IO62
NET PMC_CONN4_IO60
NET PMC_CONN4_IO58
NET PMC_CONN4_IO56
NET PMC_CONN4_IO14
NET PMC_CONN4_IO12
NET PMC_CONN4_IO10
NET FPGA_PMC_CONN4_IO13
NET PMC_CONN4_IO11
NET PMC_CONN4_IO9
}

```

```

NET_CLASS PS2_1
{
NET PS2_1_DATA_OUT
NET PS2_1_DATA_IN
NET PS2_1_CLK_OUT
NET PS2_1_CLK_IN
}
NET_CLASS PS2_2
{
NET PS2_2_DATA_OUT
NET PS2_2_DATA_IN
NET PS2_2_CLK_OUT
NET PS2_2_CLK_IN
}
NET_CLASS SYSACE_FLASH
{
NET SYSACE_CFA05
NET SYSACE_CFA04
NET SYSACE_CFA03
NET SYSACE_CFA02
NET SYSACE_CFA01
NET SYSACE_CFA00
NET SYSACE_CFA10
NET SYSACE_CFA09
NET SYSACE_CFA08
NET SYSACE_CFA07
NET SYSACE_CFA06
NET SYSACE_CFD04
NET SYSACE_CFD03
NET SYSACE_CFD02
NET SYSACE_CFD01
NET SYSACE_CFD00
NET SYSACE_CFD09
NET SYSACE_CFD08
NET SYSACE_CFD07
NET SYSACE_CFD06
NET SYSACE_CFD05
NET SYSACE_CFD15
NET SYSACE_CFD14
NET SYSACE_CFD13
NET SYSACE_CFD12
NET SYSACE_CFD11
NET SYSACE_CFD10
NET SYSACE_CFCDD1
NET SYSACE_CFCDD2
NET SYSACE_CFCDD3
NET SYSACE_CFWAIT
NET SYSACE_CFRBDSY
NET SYSACE_CFRWE
NET SYSACE_CFDE
}
NET_CLASS SYSACE_MPU
{
NET SYSACE_MPA03
NET SYSACE_MPA02
NET SYSACE_MPA01
NET SYSACE_MPA00
NET SYSACE_MPA06
NET SYSACE_MPA05
NET SYSACE_MPA04
NET SYSACE_MPD04
NET SYSACE_MPD03
NET SYSACE_MPD02
NET SYSACE_MPD01
NET SYSACE_MPD00
NET SYSACE_MPD09
NET SYSACE_MPD08
NET SYSACE_MPD07
NET SYSACE_MPD06
NET SYSACE_MPD05
NET SYSACE_MPD15
NET SYSACE_MPD14
NET SYSACE_MPD13
NET SYSACE_MPD12
NET SYSACE_MPD11
NET SYSACE_MPD10
NET SYSACE_MPBRDY
NET SYSACE_MPIRQ
NET SYSACE_MPCE
NET SYSACE_MPWE
NET SYSACE_MPDE
}

```

```

NET_CLASS SYSACE_JTAG_2V5
{
NET SYSACE_TSTTDO
NET SYSACE_TSTTMS_2V5
NET SYSACE_TSTTCK_2V5
NET SYSACE_TSTTDDI_2V5
}
NET_CLASS SYSACE_JTAG_3V3
{
NET SYSACE_TSTTMS_3V3
NET SYSACE_TSTTCK_3V3
NET SYSACE_TSTTDDI_3V3
}
NET_CLASS TFT_CNTRL_FPGA
{
NET TFT_FPGA_DPS
NET TFT_FPGA_DE
NET TFT_FPGA_VSYNC
NET TFT_FPGA_HSYNC
NET TFT_FPGA_CLK
}
NET_CLASS TFT_CLR_FPGA
{
NET TFT_FPGA_B5
NET TFT_FPGA_B4
NET TFT_FPGA_B3
NET TFT_FPGA_B2
NET TFT_FPGA_B1
NET TFT_FPGA_B0
NET TFT_FPGA_G5
NET TFT_FPGA_G4
NET TFT_FPGA_G3
NET TFT_FPGA_G2
NET TFT_FPGA_G1
NET TFT_FPGA_G0
NET TFT_FPGA_R5
NET TFT_FPGA_R4
NET TFT_FPGA_R3
NET TFT_FPGA_R2
NET TFT_FPGA_R1
NET TFT_FPGA_R0
}
NET_CLASS TFT_CNTRL_LCD
{
NET TFT_LCD_DPS
NET TFT_LCD_DE
NET TFT_LCD_VSYNC
NET TFT_LCD_HSYNC
NET TFT_LCD_CLK
}
NET_CLASS TFT_CLR_LCD
{
NET TFT_LCD_B5
NET TFT_LCD_B4
NET TFT_LCD_B3
NET TFT_LCD_B2
NET TFT_LCD_B1
NET TFT_LCD_B0
NET TFT_LCD_G5
NET TFT_LCD_G4
NET TFT_LCD_G3
NET TFT_LCD_G2
NET TFT_LCD_G1
NET TFT_LCD_G0
NET TFT_LCD_R5
NET TFT_LCD_R4
NET TFT_LCD_R3
NET TFT_LCD_R2
NET TFT_LCD_R1
NET TFT_LCD_R0
}
NET_CLASS CPU_TRACE
{
NET TS6
NET TS5
NET TS4
NET TS3
NET TS2E
NET TS1E
NET TS20
NET TS10
NET TRC_CLK
}

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PCB: 1280285  
ASM: 0431182  
SCH: 0381135

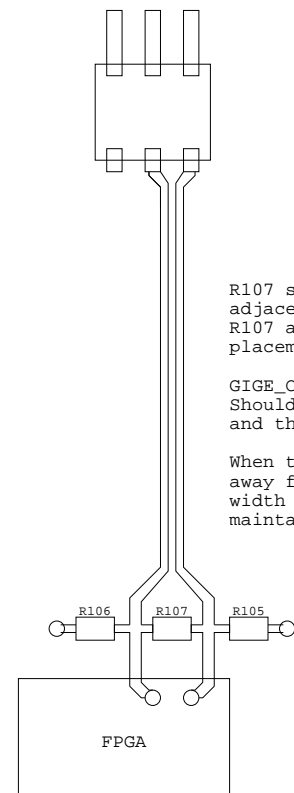
Title: ML300\_CPU  
Net Classes  
Page 2 of 2

# ML300 CPU - Net Classes

## Page 2 of 2

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 11 of 55	Drawn By BP

V2P7\_BANK0  
FF672  
(DIE DOWN)

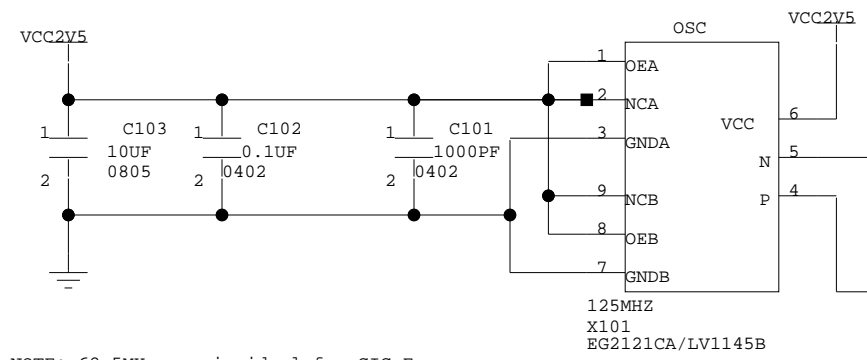


R107 should be Placed immediately adjacent to the FPGA. R105 and R107 are for DC Current, so placement is not critical.

GIGE\_CLK\_P and GIGE\_CLK\_N Should be routed differentially, and their trancelengths matched.

When the traces need to deviate away from eachother, the trace width should be modified, to maintain a controlled impedance.

C101, C102 and C103 should be Placed immediately adjacent to X101



NOTE: 62.5MHz osc is ideal for GIG-E  
125MHz osc must divide by 2 internally

Total trancelength GIGE\_CLK\_P = GIGE\_CLK\_N  
These Traces are should be routed as 100 Ohm differential signals.

FPGA\_GPIO\_[00:31]

Ethernet Phy

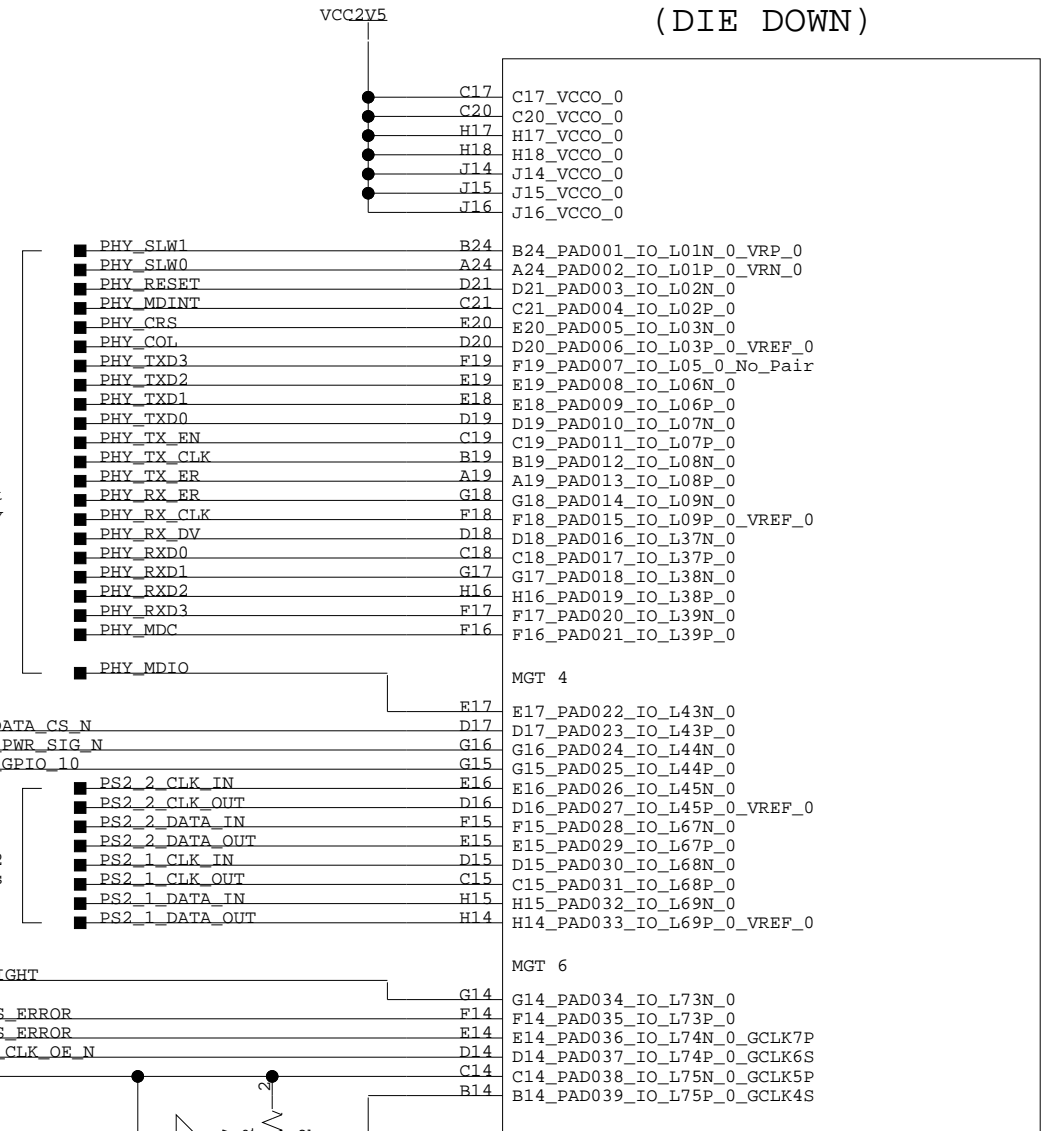
PS/2 Ports

PLB and OPB Bus Error

These resistor should be placed close to the FPGA

Matched Trace Lengths  
Differential Pair

These resistor provide for LVPECL to LVDS Conversion, so use for the ED2121 CA OSC. DNP when using the LV1145B, as is an LVDS differential oscillator, and doesn't need.



U1  
DEVICE=XC2VP7-6FF672C  
PKG\_TYPE=FF672  
PARTS=1  
LEVEL=STD

# Test Clock using LineSim

## ML300 CPU - V2P7 Bank 0 PS/2, Ethernet



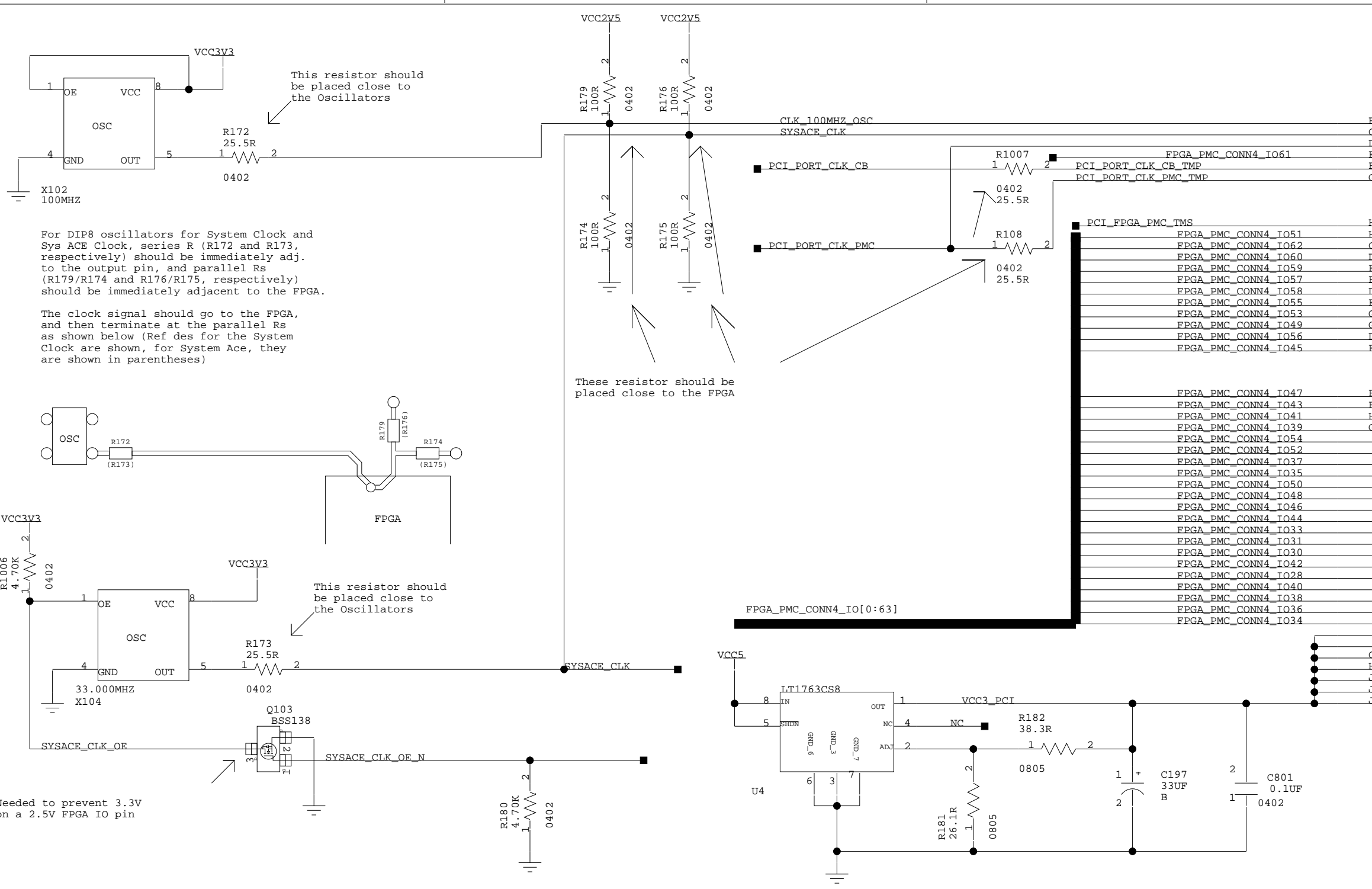
PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU	
2VP7 Bank 0 Ethernet and PS/2	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 12 of 55	Drawn By BP

V2P7\_BANK1  
FF672  
(DIE DOWN)

B13	FPGA_PMC_CONN4_IO61	H13	FPGA_PMC_CONN4_IO47	F11
C13	FPGA_PMC_CONN4_IO62	H12	FPGA_PMC_CONN4_IO43	F10
D13	FPGA_PMC_CONN4_IO60	C12	FPGA_PMC_CONN4_IO41	H11
E13	FPGA_PMC_CONN4_IO59	D12	FPGA_PMC_CONN4_IO39	G10
F13	FPGA_PMC_CONN4_IO57	E12	FPGA_PMC_CONN4_IO54	C9
G13	FPGA_PMC_CONN4_IO58	F12	FPGA_PMC_CONN4_IO52	D9
	FPGA_PMC_CONN4_IO55	D11	FPGA_PMC_CONN4_IO37	E9
	FPGA_PMC_CONN4_IO53	E11	FPGA_PMC_CONN4_IO35	G9
	FPGA_PMC_CONN4_IO49	G12	FPGA_PMC_CONN4_IO50	A8
	FPGA_PMC_CONN4_IO56	G11	FPGA_PMC_CONN4_IO48	B8
	FPGA_PMC_CONN4_IO45	D10	FPGA_PMC_CONN4_IO46	C8
		E10	FPGA_PMC_CONN4_IO44	D8
			FPGA_PMC_CONN4_IO33	E9
			FPGA_PMC_CONN4_IO31	E8
			FPGA_PMC_CONN4_IO30	F8
			FPGA_PMC_CONN4_IO42	D7
			FPGA_PMC_CONN4_IO28	E7
			FPGA_PMC_CONN4_IO40	C6
			FPGA_PMC_CONN4_IO38	D6
			FPGA_PMC_CONN4_IO36	A3
			FPGA_PMC_CONN4_IO34	B3
				C7
				H9
				C10
				H10
				J11
				J12
				J13
				C7_VCCO_1
				H9_VCCO_1
				C10_VCCO_1
				H10_VCCO_1
				J11_VCCO_1
				J12_VCCO_1
				J13_VCCO_1

U1  
DEVICE=XC2VP7-6FF672C  
PKG\_TYPE=FF672  
PARTS=1  
LEVEL=STD



This resistor should be placed close to the Oscillators

These resistor should be placed close to the FPGA

This resistor should be placed close to the Oscillators

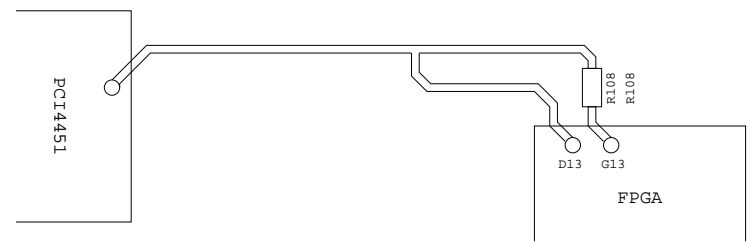
VCC3\_PCI is a power line so should be thick or a plane

Needed to prevent 3.3V on a 2.5V FPGA IO pin

The Clock line to the Cardbus PCI4451 (R108) and the PMC Connectors (R1007) should have their Series Rs immediately adjacent to the FPGA.

The Feedbackpath for Cardbus (to D13) should go half way to the PCI4451, before coming back to the FPGA. The length to the PCI4451 should equal the feedback loop.

The Cardbus layout is shown below.



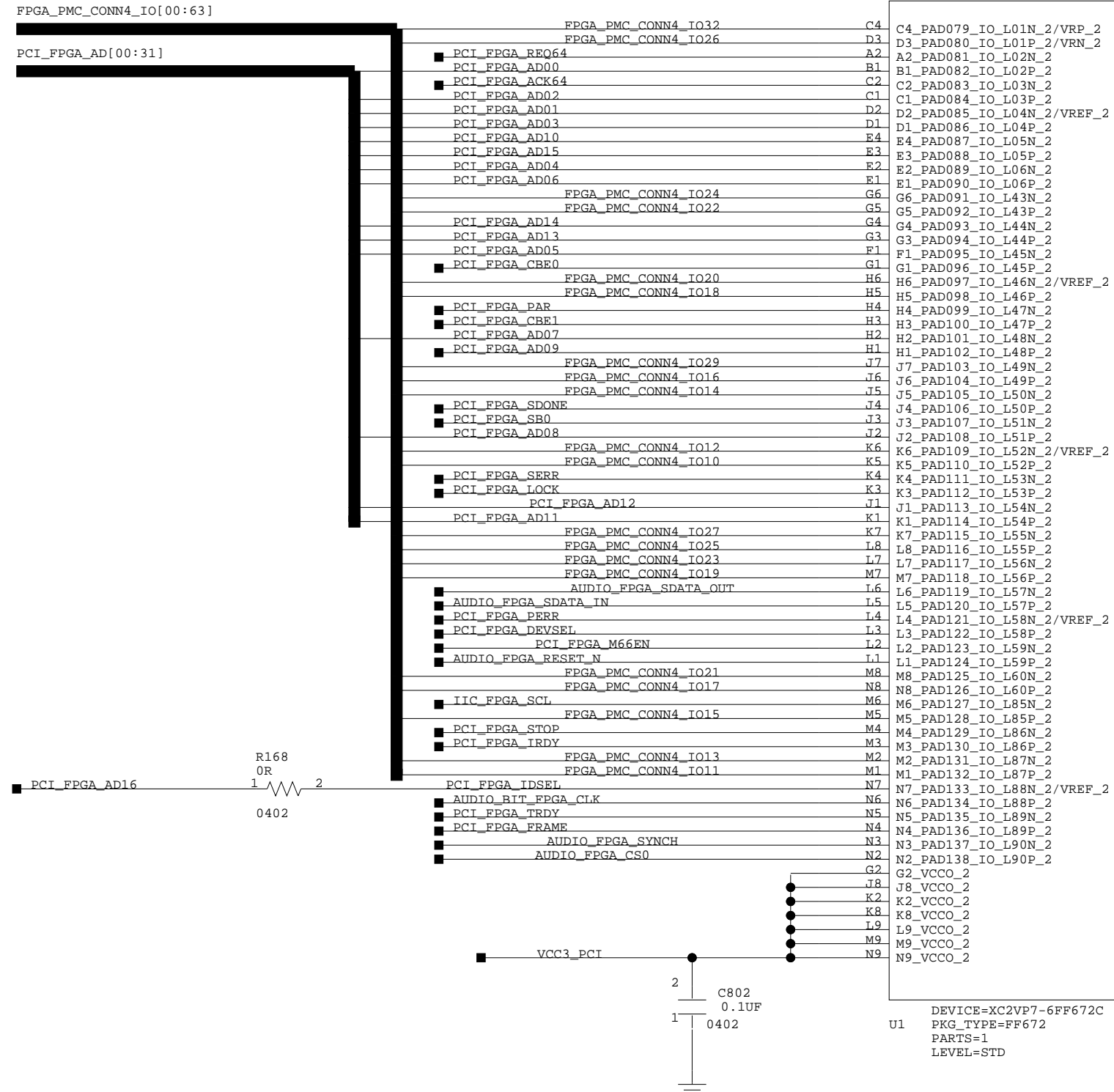
ML300 CPU - V2P7 Bank 1  
PMC General Purpose IO



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU	
2VP7 Bank 1 PMC General Purpose IO	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 13 of 55	Drawn By BP

V2P7\_BANK2  
FF672  
(DIE DOWN)



U1 DEVICE=XC2VP7-6FF672C  
PKG\_TYPE=FF672  
PARTS=1  
LEVEL=STD



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300\_CPU  
2VP7 Bank 2  
PMC GPIO and PCI

ML300 CPU - V2P7 Bank 2  
PMC GPIO and PCI

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 14 of 55	Drawn By BP

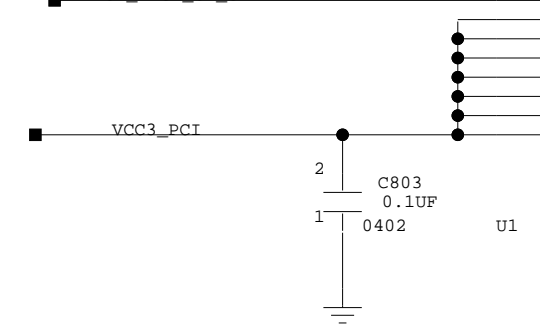
V2P7\_BANK3  
FF672  
(DIE DOWN)

PCI\_FPGA\_AD[00:31]  
FPGA\_GPIO\_[00:31]

IIC_FPGA_SDA	P2	P2_PAD139_IO_L90N_3
FPGA_CPU_RESET	P3	P3_PAD140_IO_L90P_3
PCI_FPGA_AD30	P4	P4_PAD141_IO_L89N_3
PCI_FPGA_AD29	P5	P5_PAD142_IO_L89P_3
FPGA_PMC_CONN4_IO9	P6	P6_PAD143_IO_L88N_3
FPGA_GPIO_01	P7	P7_PAD144_IO_L88P_3
PCI_FPGA_AD17	R1	R1_PAD145_IO_L87N_3/VREF_3
PCI_FPGA_AD16	R2	R2_PAD146_IO_L87P_3
PCI_FPGA_PMC_REQ	R3	R3_PAD147_IO_L86N_3
PCI_FPGA_PMC_GNT	R4	R4_PAD148_IO_L86P_3
FPGA_GPIO_02	R5	R5_PAD149_IO_L85N_3
FPGA_GPIO_03	R6	R6_PAD150_IO_L85P_3
FPGA_GPIO_04	P8	P8_PAD151_IO_L60N_3
FPGA_GPIO_05	R8	R8_PAD152_IO_L60P_3
PCI_FPGA_CBE2	T1	T1_PAD153_IO_L59N_3
PCI_FPGA_AD19	T2	T2_PAD154_IO_L59P_3
PCI_FPGA_BM4	T3	T3_PAD155_IO_L58N_3
PCI_FPGA_BUS_RST	T4	T4_PAD156_IO_L58P_3
FPGA_GPIO_06	T5	T5_PAD157_IO_L57N_3/VREF_3
FPGA_GPIO_07	T6	T6_PAD158_IO_L57P_3
FPGA_GPIO_08	R7	R7_PAD159_IO_L56N_3
FPGA_GPIO_09	T7	T7_PAD160_IO_L56P_3
FPGA_GPIO_00	T8	T8_PAD161_IO_L55N_3
TOUCH_CS_N	U7	U7_PAD162_IO_L55P_3
PCI_FPGA_AD18	U1	U1_PAD163_IO_L54N_3
PCI_FPGA_AD22	V1	V1_PAD164_IO_L54P_3
PCI_FPGA_BM3	U3	U3_PAD165_IO_L53N_3
PCI_FPGA_PRS2	U4	U4_PAD166_IO_L53P_3
TOUCH_IRQ_N	U5	U5_PAD167_IO_L52N_3
TOUCH_DOUT	U6	U6_PAD168_IO_L52P_3
PCI_FPGA_AD21	V2	V2_PAD169_IO_L51N_3/VREF_3
PCI_FPGA_INTD	V3	V3_PAD170_IO_L51P_3
PCI_FPGA_PRS1	V4	V4_PAD171_IO_L50N_3
TOUCH_BUSY	V5	V5_PAD172_IO_L50P_3
TOUCH_DIN	V6	V6_PAD173_IO_L49N_3
IIC_FPGA_IRQ	V7	V7_PAD174_IO_L49P_3
PCI_FPGA_AD20	W1	W1_PAD175_IO_L48N_3
PCI_FPGA_CBE3	W2	W2_PAD176_IO_L48P_3
PCI_FPGA_INTB	W3	W3_PAD177_IO_L47N_3
PCI_FPGA_INTC	W4	W4_PAD178_IO_L47P_3
TOUCH_DCLK	W5	W5_PAD179_IO_L46N_3
IIC_CRIT_A	W6	W6_PAD180_IO_L46P_3
PCI_FPGA_AD23	Y1	Y1_PAD181_IO_L45N_3/VREF_3
PCI_FPGA_AD25	AA1	AA1_PAD182_IO_L45P_3
IIC_FPGA_WP	Y3	Y3_PAD183_IO_L44N_3
PCI_FPGA_INTA	Y4	Y4_PAD184_IO_L44P_3
PCI_FPGA_CB_SUSPEND	Y5	Y5_PAD185_IO_L43N_3
PCI_FPGA_CB_IRQSER	Y6	Y6_PAD186_IO_L43P_3
PCI_FPGA_PMC_TDI	AB3	AB3_PAD187_IO_L06N_3
PCI_FPGA_PMC_TDO	AB4	AB4_PAD188_IO_L06P_3
PCI_FPGA_AD24	AC1	AC1_PAD189_IO_L05N_3
PCI_FPGA_AD28	AC2	AC2_PAD190_IO_L05P_3
PCI_FPGA_AD27	AD1	AD1_PAD191_IO_L04N_3
PCI_FPGA_AD26	AD2	AD2_PAD192_IO_L04P_3
PCI_FPGA_AD31	AE1	AE1_PAD193_IO_L03N_3/VREF_3
PCI_FPGA_PMC_TCK	AF2	AF2_PAD194_IO_L03P_3
PCI_FPGA_GBL_RST	AC3	AC3_PAD195_IO_L02N_3
PCI_FPGA_PMC_TRST	AD4	AD4_PAD196_IO_L02P_3
PCI_FPGA_CB_REQ	AE3	AE3_PAD197_IO_L01N_3/VRP_3
PCI_FPGA_CB_GNT	AF3	AF3_PAD198_IO_L01P_3/VRN_3
	P9	P9_VCCO_3
	R9	R9_VCCO_3
	T9	T9_VCCO_3
	U2	U2_VCCO_3
	U8	U8_VCCO_3
	V8	V8_VCCO_3
	Y2	Y2_VCCO_3

Touchscreen

The Touchscreen is on the ML300\_PWR\_IO board,  
and the connection is shown on page 55.



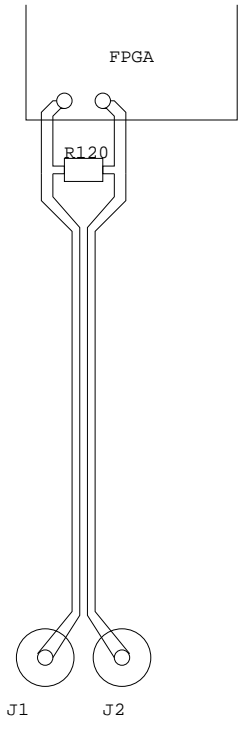
DEVICE=XC2VP7-6FF672C  
PKG\_TYPE=FF672  
PARTS=1  
LEVEL=STD



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

ML300 CPU - V2P7 Bank 3  
IIC, Audio, PMC GPIO,  
PCI and TouchScrn

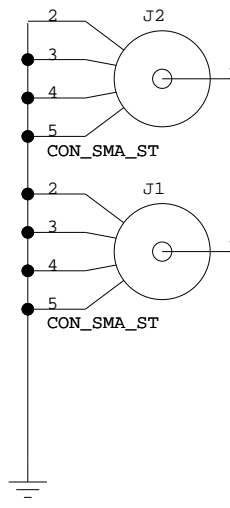
Title: ML300_CPU 2VP7 Bank 3 IIC, Audio, PCI and Touch	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 15 of 55	Drawn By BP



R120 should be placed immediately adjacent to the FPGA

USER\_MGT\_CLK\_P and USER\_MGT\_CLK\_N Should be routed differentially, and their tracelengths matched.

When the traces need to deviate away from each other, the trace width should be modified, to maintain a controlled impedance.



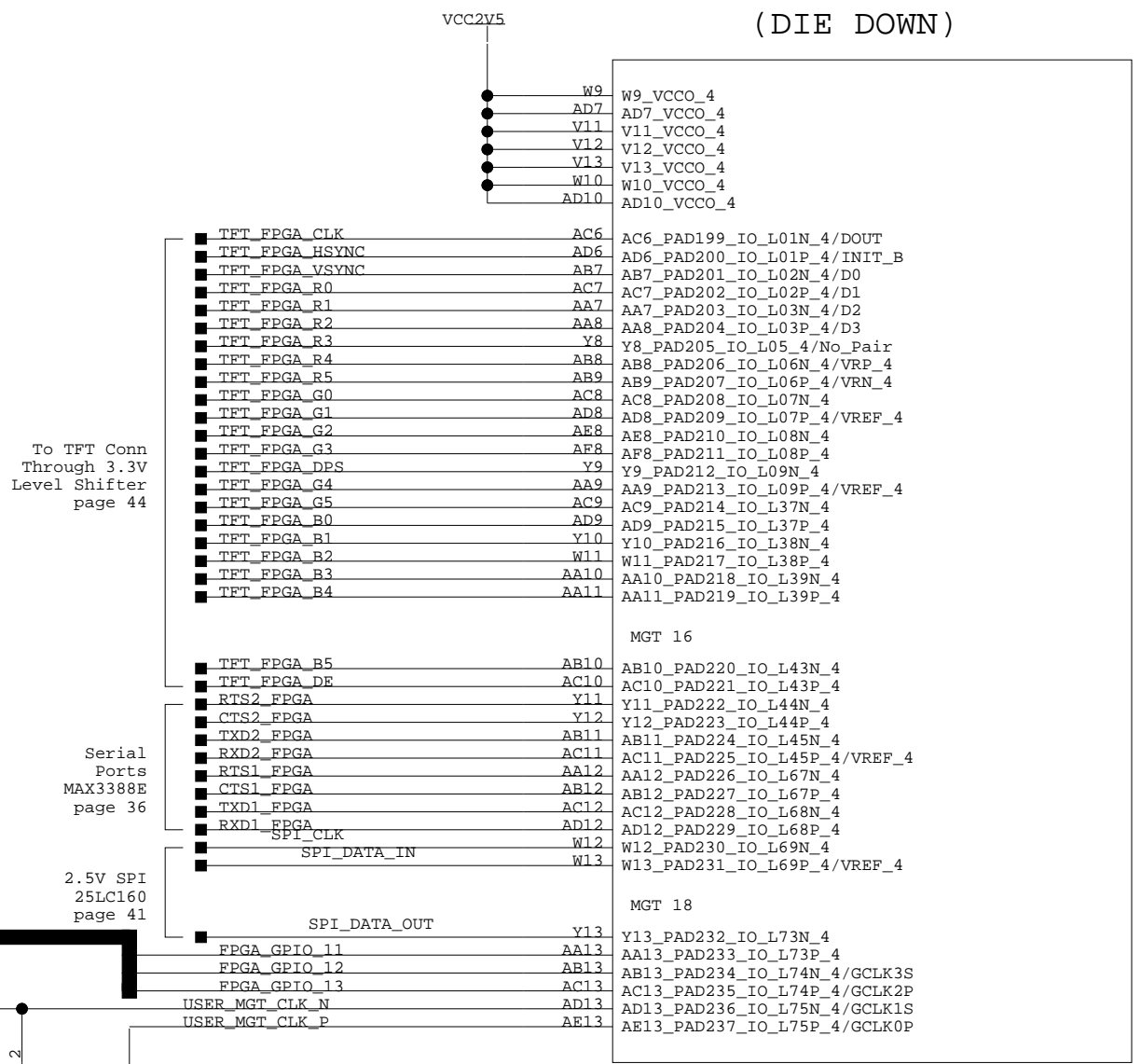
Matched Trace Lengths

This resistor should be placed close to the FPGA  
See figure above.

Total tracelength GIGE\_CLK\_LVPCL\_P + GIGE\_CLK\_P = GIGE\_CLK\_LVPCL\_N + GIGE\_CLK\_N

These Traces are should be routed as 100 Ohm differential signals, 8mil track, 10mil spacing

V2P7\_BANK4  
FF672  
(DIE DOWN)



To TFT Conn  
Through 3.3V  
Level Shifter  
page 44

Serial  
Ports  
MAX3388E  
page 36

2.5V SPI  
25LC160  
page 41

U1  
DEVICE=XC2VP7-6FF672C  
PKG\_TYPE=FF672  
PARTS=1  
LEVEL=STD

ML300 CPU - V2P7 Bank 4  
TFT LCD, Serial, SPI

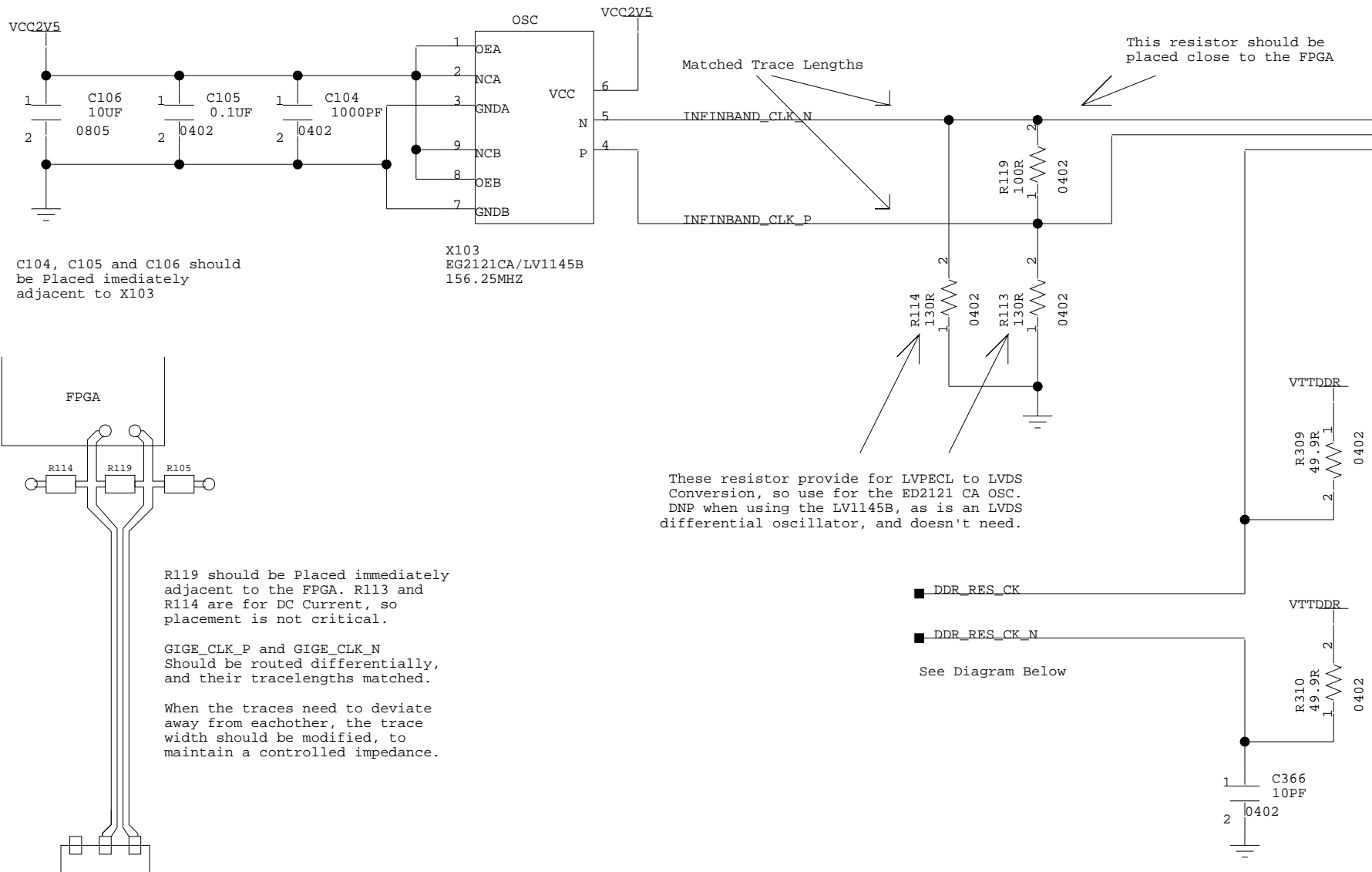


PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU	
2VP7 Bank 4 TFT LCD, Serial and SPI	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 16 of 55	Drawn By BP

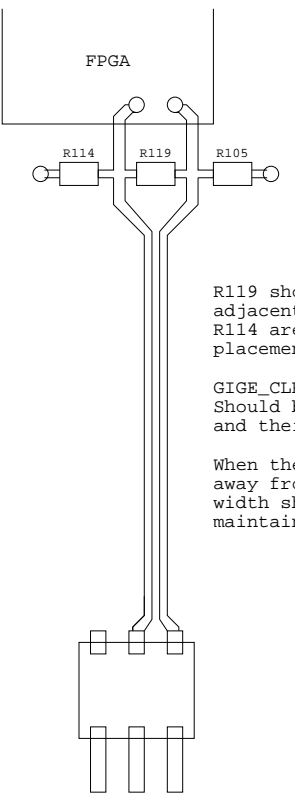


V2P7\_BANK5  
FF672  
(DIE DOWN)



C104, C105 and C106 should be Placed immediately adjacent to X103

X103  
EG2121CA/LV1145B  
156.25MHZ



R119 should be Placed immediately adjacent to the FPGA. R113 and R114 are for DC Current, so placement is not critical.

GIGE\_CLK\_P and GIGE\_CLK\_N Should be routed differentially, and their trancelengths matched.

When the traces need to deviate away from eachother, the trace width should be modified, to maintain a controlled impedance.

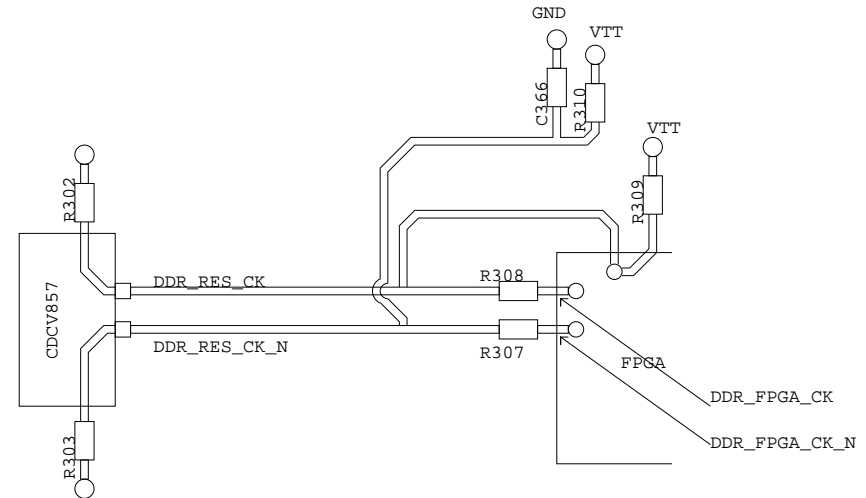
These resistor provide for LVPECL to LVDS Conversion, so use for the ED2121 CA OSC. DNP when using the LV1145B, as is an LVDS differential oscillator, and doesn't need.

DDR\_RES CK  
DDR\_RES CK\_N  
See Diagram Below

- FPGA\_GPIO\_14
- FPGA\_GPIO\_15
- SYSACE\_MPDE
- SYSACE\_MPWE
- SYSACE\_MPA00
- SYSACE\_MPA01
- SYSACE\_MPA02
- SYSACE\_MPA03
- SYSACE\_MPD00
- SYSACE\_MPD01
- SYSACE\_MPD02
- SYSACE\_MPD03
- SYSACE\_MPD04
- SYSACE\_MPD05
- SYSACE\_MPD06
- SYSACE\_MPD07
- SYSACE\_MPD08
- SYSACE\_MPD09
- SYSACE\_MPD10
- SYSACE\_MPD11
- SYSACE\_MPD12
- SYSACE\_MPD13
- SYSACE\_MPD14
- SYSACE\_MPD15
- SYSACE\_MPA04
- SYSACE\_MPA05
- SYSACE\_MPA06
- SYSACE\_MPCE
- SYSACE\_MPIRQ
- SYSACE\_MPBRDY
- CPU\_TDO\_TMP
- CPU\_TDI
- CPU\_TCK
- CPU\_TMS
- CPU\_HALT\_N
- CPU\_TRST

AE14	AE14_PAD238_IO_L75N_5/GCLK7S
AD14	AD14_PAD239_IO_L75P_5/GCLK6P
AC14	AC14_PAD240_IO_L74N_5/GCLK5S
AB14	AB14_PAD241_IO_L74P_5/GCLK4P
AA14	AA14_PAD242_IO_L73N_5
Y14	Y14_PAD243_IO_L73P_5
MGT 19	
W14	W14_PAD244_IO_L69N_5/VREF_5
W15	W15_PAD245_IO_L69P_5
AD15	AD15_PAD246_IO_L68N_5
AC15	AC15_PAD247_IO_L68P_5
AB15	AB15_PAD248_IO_L67N_5
AA15	AA15_PAD249_IO_L67P_5
AC16	AC16_PAD250_IO_L45N_5/VREF_5
AB16	AB16_PAD251_IO_L45P_5
Y15	Y15_PAD252_IO_L44N_5
Y16	Y16_PAD253_IO_L44P_5
AC17	AC17_PAD254_IO_L43N_5
AB17	AB17_PAD255_IO_L43P_5
MGT 21	
AA16	AA16_PAD256_IO_L39N_5
AA17	AA17_PAD257_IO_L39P_5
W16	W16_PAD258_IO_L38N_5
Y17	Y17_PAD259_IO_L38P_5
AD18	AD18_PAD260_IO_L37N_5
AC18	AC18_PAD261_IO_L37P_5
AA18	AA18_PAD262_IO_L09N_5/VREF_5
Y18	Y18_PAD263_IO_L09P_5
AF19	AF19_PAD264_IO_L08N_5
AE19	AE19_PAD265_IO_L08P_5
AD19	AD19_PAD266_IO_L07N_5/VREF_5
AC19	AC19_PAD267_IO_L07P_5
AB18	AB18_PAD268_IO_L06N_5/VRP_5
AB19	AB19_PAD269_IO_L06P_5/VRN_5
Y19	Y19_PAD270_IO_L05_5/No_Pair
AA19	AA19_PAD271_IO_L03N_5/D4
AA20	AA20_PAD272_IO_L03P_5/D5
AC20	AC20_PAD273_IO_L02N_5/D6
AB20	AB20_PAD274_IO_L02P_5/D7
AD21	AD21_PAD275_IO_L01N_5/RDWR_B
AC21	AC21_PAD276_IO_L01P_5/CS_B
V14	V14_VCCO_5
V15	V15_VCCO_5
V16	V16_VCCO_5
W17	W17_VCCO_5
W18	W18_VCCO_5
AD17	AD17_VCCO_5
AD20	AD20_VCCO_5

U1  
DEVICE=XC2VP7-6FF672C  
PKG\_TYPE=FF672  
PARTS=1  
LEVEL=STD



The Clock traces to the DDR PLL (CDCV857) must be matched trancelength. The Length of the feedback loop (i.e. length from FPGA back to FPGA) for the DDR\_XXX CK net should match the net to DDR Clk Replicator

The Negative DDR Clock signal should be routed s.t. the trancelength matches that of the positive DDR Clock net, and the length to the load cap (C366) and term R (R310) match the length of the feedback loop.

See Page 28 for the DDR Clock Replicator

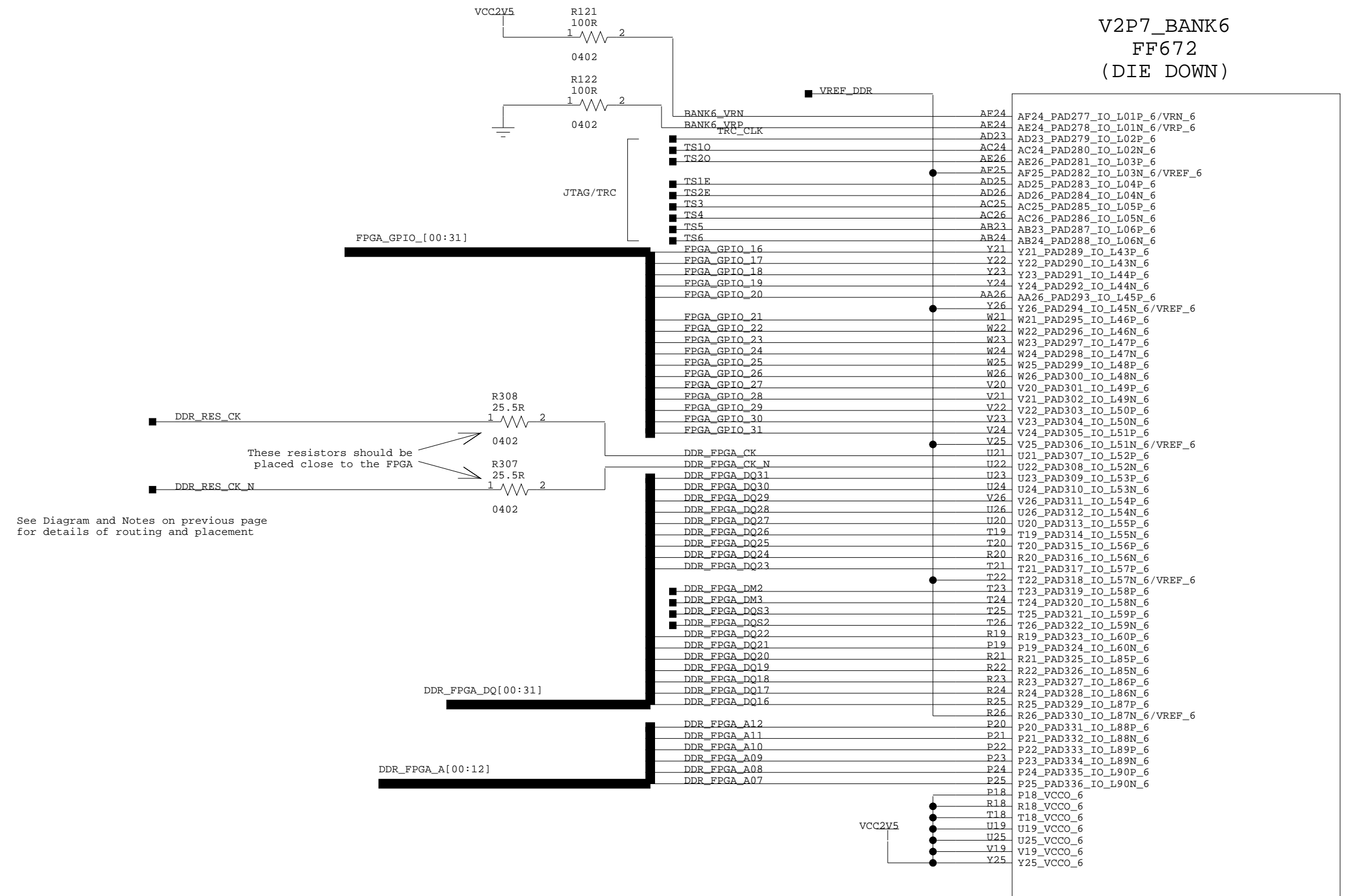
ML300 CPU - V2P7 Bank 5  
System ACE, CPU Debug



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU	
2VP7 Bank 5 System ACE and CPU Debug	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 17 of 56	Drawn By BP

V2P7\_BANK6  
FF672  
(DIE DOWN)



See Diagram and Notes on previous page for details of routing and placement

DEVICE=XC2VP7-6FF672C  
PKG\_TYPE=FF672  
PARTS=1  
LEVEL=STD

U1



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300\_CPU  
2VP7 Bank 6  
CPU Trace and DDR

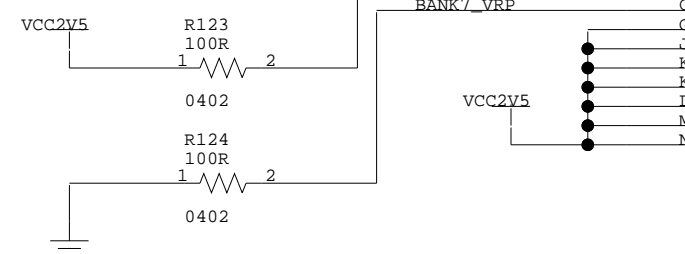
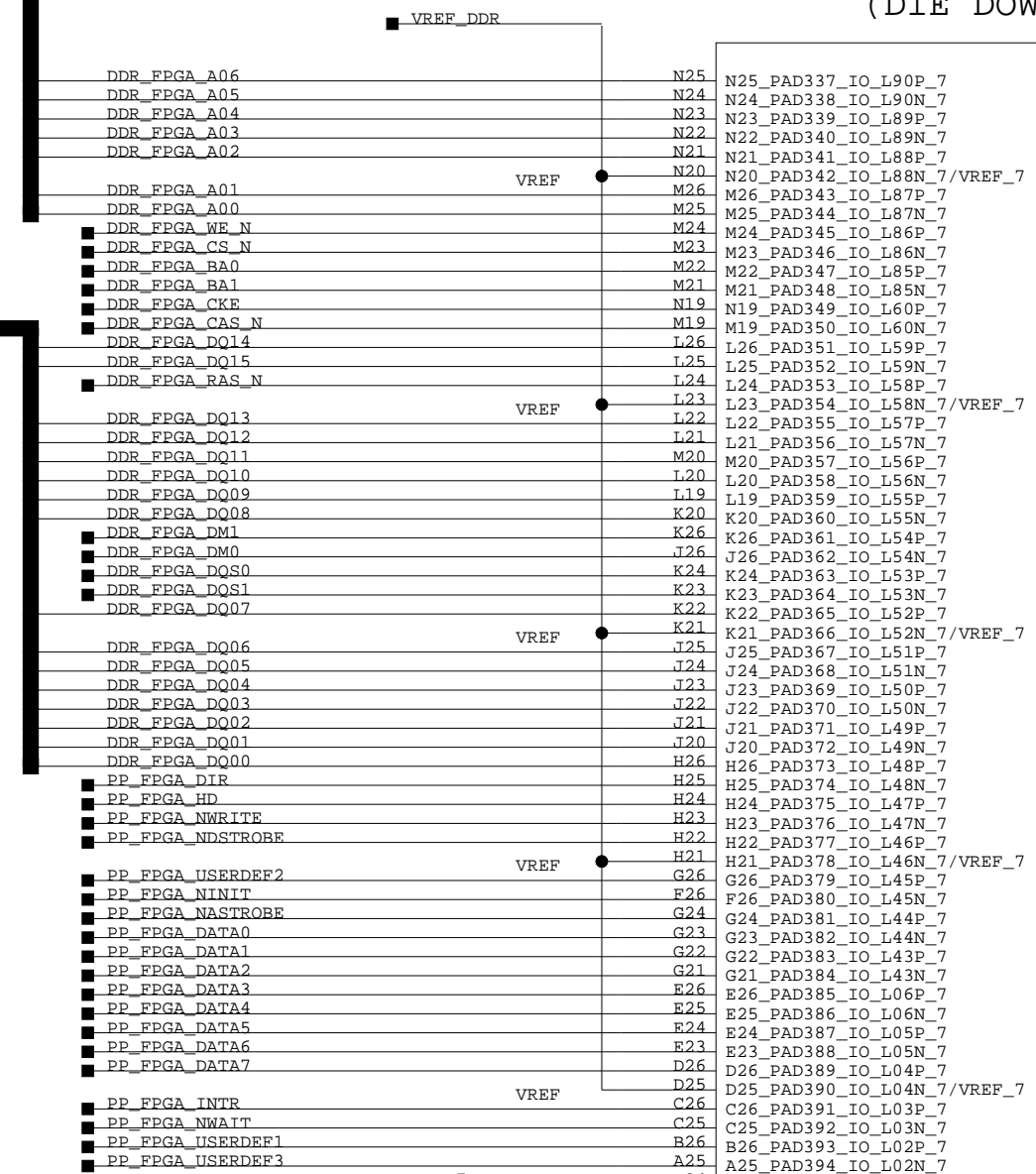
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 18 of 55	Drawn By BP

ML300 CPU - V2P7 Bank 6  
CPU Trace, DDR

V2P7\_BANK7  
FF672  
(DIE DOWN)

DDR\_FPGA\_A[00:12]

DDR\_FPGA\_DQ[00:31]



N25	N25_PAD337_IO_L90P_7
N24	N24_PAD338_IO_L90N_7
N23	N23_PAD339_IO_L89P_7
N22	N22_PAD340_IO_L89N_7
N21	N21_PAD341_IO_L88P_7
N20	N20_PAD342_IO_L88N_7/VREF_7
M26	M26_PAD343_IO_L87P_7
M25	M25_PAD344_IO_L87N_7
M24	M24_PAD345_IO_L86P_7
M23	M23_PAD346_IO_L86N_7
M22	M22_PAD347_IO_L85P_7
M21	M21_PAD348_IO_L85N_7
N19	N19_PAD349_IO_L60P_7
M19	M19_PAD350_IO_L60N_7
L26	L26_PAD351_IO_L59P_7
L25	L25_PAD352_IO_L59N_7
L24	L24_PAD353_IO_L58P_7
L23	L23_PAD354_IO_L58N_7/VREF_7
L22	L22_PAD355_IO_L57P_7
L21	L21_PAD356_IO_L57N_7
M20	M20_PAD357_IO_L56P_7
L20	L20_PAD358_IO_L56N_7
L19	L19_PAD359_IO_L55P_7
K20	K20_PAD360_IO_L55N_7
K26	K26_PAD361_IO_L54P_7
J26	J26_PAD362_IO_L54N_7
K24	K24_PAD363_IO_L53P_7
K23	K23_PAD364_IO_L53N_7
K22	K22_PAD365_IO_L52P_7
K21	K21_PAD366_IO_L52N_7/VREF_7
J25	J25_PAD367_IO_L51P_7
J24	J24_PAD368_IO_L51N_7
J23	J23_PAD369_IO_L50P_7
J22	J22_PAD370_IO_L50N_7
J21	J21_PAD371_IO_L49P_7
J20	J20_PAD372_IO_L49N_7
H26	H26_PAD373_IO_L48P_7
H25	H25_PAD374_IO_L48N_7
H24	H24_PAD375_IO_L47P_7
H23	H23_PAD376_IO_L47N_7
H22	H22_PAD377_IO_L46P_7
H21	H21_PAD378_IO_L46N_7/VREF_7
G26	G26_PAD379_IO_L45P_7
F26	F26_PAD380_IO_L45N_7
G24	G24_PAD381_IO_L44P_7
G23	G23_PAD382_IO_L44N_7
G22	G22_PAD383_IO_L43P_7
G21	G21_PAD384_IO_L43N_7
E26	E26_PAD385_IO_L06P_7
E25	E25_PAD386_IO_L06N_7
E24	E24_PAD387_IO_L05P_7
E23	E23_PAD388_IO_L05N_7
D26	D26_PAD389_IO_L04P_7
D25	D25_PAD390_IO_L04N_7/VREF_7
C26	C26_PAD391_IO_L03P_7
C25	C25_PAD392_IO_L03N_7
B26	B26_PAD393_IO_L02P_7
A25	A25_PAD394_IO_L02N_7
D24	D24_PAD395_IO_L01P_7/VRN_7
C23	C23_PAD396_IO_L01N_7/VRP_7
G25	G25_VCCO_7
J19	J19_VCCO_7
K19	K19_VCCO_7
K25	K25_VCCO_7
L18	L18_VCCO_7
M18	M18_VCCO_7
N18	N18_VCCO_7

DEVICE=XC2VP7-6FF672C  
PKG\_TYPE=FF672  
PARTS=1  
LEVEL=STD

U1

ML300 CPU - V2P7 Bank 7  
DDR and Parallel Port



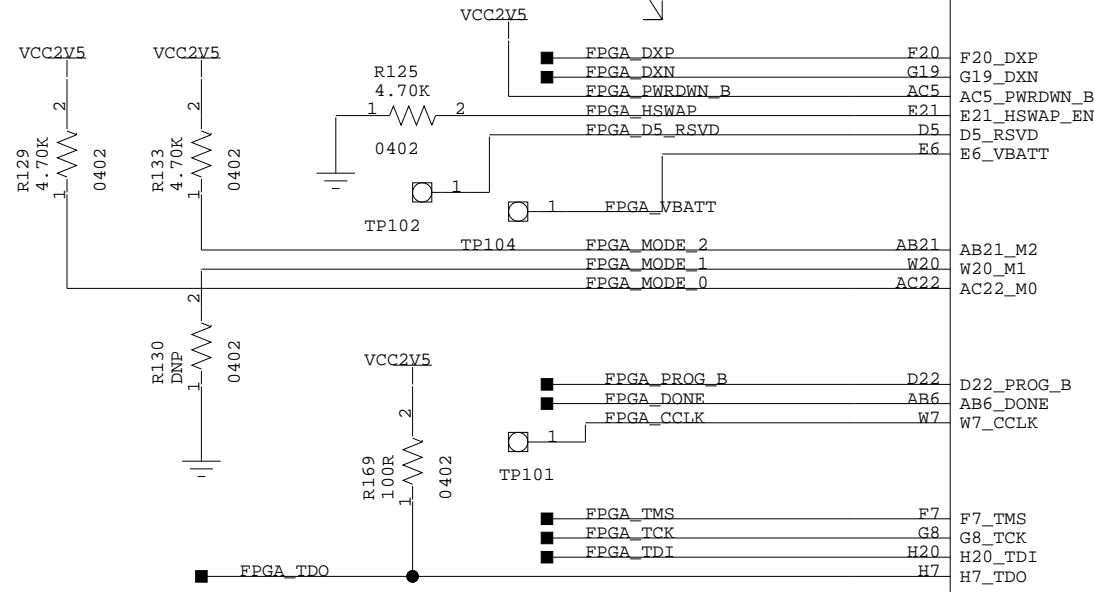
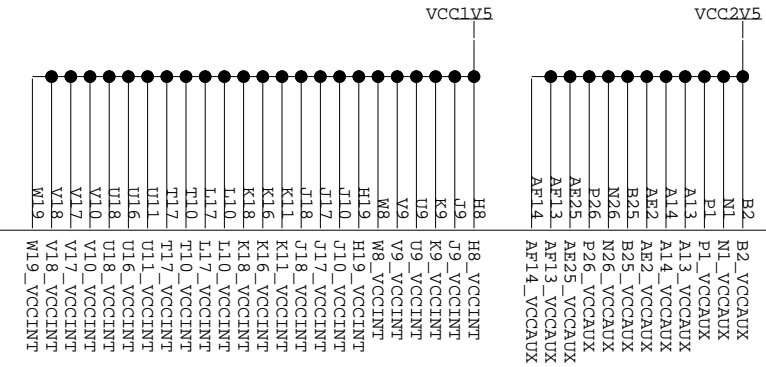
PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300\_CPU  
2VP7 Bank 7  
DDR and Parallel Port

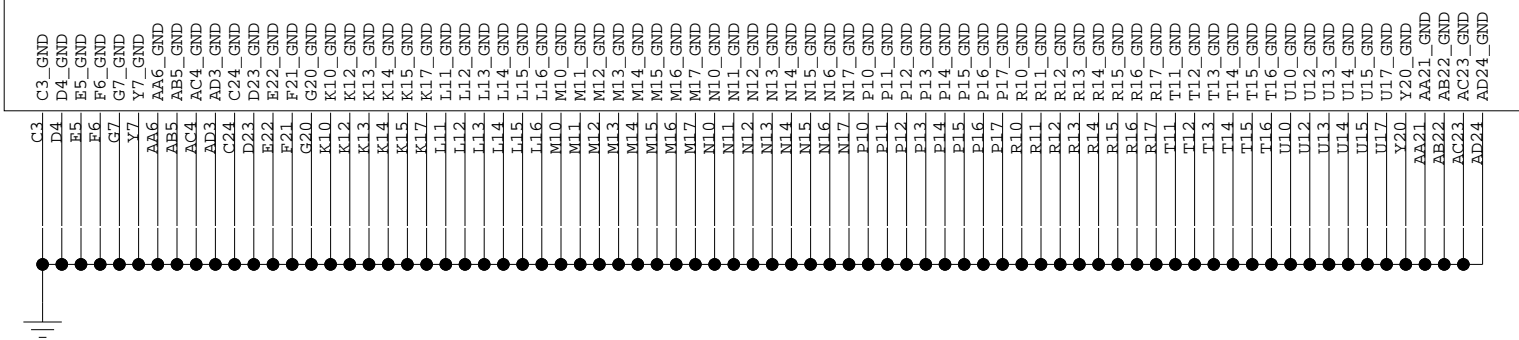
Date:	October 17th, 2002	Ver:	1.00
Sheet Size:	B	Rev:	A
Sheet	19 of 55	Drawn By	BP

These signals (FPGA\_DXP, FPGA\_DYN) should be routed as differential signals to the MAX11617AMEE (U251), and isolated from other signals as much as possible

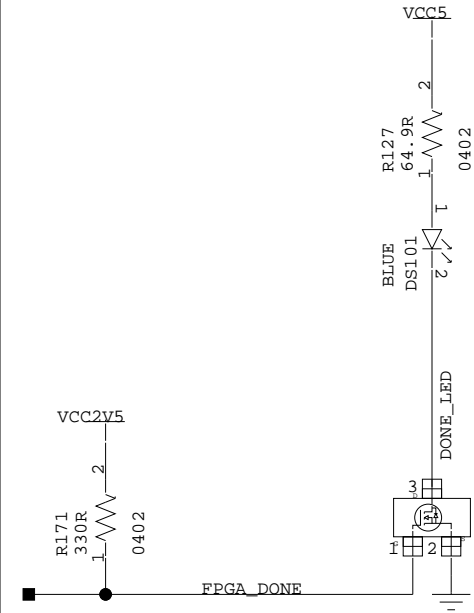
DEVICE=XC2VP7-6FF672C  
 PKG\_TYPE=FF672  
 PARTS=1  
 LEVEL=STD



V2P7\_MISC  
 FF672  
 (DIE DOWN)



Done LED



See Page 35 for placement of DS101

# ML300 CPU - V2P7 Auxiliary Miscellaneous/Config

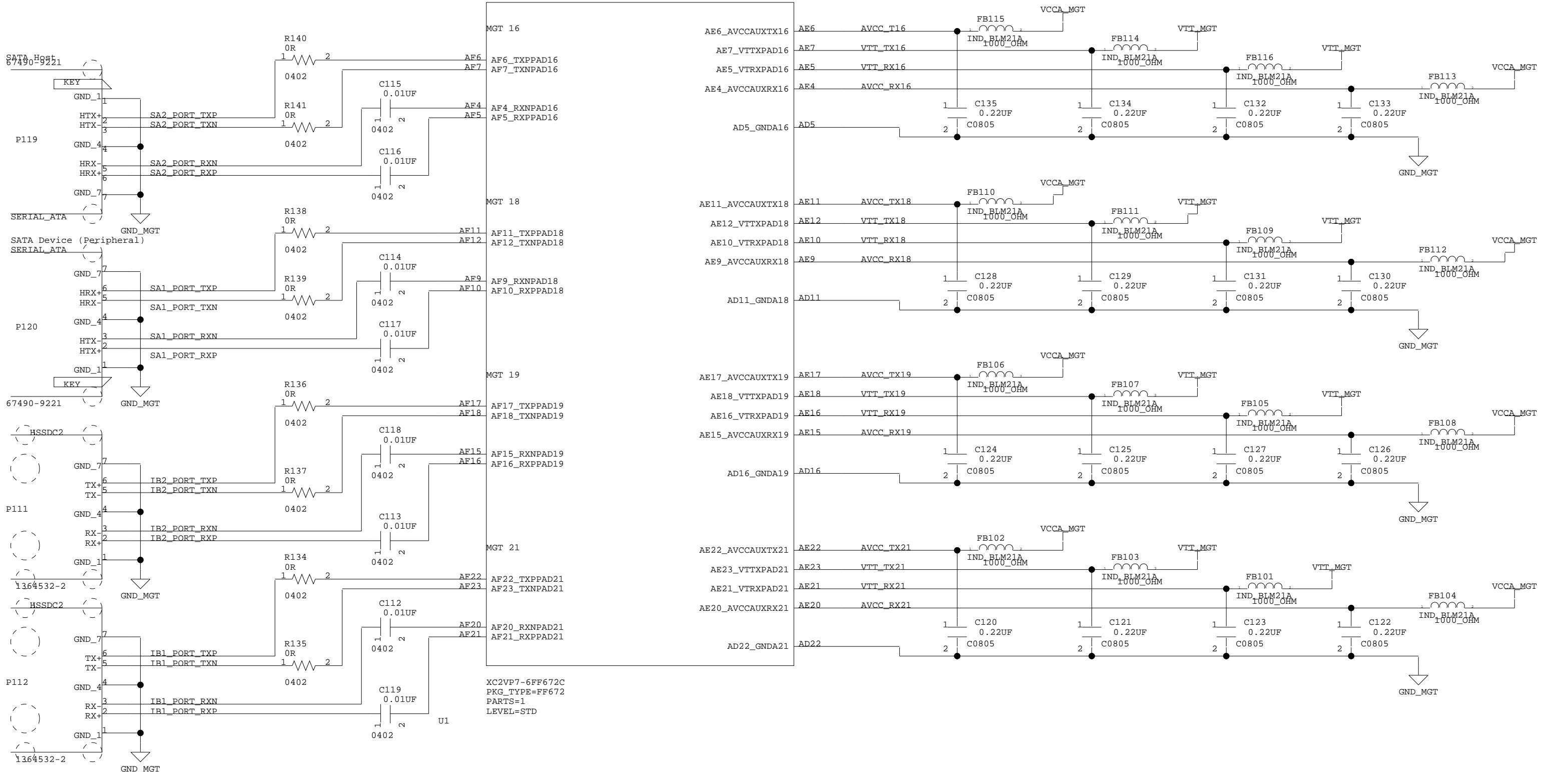


PCB: 1280285  
 ASM: 0431182  
 SCH: 0381135

Title: ML300_CPU 2VP7 Misc / Config	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 20 of 55	Drawn By BP

Silkscreen: "HSSDC2"

### V2P7\_MGT\_BOTTOM FF672 (DIE DOWN)



#### NOTES

- Each of the pairs must be matched trace length, such that  
 $GIGEX\_XX\_P + GIGEX\_XX\_CONN\_P = GIGEX\_XX\_N + GIGEX\_XX\_CONN\_N$
- Each of the pairs must be 100 ohm controlled differential impedance
  - track width XX mils
  - track spacing XX mils
- Put res on transmit lines (TX) near the connector, Caps on receive lines (RX) near the FPGA,
- Serial ATA Connectors shown flipped to more easily map to the V2Pro MGT pinout



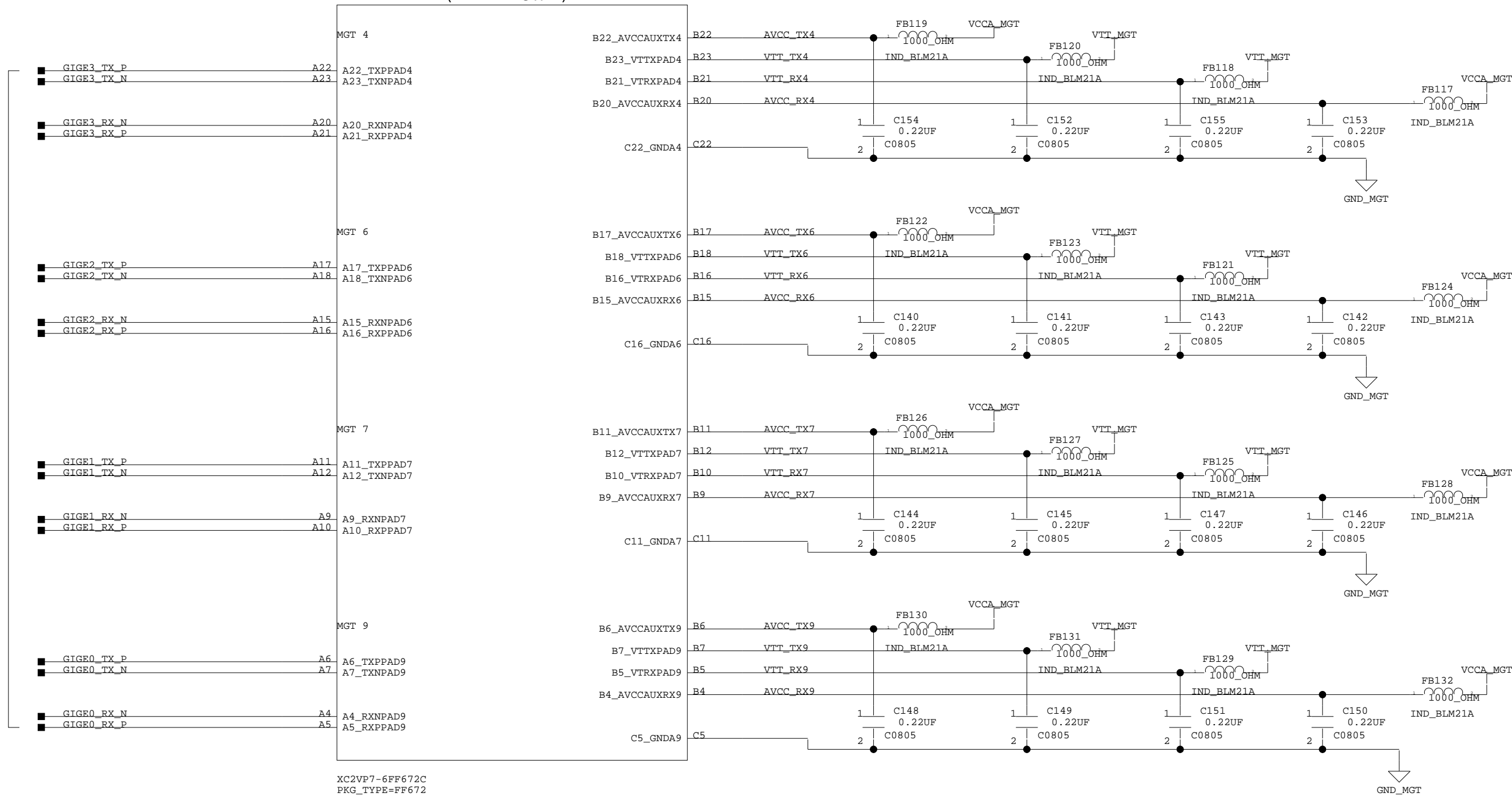
PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU	
2VP7 MGT Bottom HSSDC2 and Serial ATA	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 21 of 55	Drawn By BP

## ML300 CPU V2P7 MGT Bottom

V2P7\_MGT\_TOP  
FF672  
(DIE DOWN)

See Gigabit Ethernet Page (23)



XC2VP7-6FF672C  
PKG\_TYPE=FF672  
PARTS=1  
LEVEL=STD

U1

All 0.22UF caps on this page are 0805.



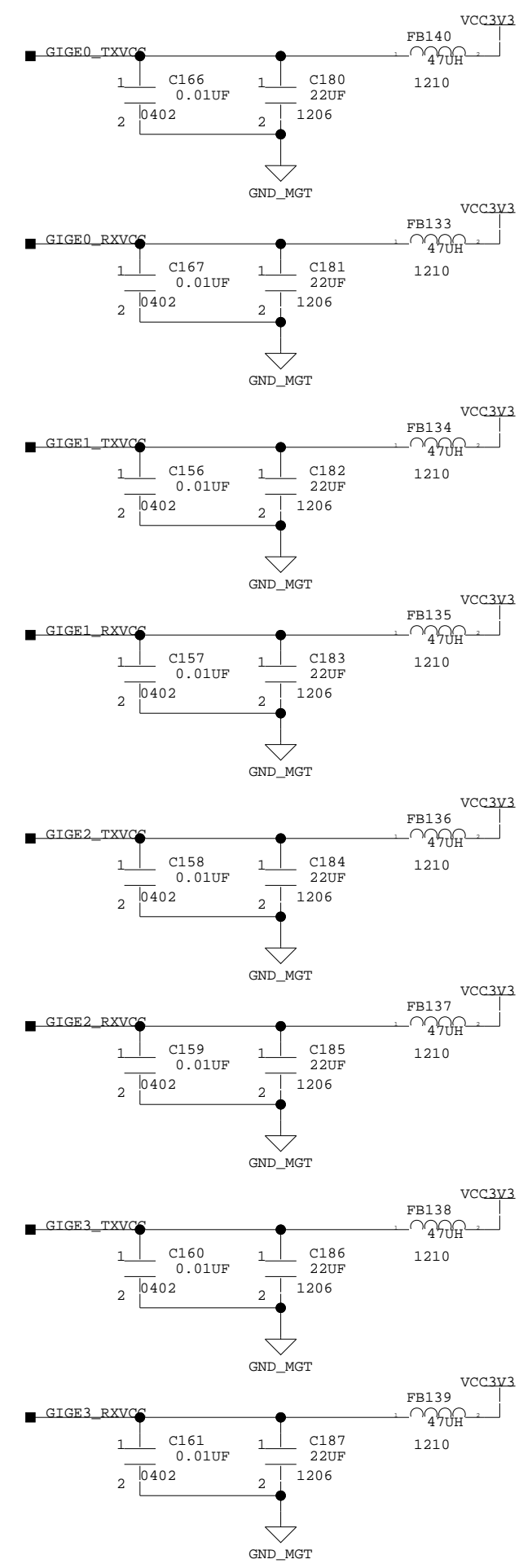
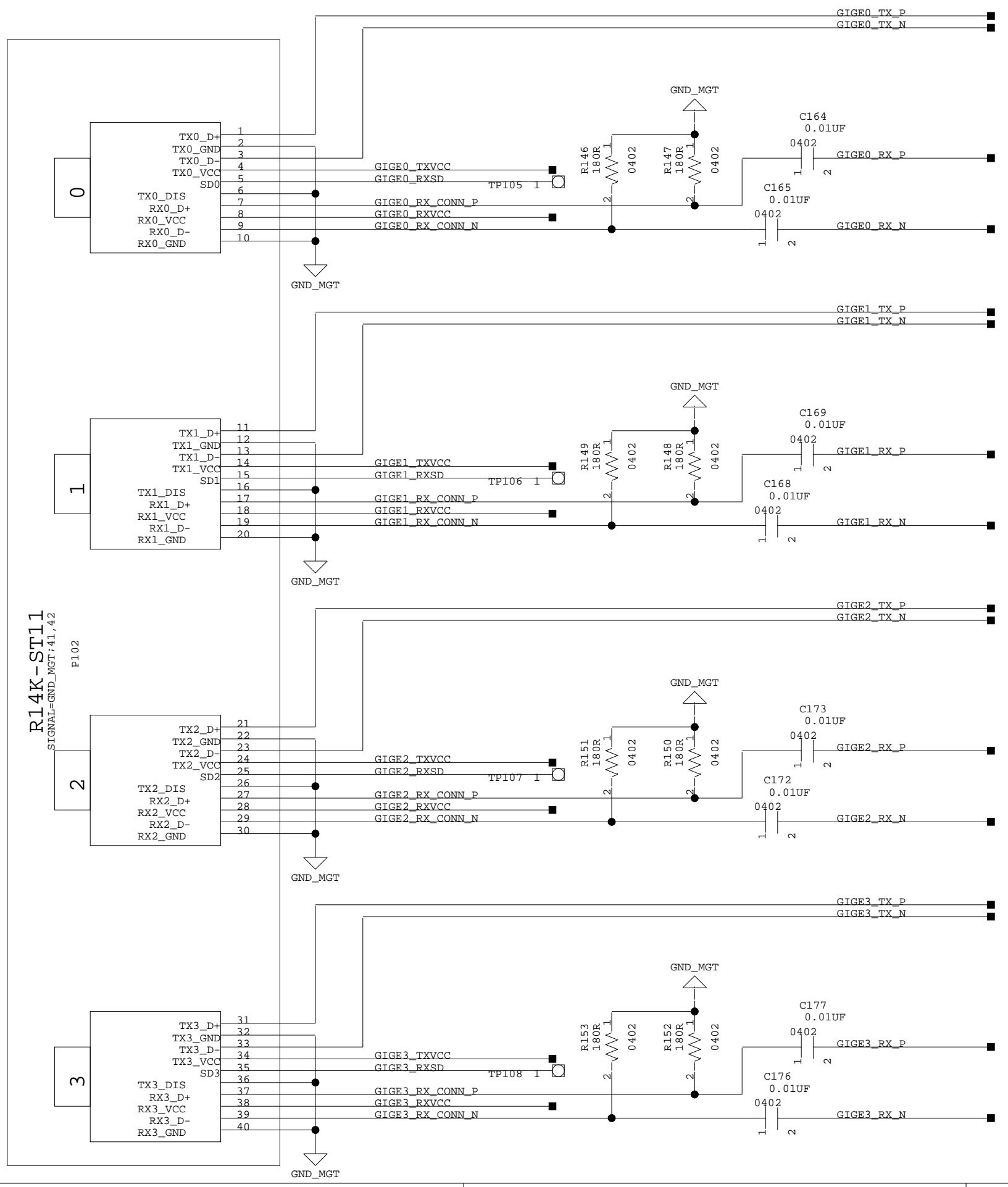
PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU 2VP7 MGT Top Gigabit Ethernet Fiber	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 22 of 55	Drawn By BP

ML300 CPU  
V2P7 MGT Top

### NOTES

- Each of the pairs must be matched trace length, such that  
 $GIGEX\_XX\_P + GIGEX\_XX\_CONN\_P = GIGEX\_XX\_N + GIGEX\_XX\_CONN\_N$
- Each of the pairs must be 100 ohm controlled differential impedance  
 - track width XX mils  
 - track spacing XX mils
- Put Caps on receive lines (RX) adjacent to the FPGA.
- TxVCC and RxVCC supply filters designed to filter out 50KHz-100KHz supply to R14K-ST11, a frequency of sensitivity for the R14K-ST11



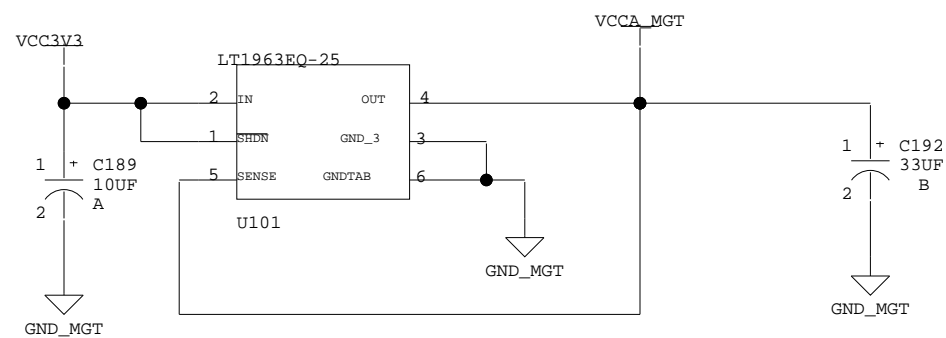
## ML300 CPU V2P7 MGT Top Fiber XCVR



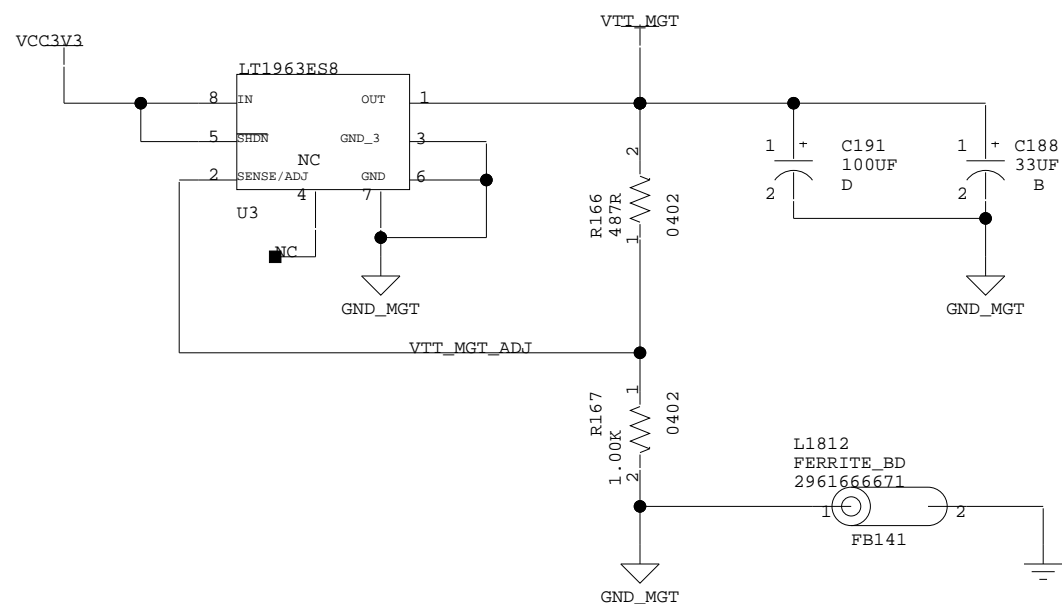
PCB: 1280285  
 ASM: 0431182  
 SCH: 0381135

Title: ML300_CPU	
Gigabit Ethernet Fiber Transceiver MGT Top	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 23 of 55	Drawn By BP

### MGT VCCA Linear Regulator



### MGT VTT Linear Regulator



## ML300 CPU MGT Power

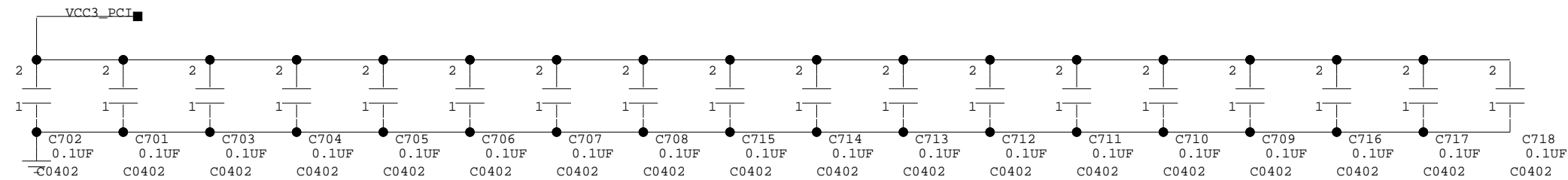


PCB: 1280285  
ASM: 0431182  
SCH: 0381135

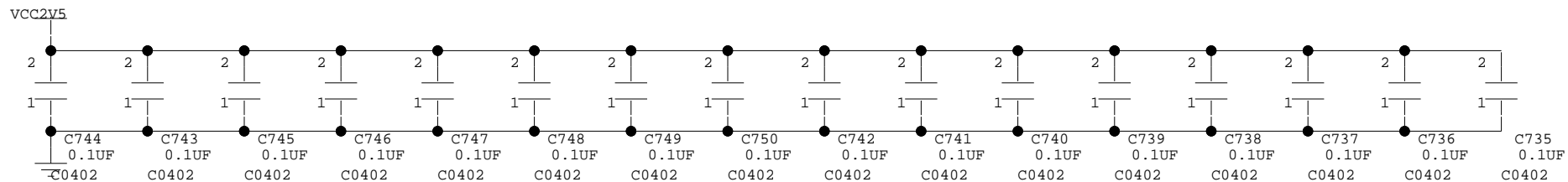
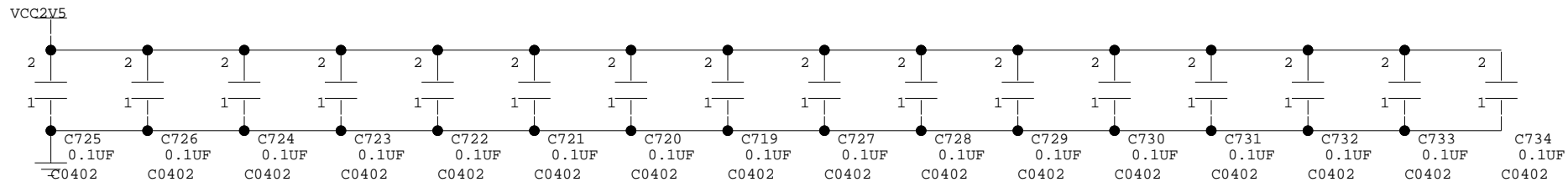
Title: ML300\_CPU  
MGT Power Supplies

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 24 of 55	Drawn By BP

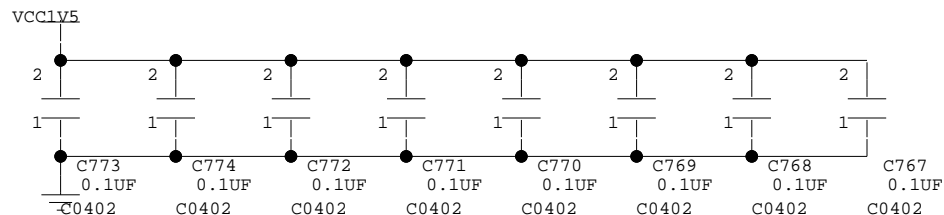
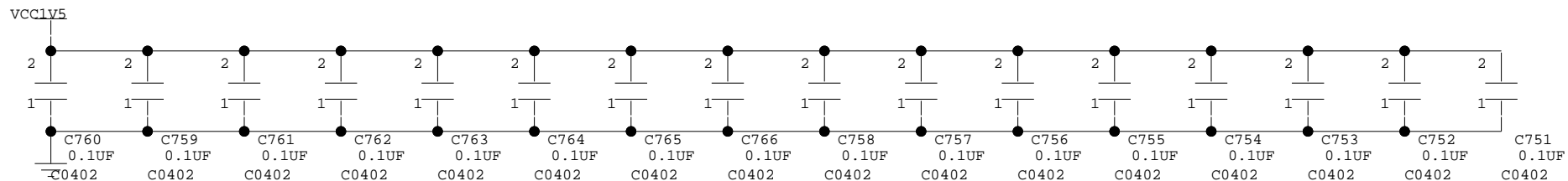




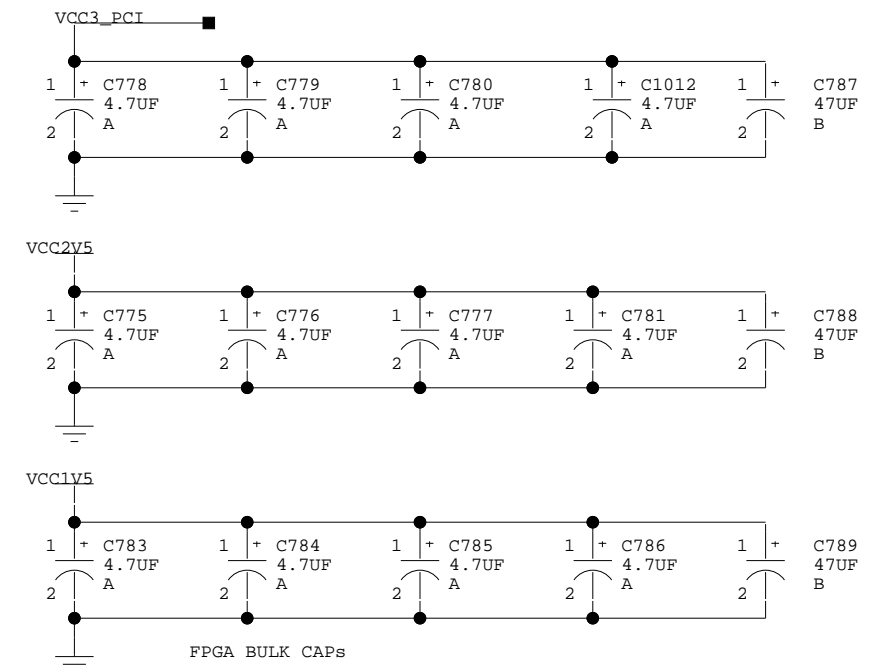
FPGA 3.3V VCCO CAPS, 1 per pin  
Placed as near as possible to U1



FPGA VCCO, VCCAUX CAPS, 1 per pin  
Placed as near as possible to U1



FPGA VCCO CAPS, 1 per pin  
Placed as near as possible to U1



FPGA BULK CAPS  
Placed as near as possible to U1

# ML300 CPU V2P7 Bypass Capacitors

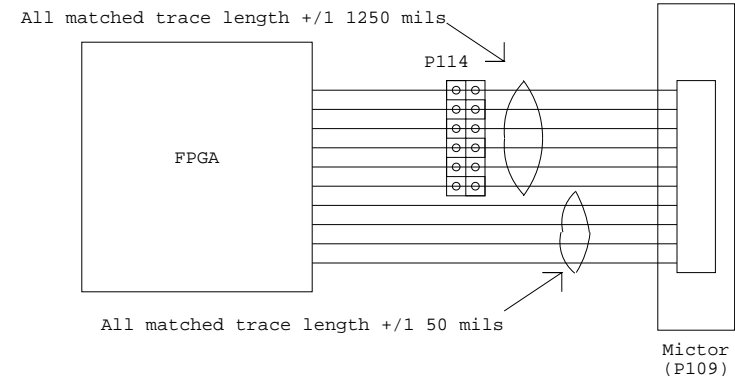


PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU V2P7 Bypass Capacitors	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 25 of 55	Drawn By GB

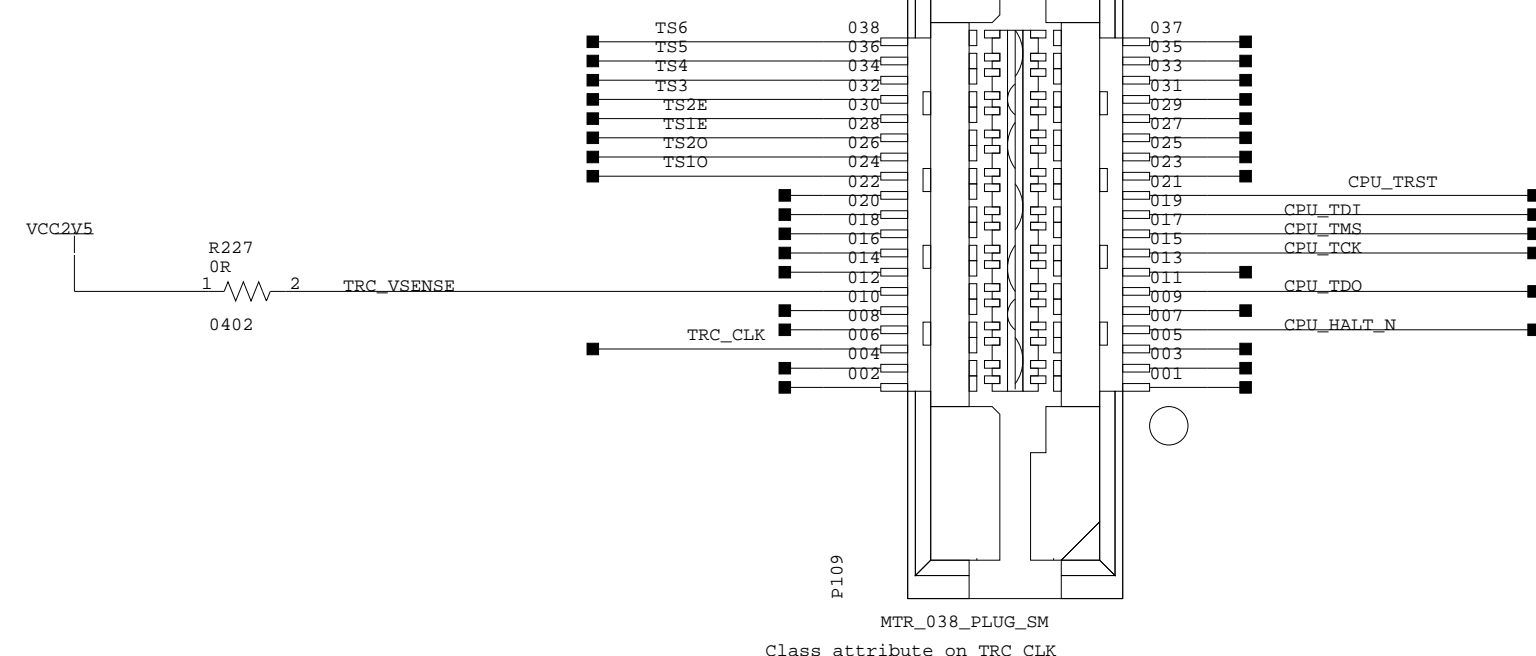
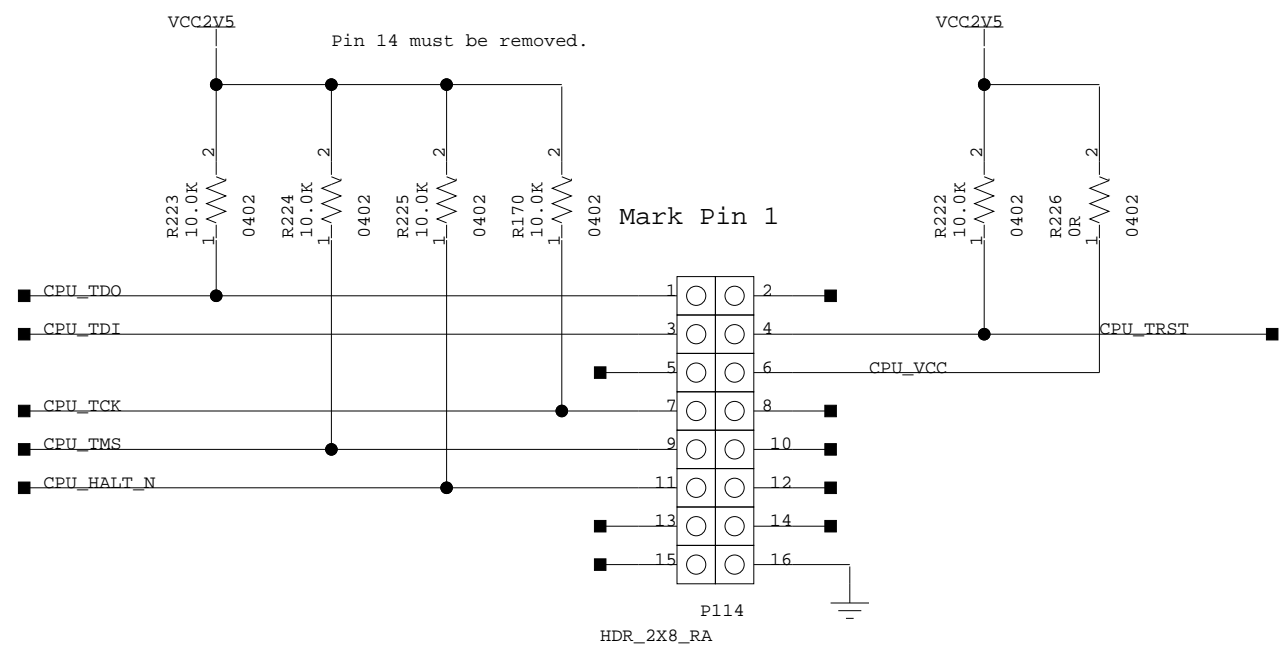
There are two sets of signals between the FPGA and the Mictor 38:

1. Bussed to include the 2X8 header above. These are the CPU Debug and should be +/- 1250 mils. The Header should be located between the Mictor and FPGA, so the FPGA and Mictor are the endpoints.
2. Only connected to the Mictor and FPGA. These are the CPU Trace and should be +/- 50 mils.



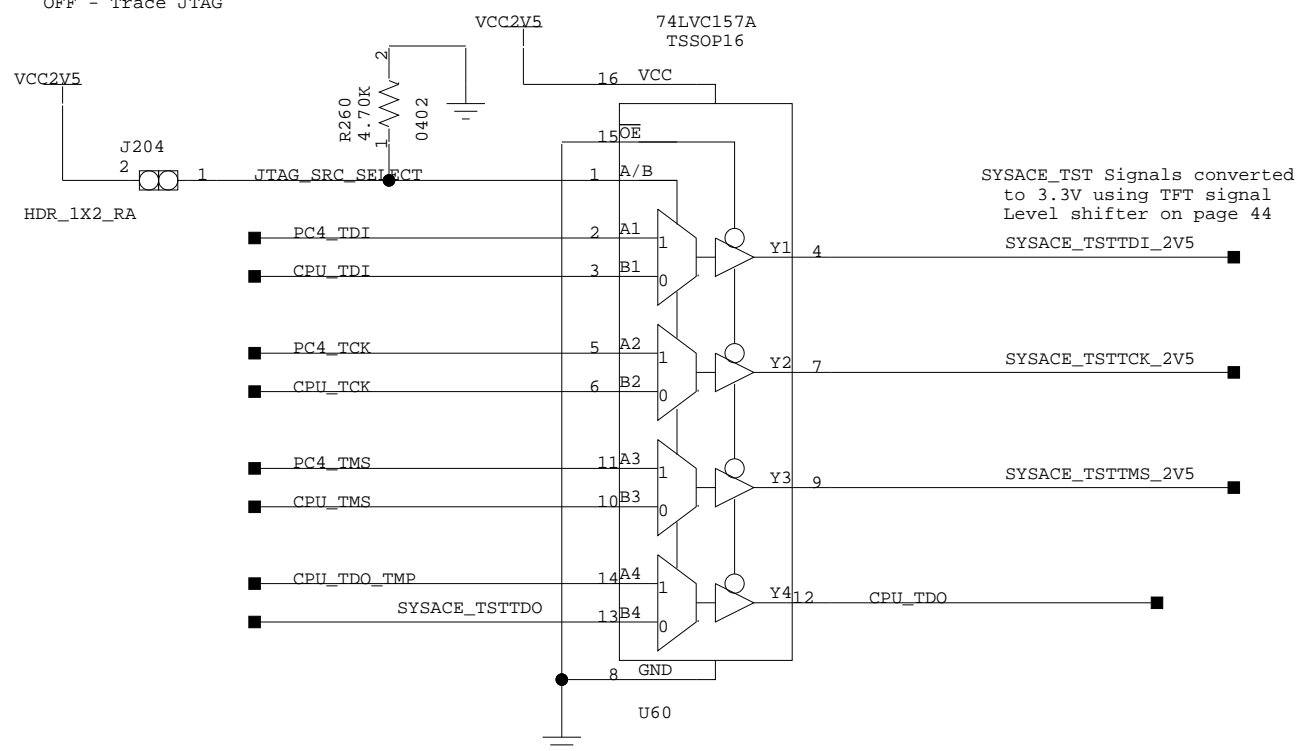
Mark Pin 1

Silkscreen:

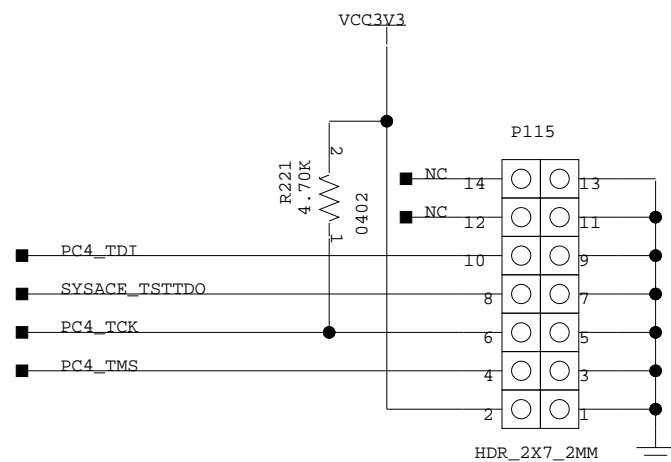


J204:

ON - PC4 JTAG  
OFF - Trace JTAG



Mark Pin 1



ML300 CPU  
V2P7 Bank 5/6 (17/18)  
Trace + Debug



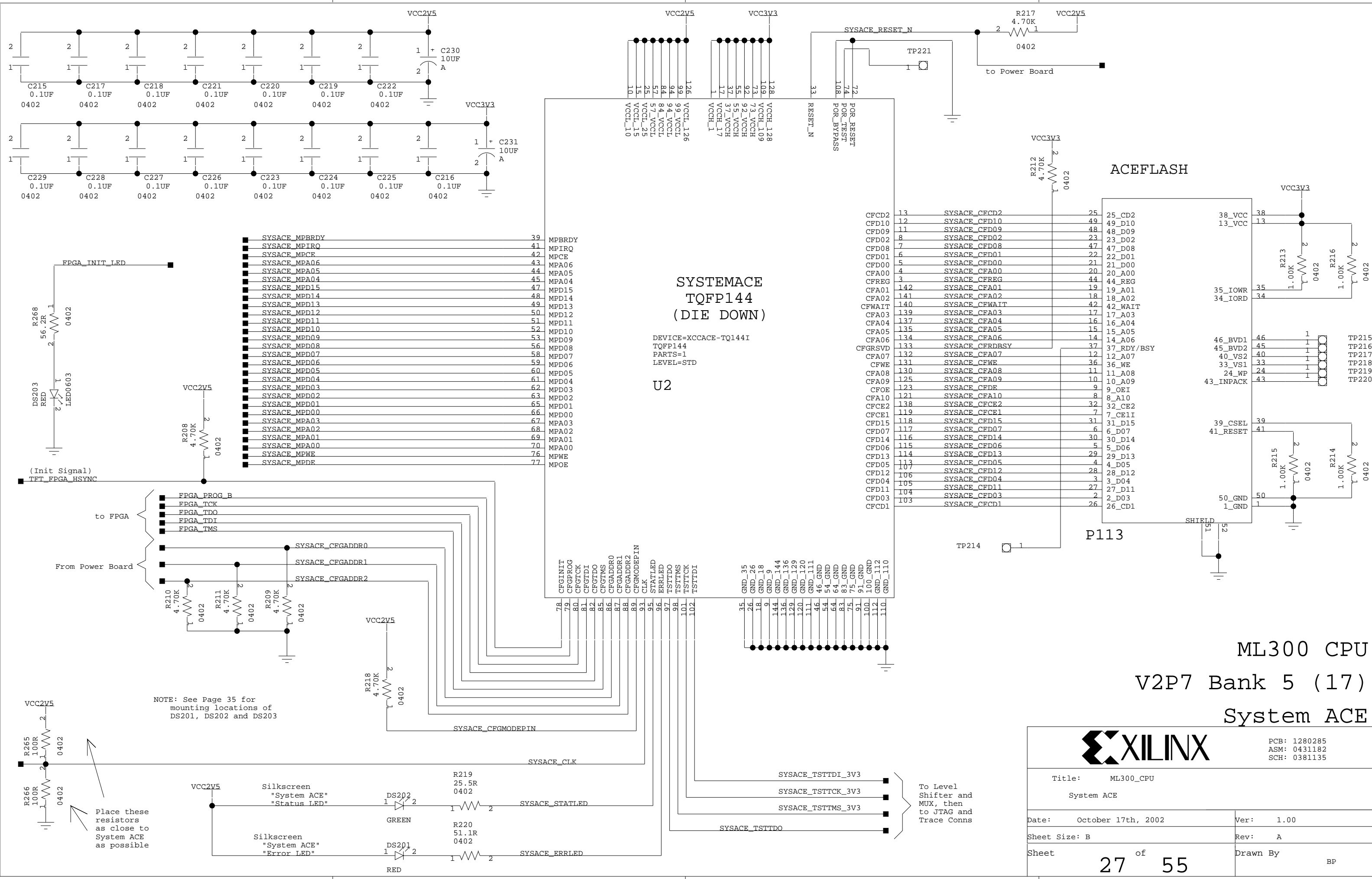
PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300\_CPU  
CPU Debug and Trace

Date: October 17th, 2002 Ver: 1.00

Sheet Size: B Rev: A

Sheet 26 of 55 Drawn By BP



PCB: 1280285  
 ASM: 0431182  
 SCH: 0381135

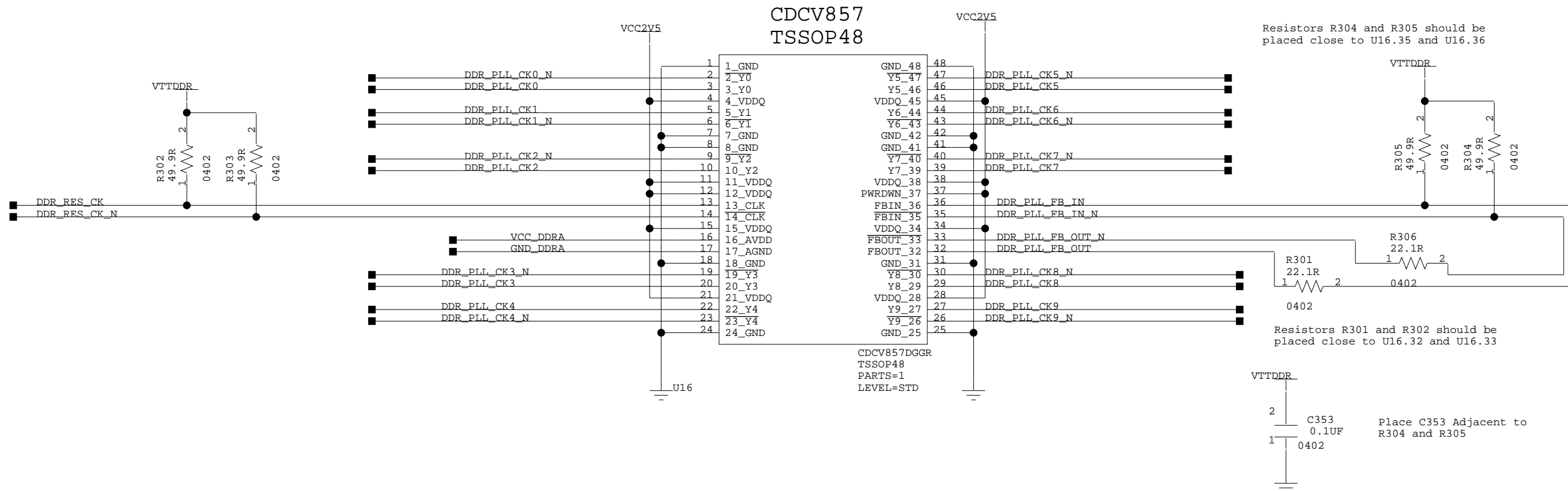
Title: ML300_CPU System ACE	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 27 of 55	Drawn By BP

NOTE: See Page 35 for mounting locations of DS201, DS202 and DS203

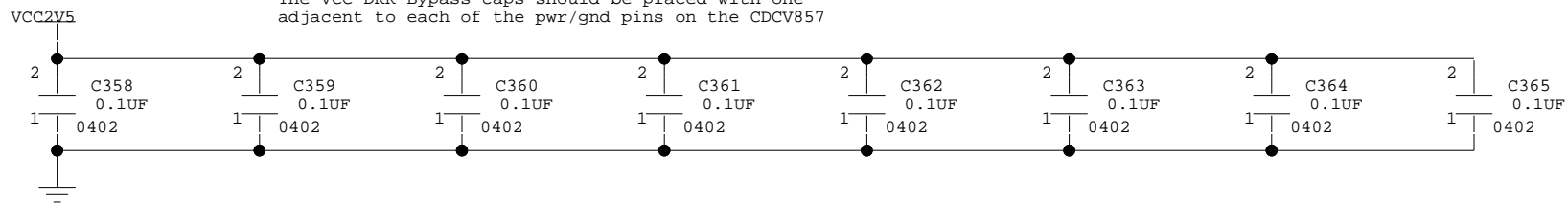
Place these resistors as close to System ACE as possible

To Level Shifter and MUX, then to JTAG and Trace Conns

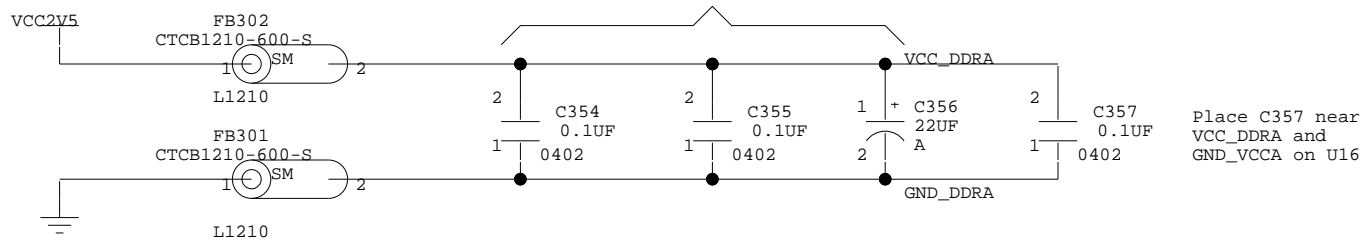
All of the CLK pairs should match tracelength  
 DDR\_CLK\_PLL Class on DDR\_PLL\_CK0, 3 and 6  
 See diagram on Page 17 for routing of clock  
 signals to FPGA



The VCC DRR Bypass caps should be placed with one adjacent to each of the pwr/gnd pins on the CDCV857



These Bypass caps should be placed adjacent to FB310 and FB302



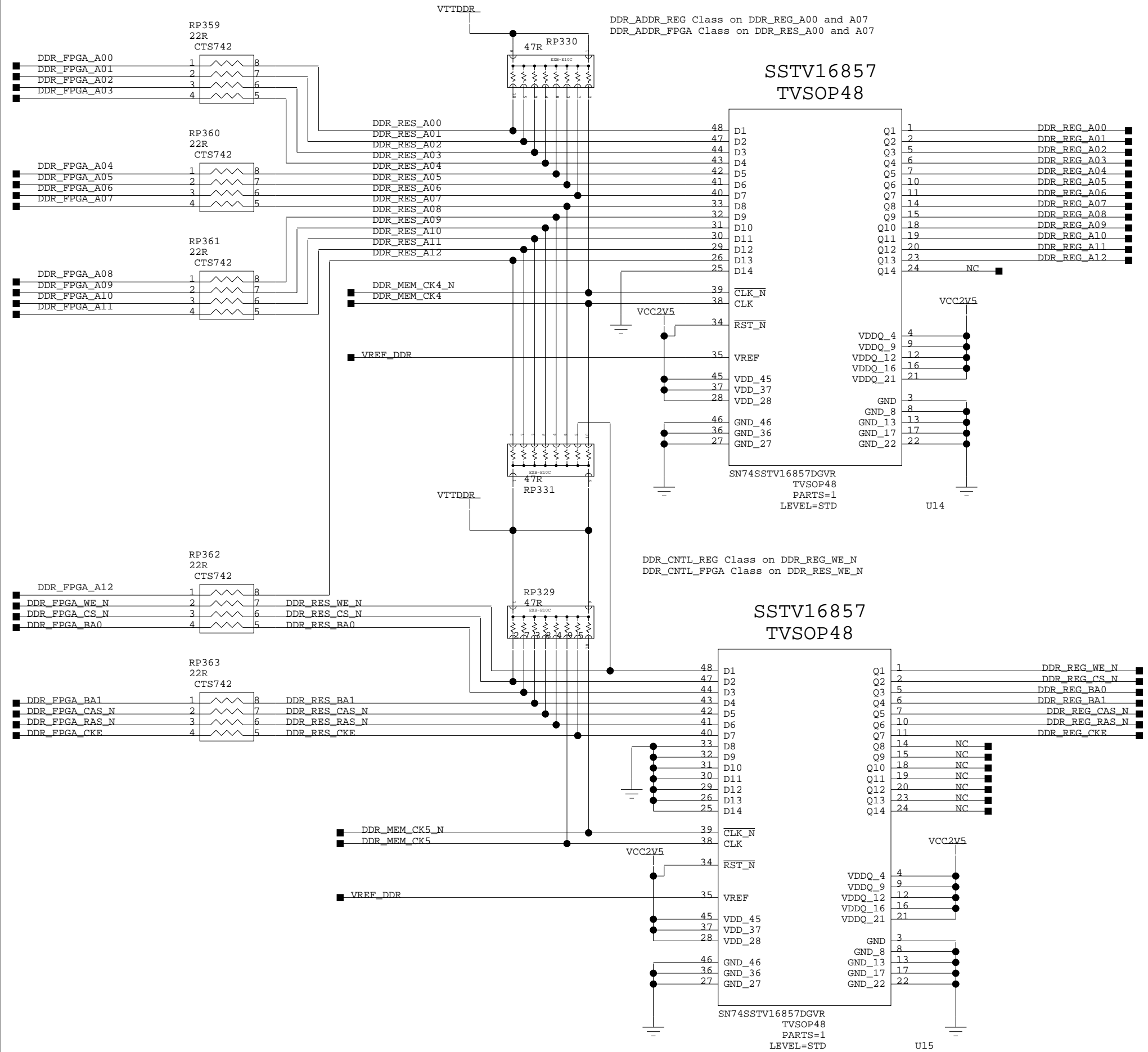
# ML300 CPU

## DDR Clock Replicator



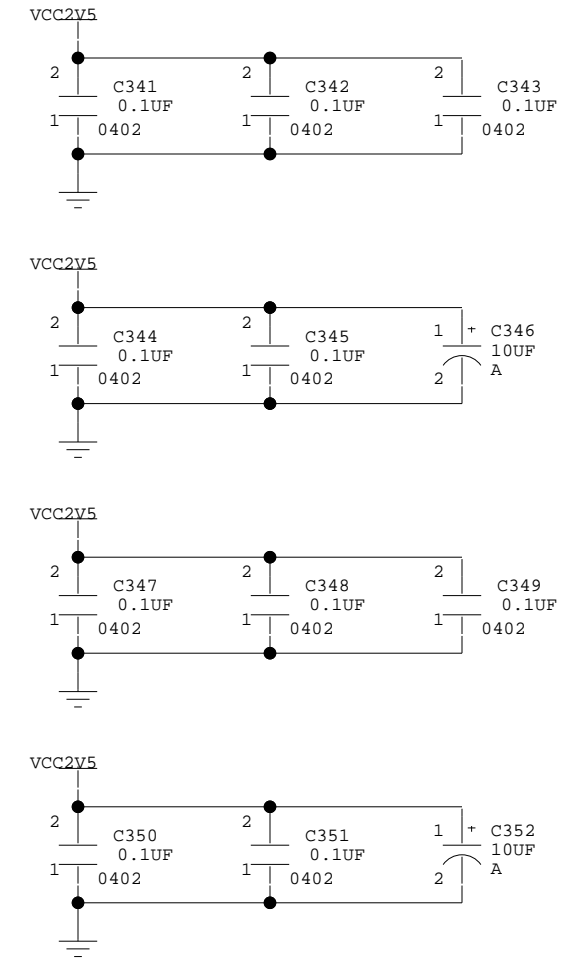
PCB: 1280285  
 ASM: 0431182  
 SCH: 0381135

Title: ML300_CPU DDR SDRAM - Clock PLL	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 28 of 55	Drawn By BP



NOTES:

1. All Traces are 50 ohm Controlled impedance.
2. Termination Rs to DDR componenets are shown on page 31.
3. Series and Parallel termination resistors on this page should be placed as close as possible to the DDR chips.
4. the 0.1UF caps should be placed at each VCC pins of both of the SSTV16859.
5. For details of trancelengths control, see page 56, Classes 1-8.

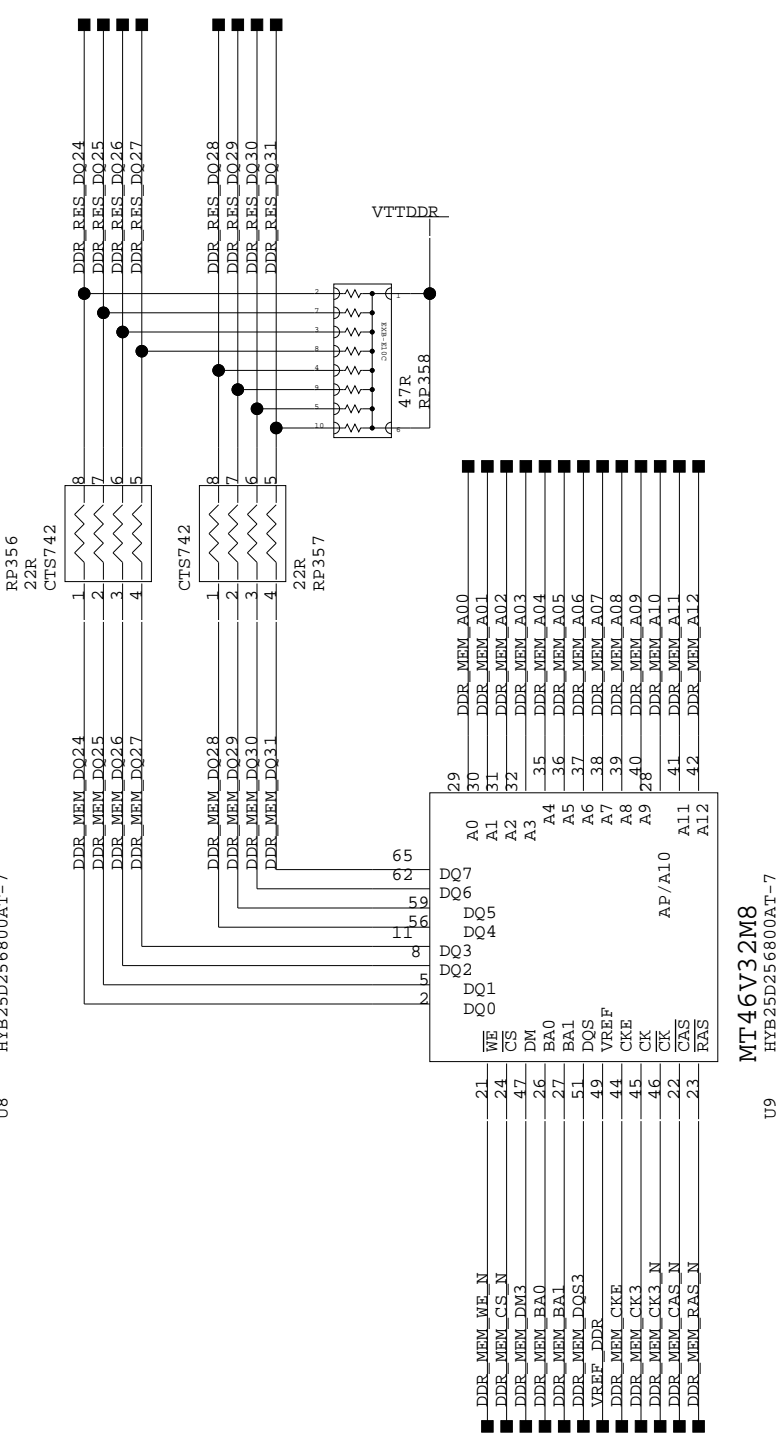
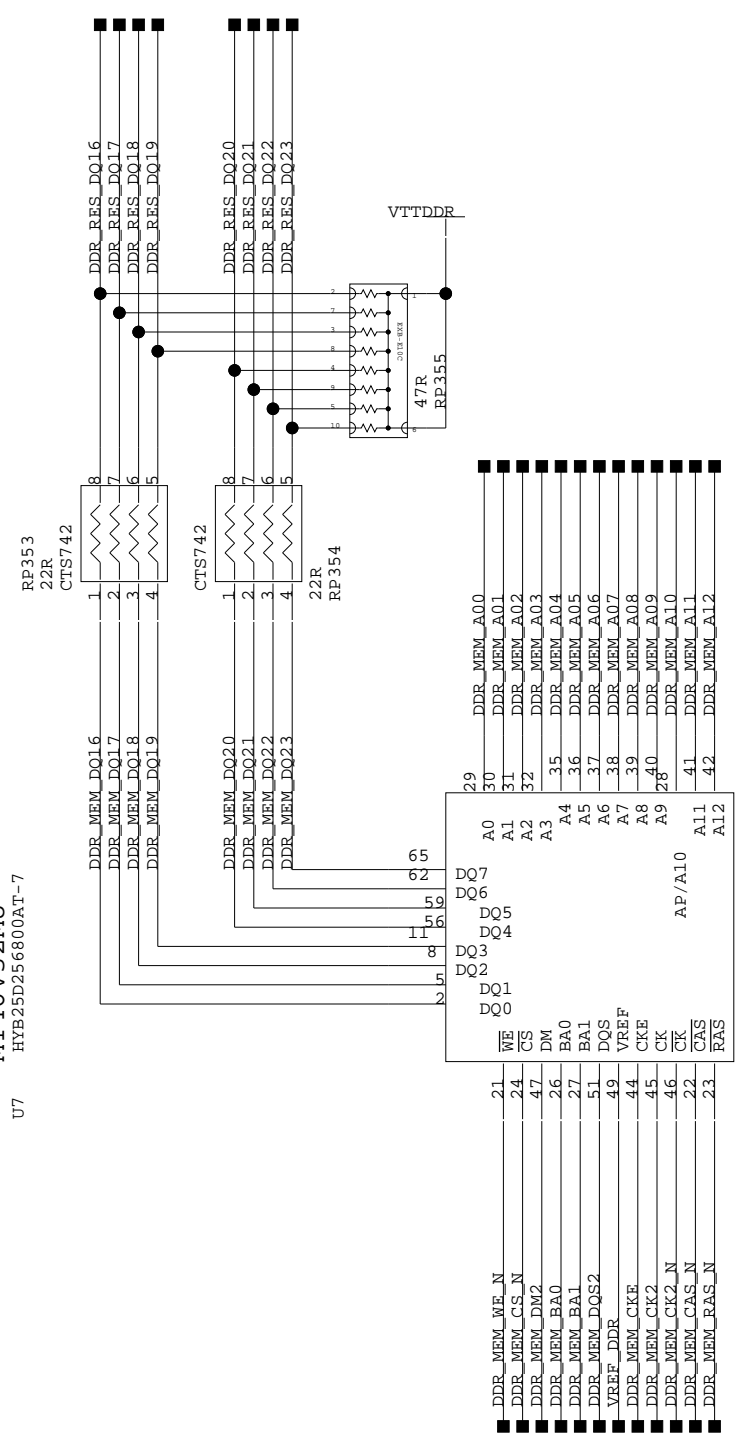
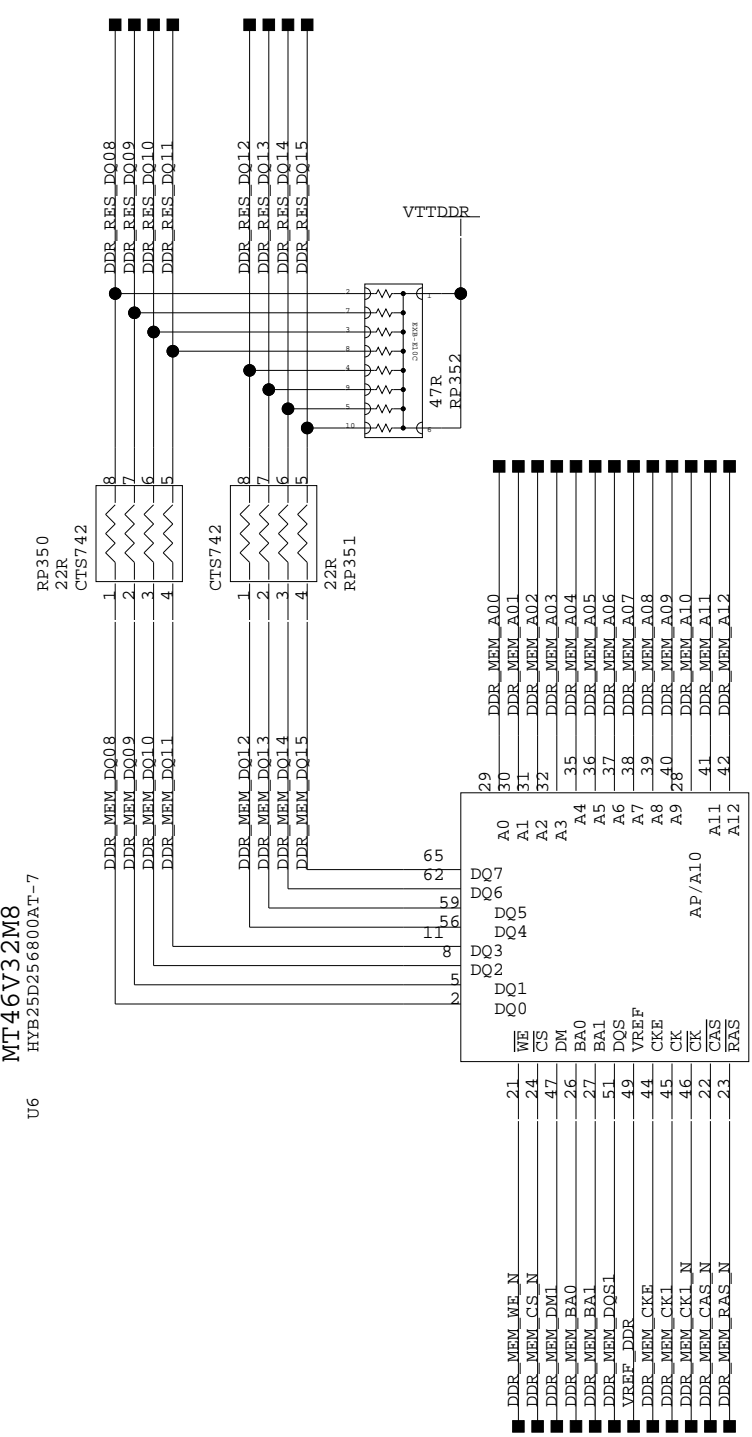
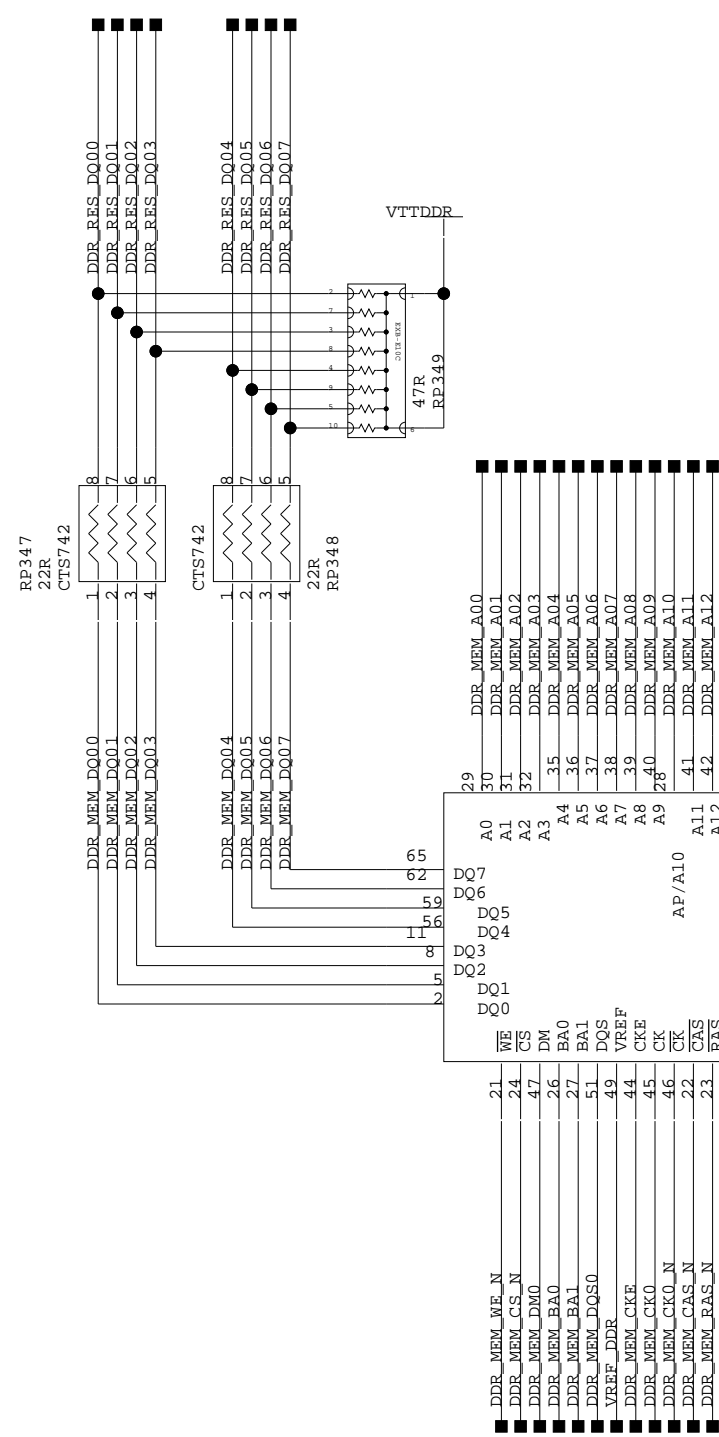


ML300 CPU  
V2P7 Bank 6/7 (18/19)  
Registers for DDR SDRAM



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU DDR SDRAM - Registers	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 29 of 56	Drawn By BP



Silkscreen: "DDR SDRAM - 4 of 8x32M"

ML300 CPU  
V2P7 Bank 6/7 (18/19)  
DDR SDRAM Chips

- NOTES:**
- All Traces are 50 ohm Controlled impedance.
  - For details of trancelengths control, see page 56, Classes 1-8.
  - Series and Parallel termination resistors on this page should be placed as close as possible to the DDR chips.
  - See page 34 for placement of bypass caps
  - Rest of Data path termination Rs shown on page 32

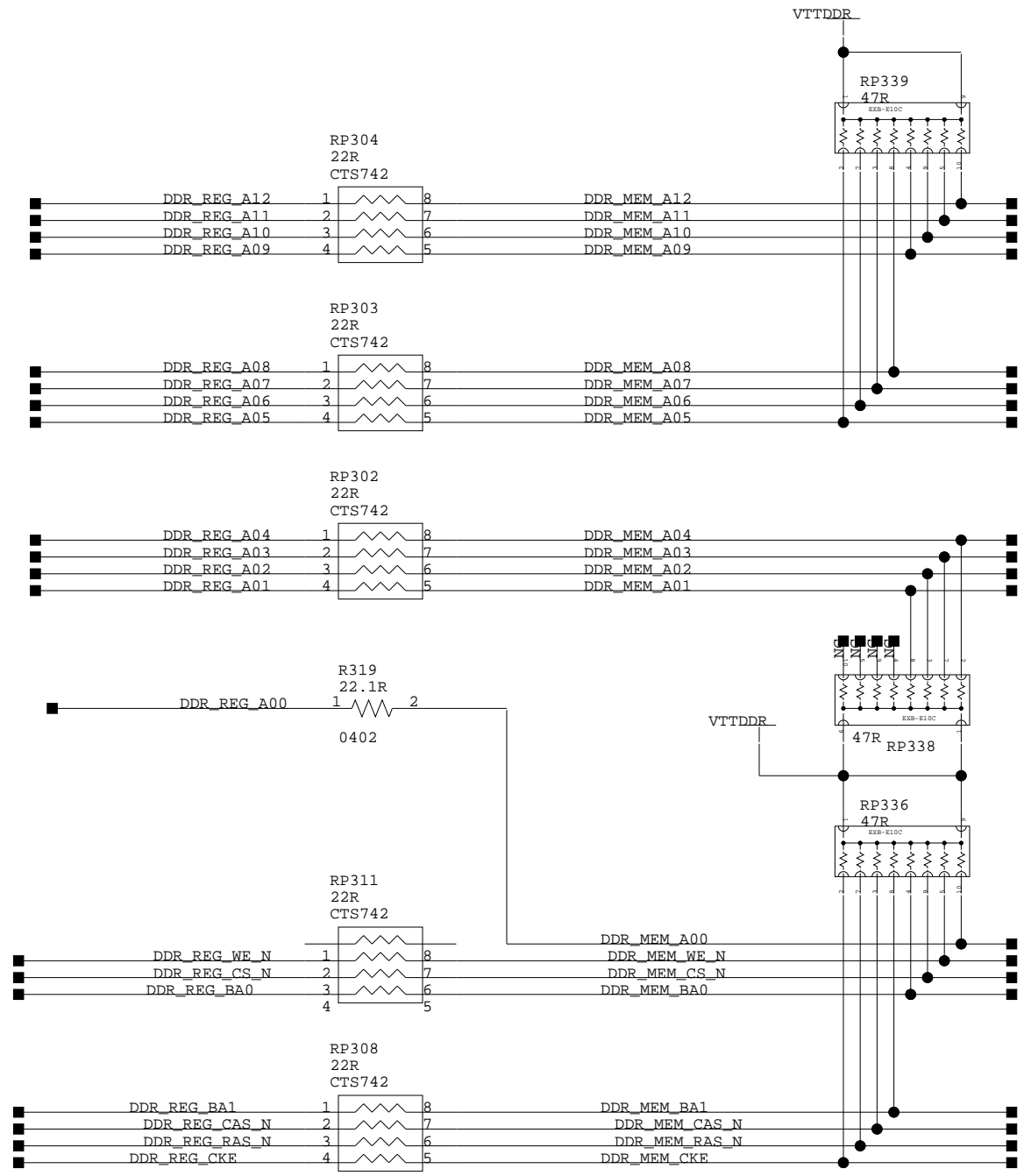


PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU DDR SDRAM - Components	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 30 of 56	Drawn By BP

NOTES:

- 1. Series termination resistors on this page should be placed as close as possible to the DDR registers (U14 and U15)
- 2. Parallel termination resistors on this page should be placed after the DDR chips relative to the DDR registers.
- 3. For details of tracelengths control, see page 56, Classes 1-8.



ML300 CPU  
 DDR Termination for DDR SDRAM  
 From Registers to Chips



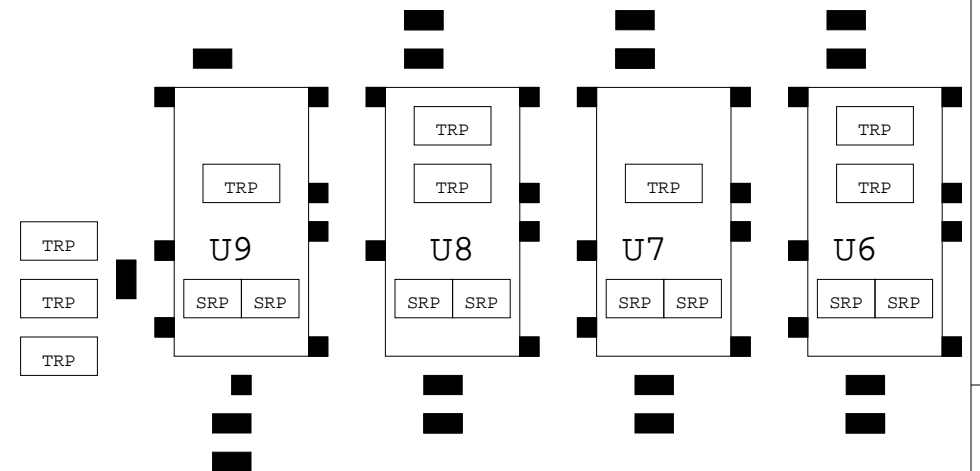
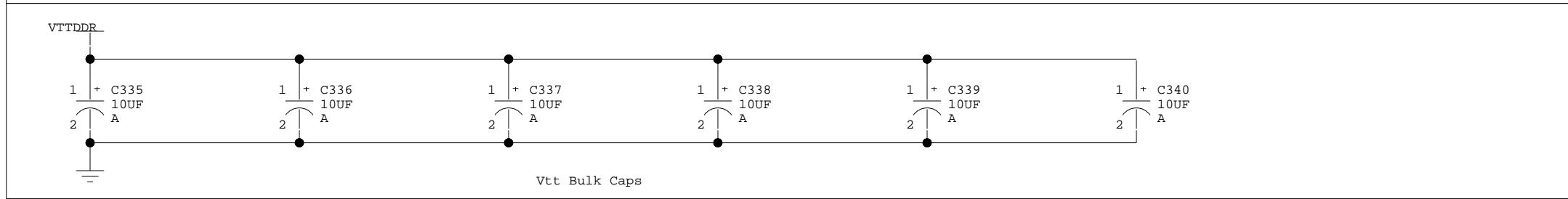
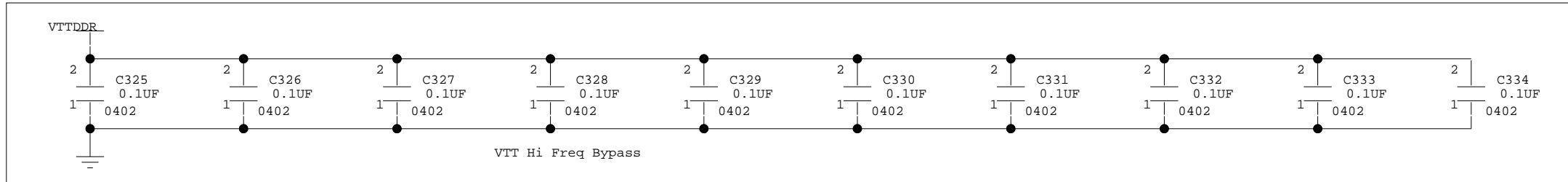
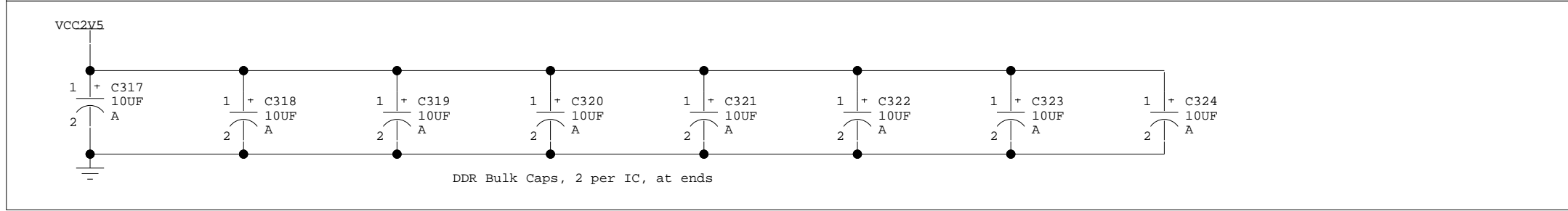
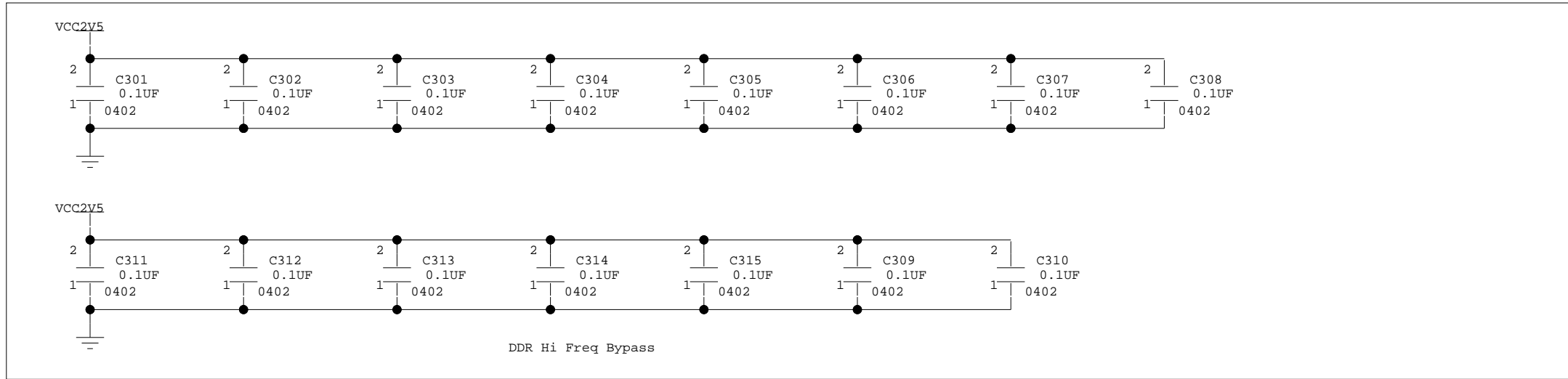
PCB: 1280285  
 ASM: 0431182  
 SCH: 0381135

Title: ML300_CPU DDR SDRAM - Termination (1 of 2)	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 31 of 56	Drawn By BP















LAYOUT FOR DDR, CAPS, RPs  
(X-Ray View to Bottom Side)

-  DDR Bulk Caps
-  DDR HF Bypass Caps (MLC)
-  VTT Bulk Caps
-  VTT HF Bypass Caps (MLC)
-  Termination Resistor Pack
-  Series Resistor Pack

# ML300 CPU

## DDR Bypass Capacitors

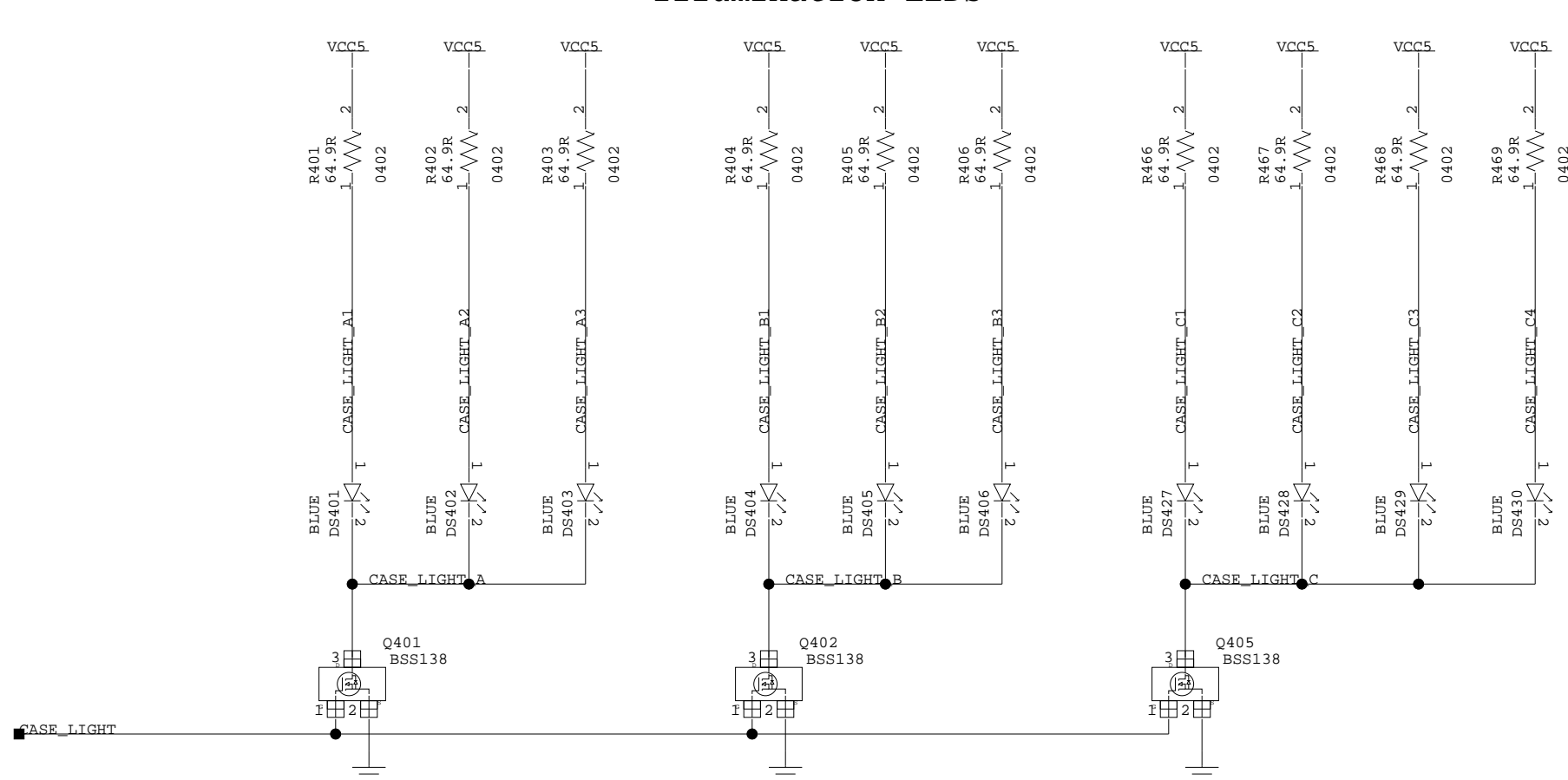


PCB: 1280285  
ASM: 0431182  
SCH: 0381135

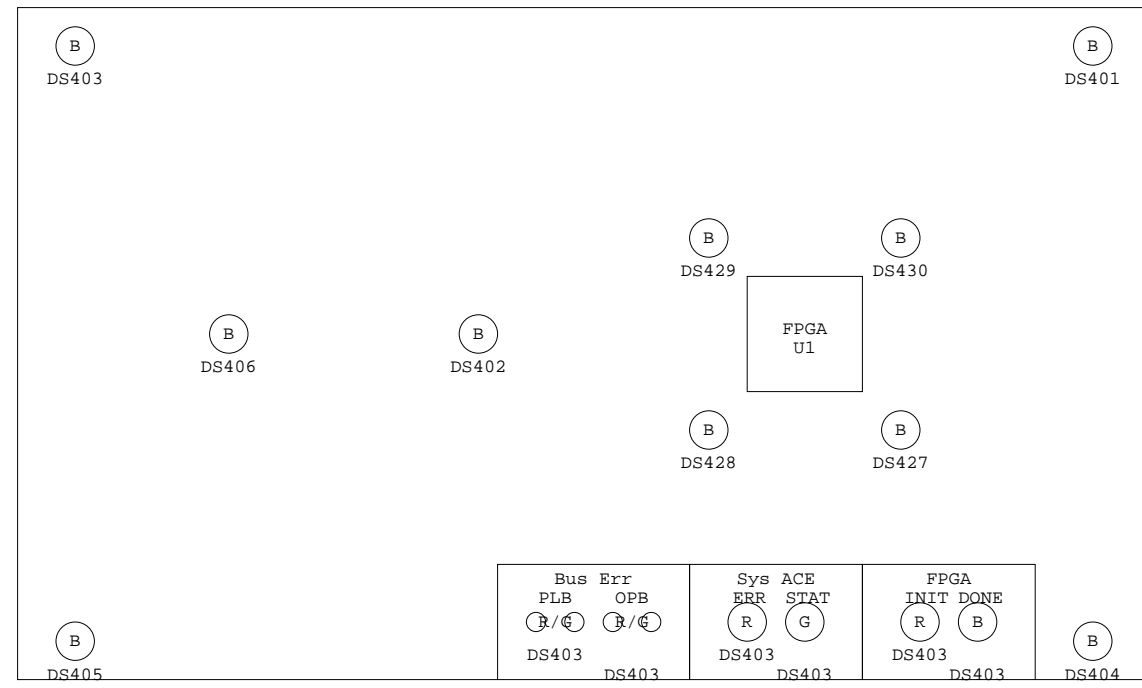
Title: ML300\_CPU  
DDR SDRAM - Bypass Caps

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 34 of 55	Drawn By GB

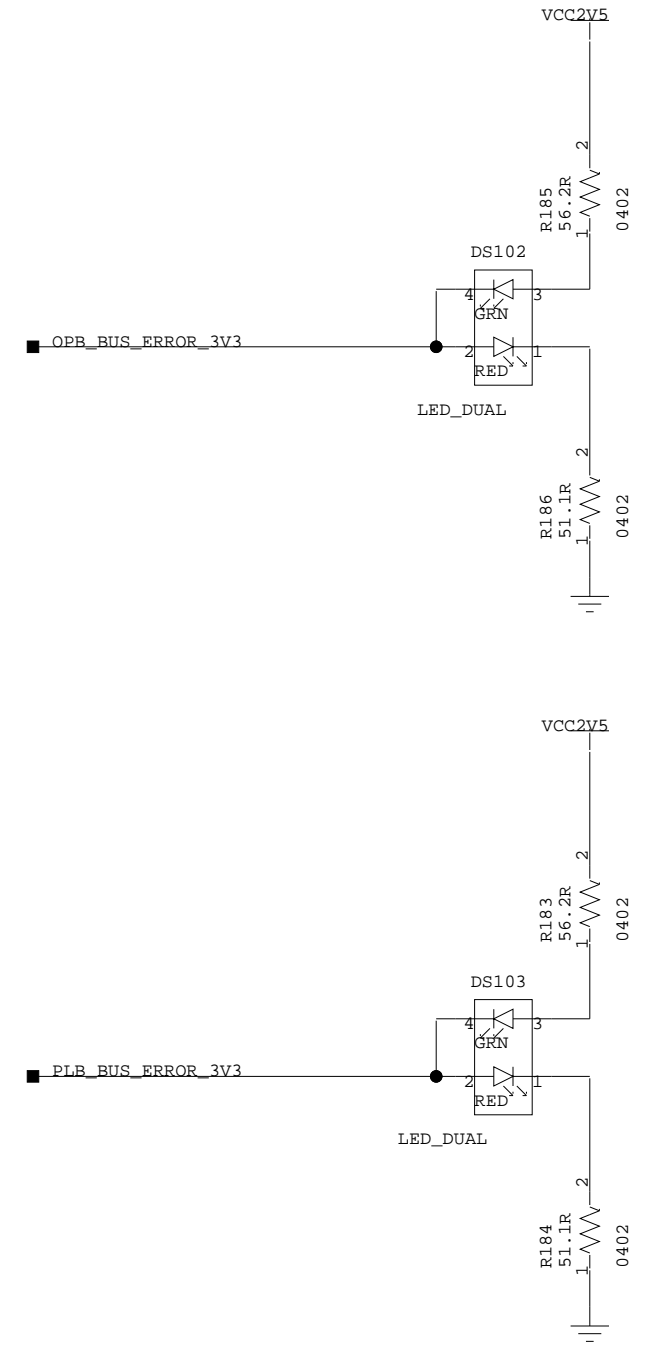
# Illumination LEDs



LED placement on Solder side of board (not X-Ray)



Bus Err	Sys ACE	FPGA
PLB ERR	ERR STAT	INIT DONE
(R/G) (R/G)	(R) (G)	(R) (B)
DS403 DS403	DS403 DS403	DS403 DS403



## ML300 CPU

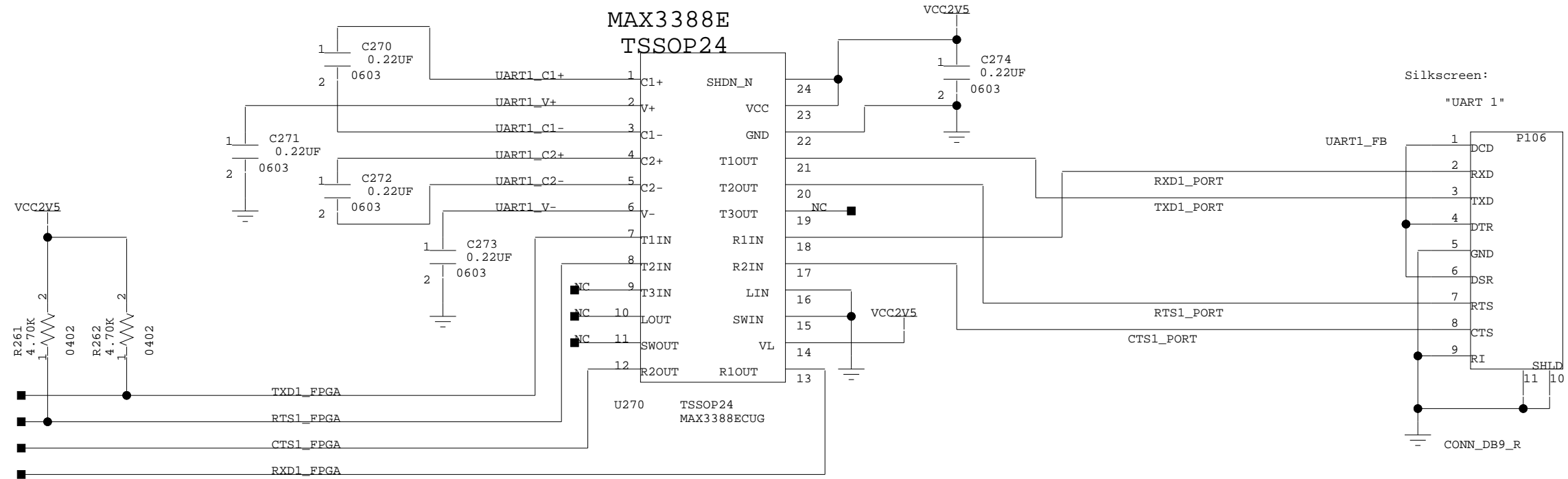
### Illumination LEDs



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU Illumination LEDs	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 35 of 55	Drawn By BP

### MAX3388E TSSOP24

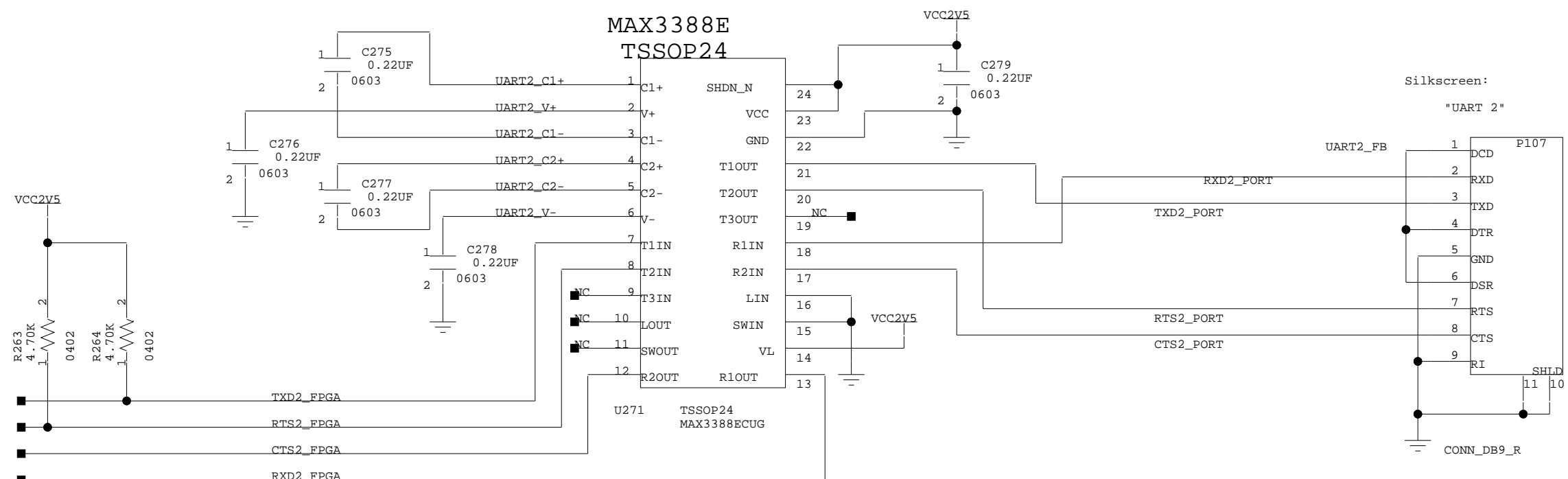


RS232 Host (DTE) Pinout

PIN	NAME	DIR
1	DCD	←
2	RX	←
3	TX	→
4	DTR	→
5	SG	←
6	DSR	←
7	RTS	→
8	CTS	←
9	RI	←

ML300 Cable Side

### MAX3388E TSSOP24



RS232 Host (DTE) Pinout

PIN	NAME	DIR
1	DCD	←
2	RX	←
3	TX	→
4	DTR	→
5	SG	←
6	DSR	←
7	RTS	→
8	CTS	←
9	RI	←

ML300 Cable Side

## ML300 CPU V2P7 Bank 4 (16) Serial Ports

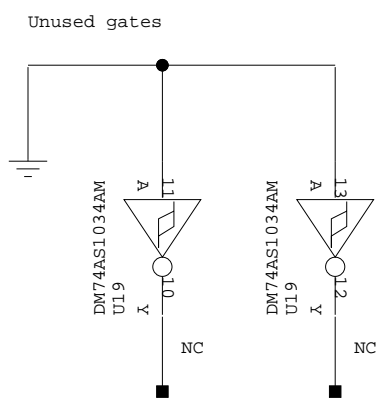
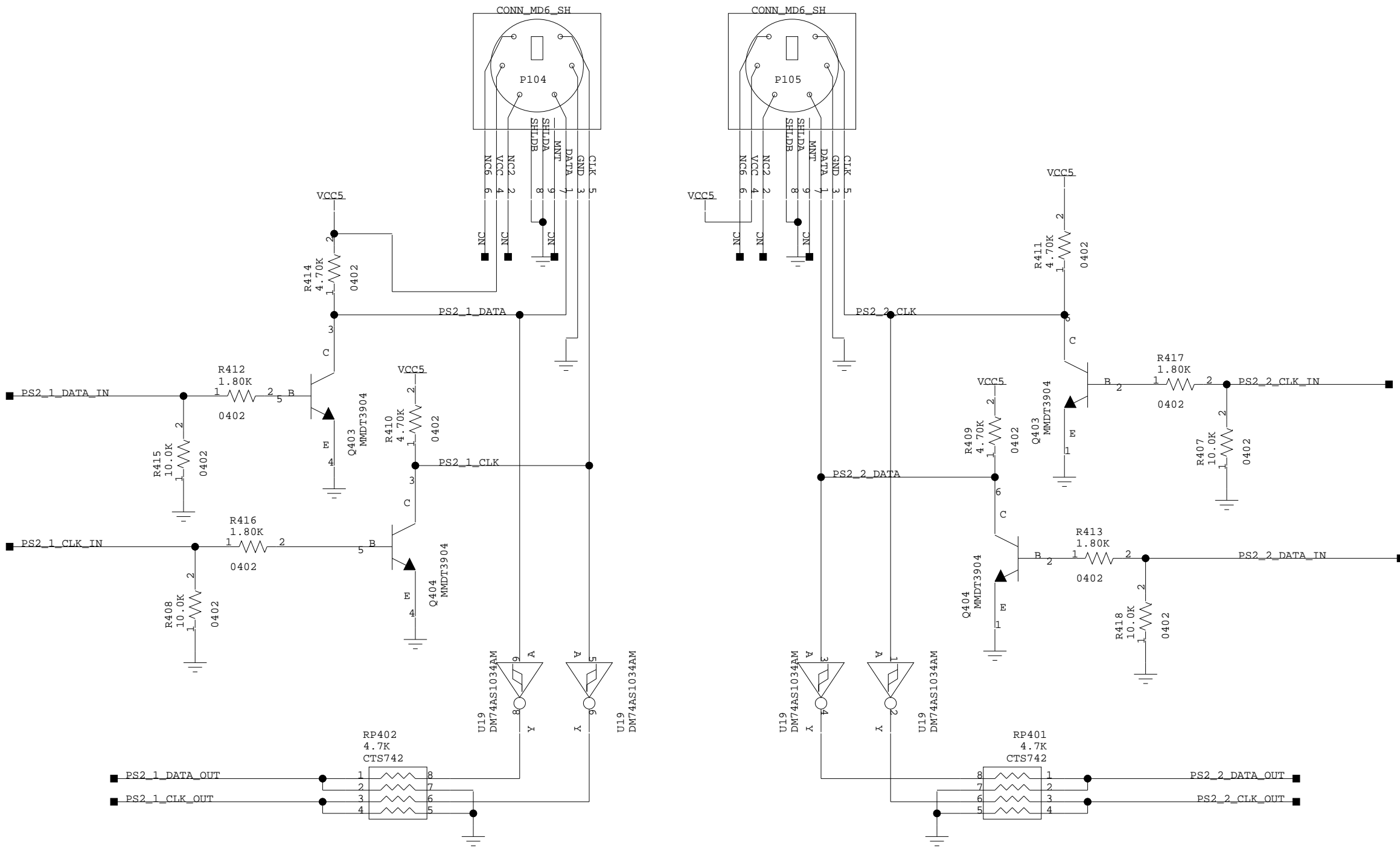


PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU Serial Ports	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 36 of 55	Drawn By BP

Silkscreen:  
"PS2 #1"  
"Mouse"

Silkscreen:  
"PS2 #2"  
"Keyboard"



**PS2 NOTES:**

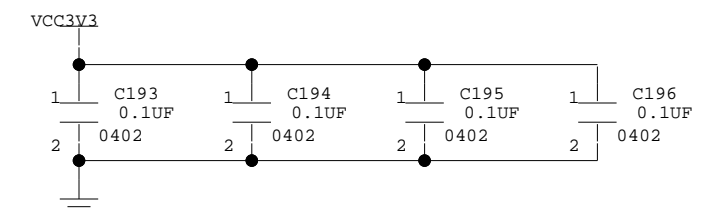
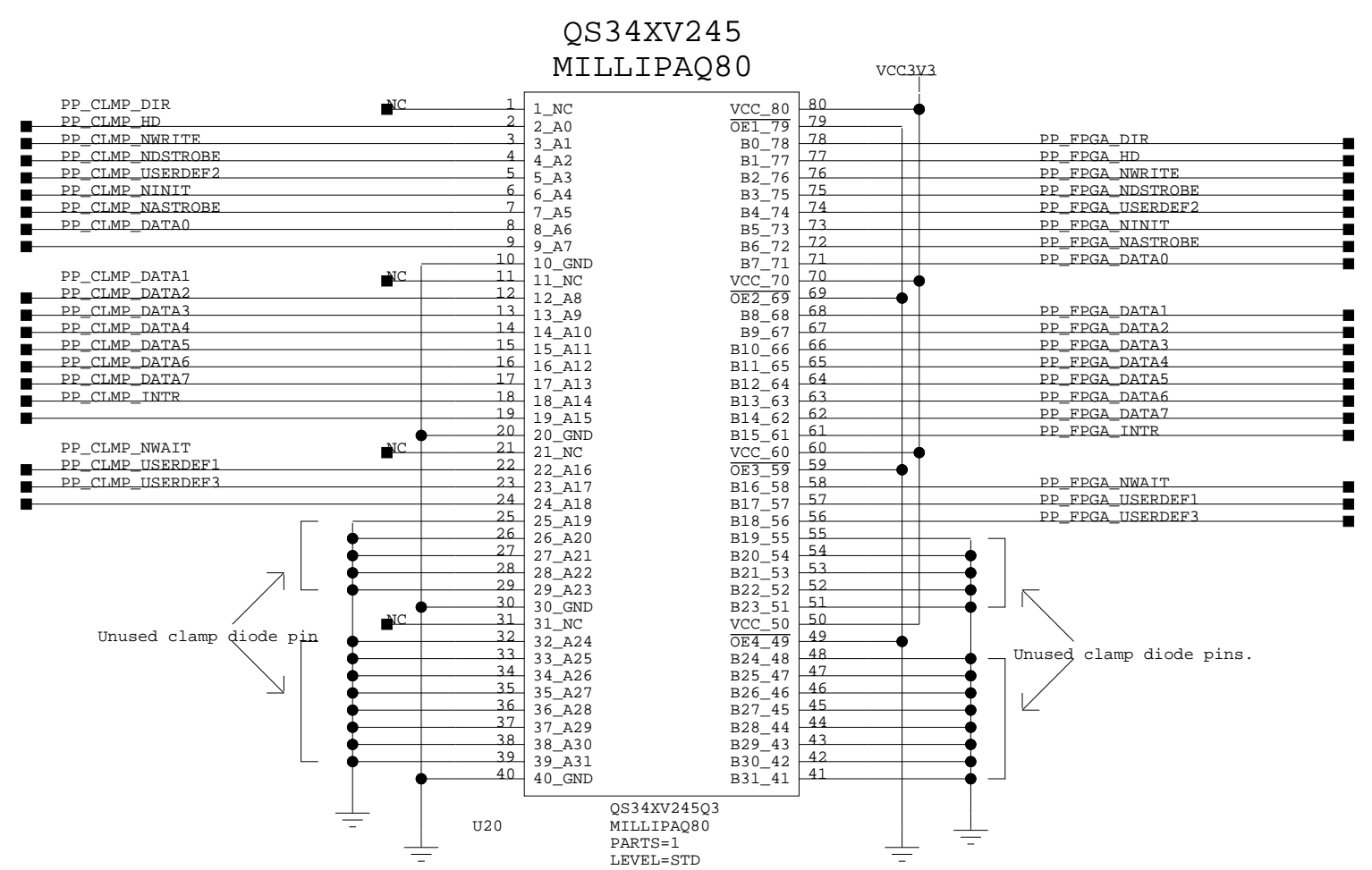
1. PS2 uses open collector. Use NPN transistor to bring the signal up to 5V levels
2. The Signal to the connector is fed back to the FPGA through a voltage divider for signals from peripheral.

ML300 CPU  
V2P7 Bank 0 (12)  
PS/2 Ports



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU PS/2 Ports	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 37 of 55	Drawn By BP



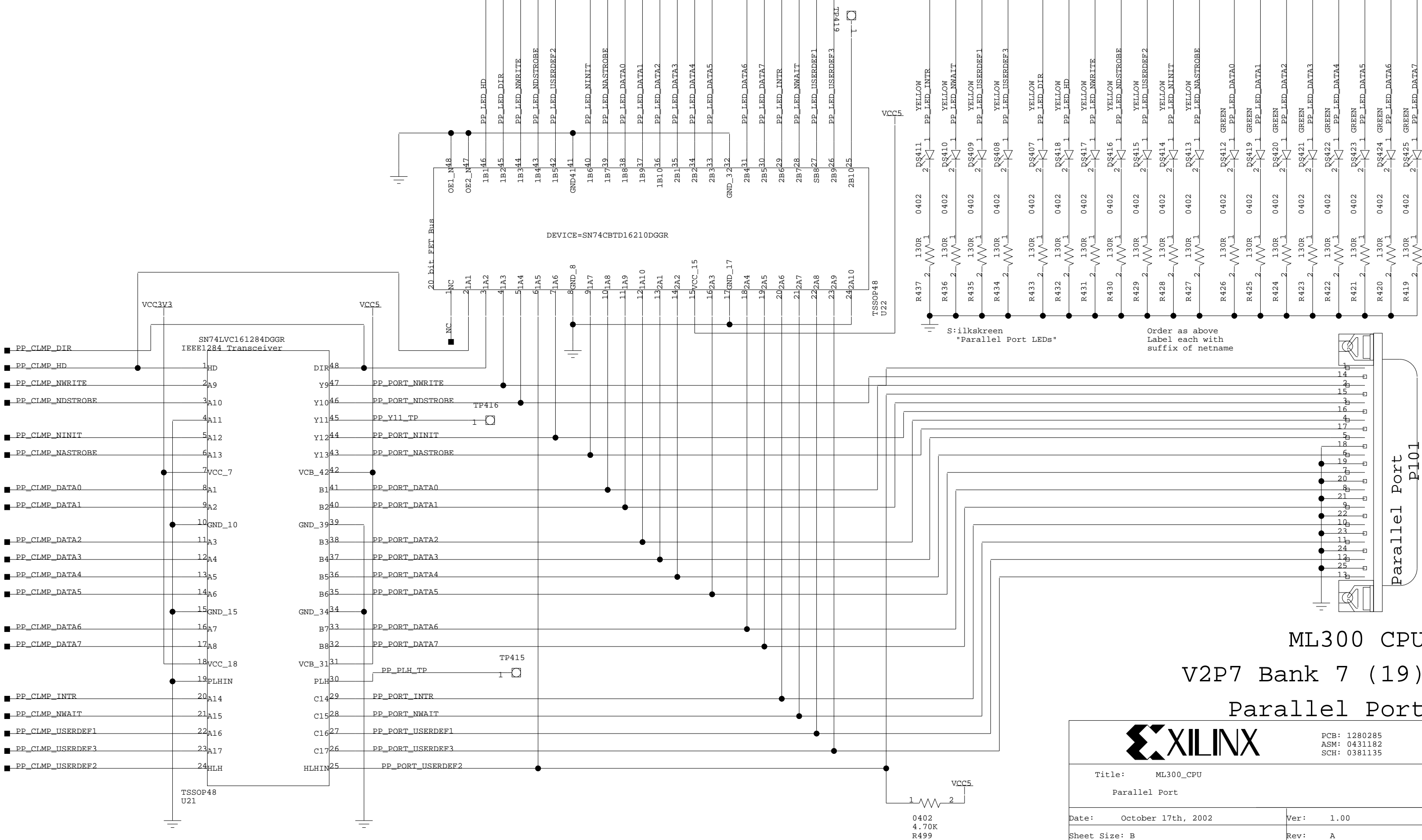
ML300 CPU  
V2P7 Bank 7 (19)  
Parallel Port Level Shifter



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU Parallel Port Level Shifter	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 38 of 55	Drawn By GB

# Parallel Port Level Shifter

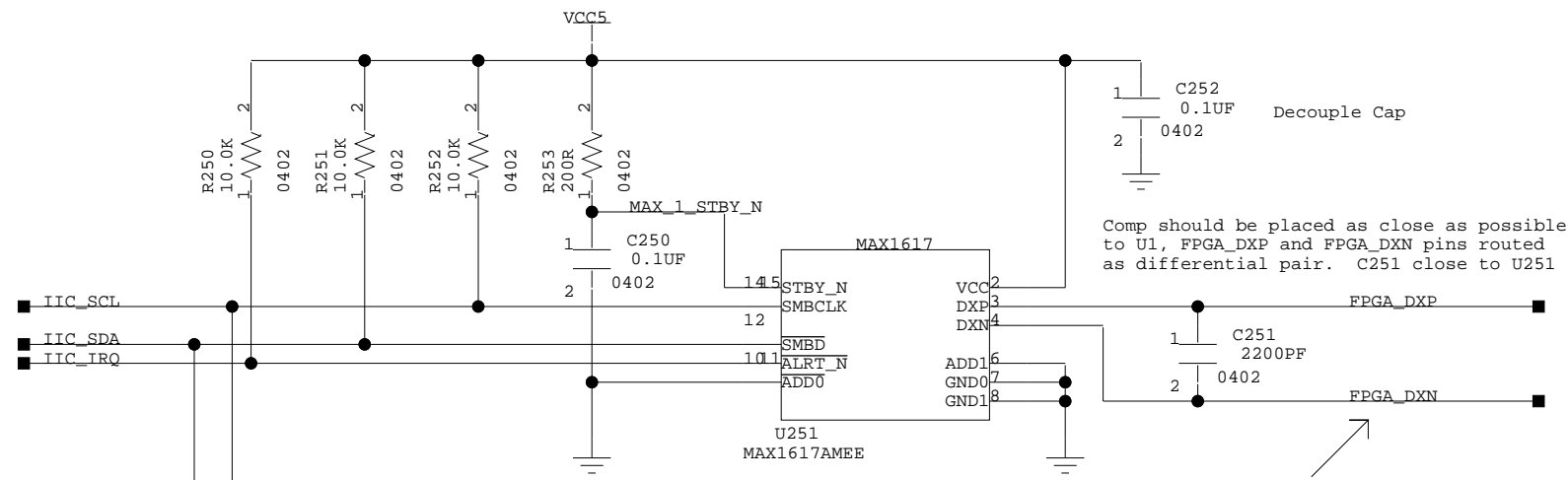


ML300 CPU  
V2P7 Bank 7 (19)  
Parallel Port



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

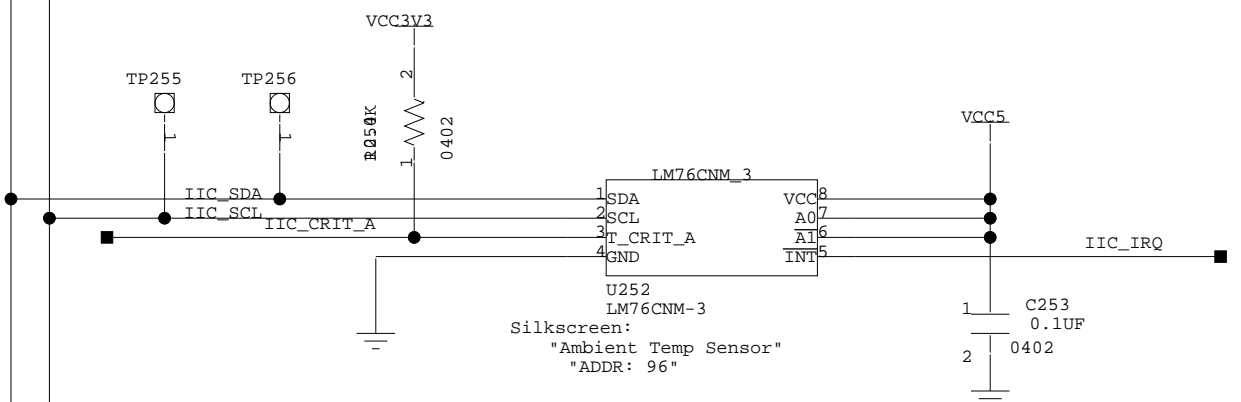
Title: ML300_CPU Parallel Port	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 39 of 55	Drawn By BP



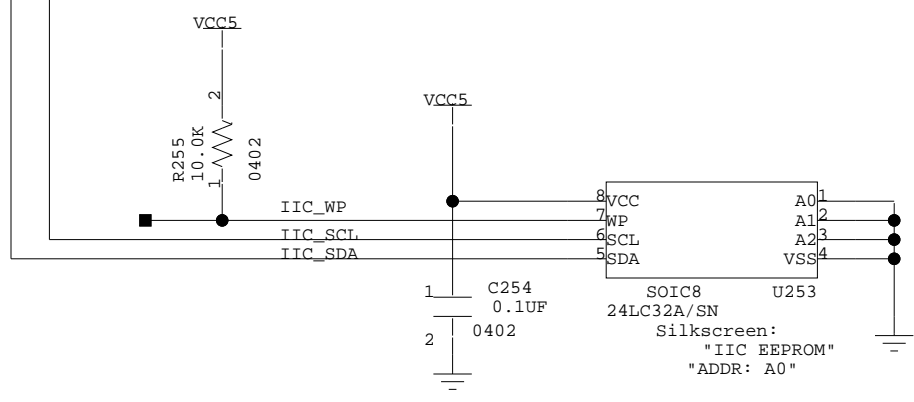
Silkscreen:  
"FPGA Temp Sensor"  
"ADDR: 30"

Comp should be placed as close as possible to U1, FPGA\_DXP and FPGA\_DNX pins routed as differential pair. C251 close to U251

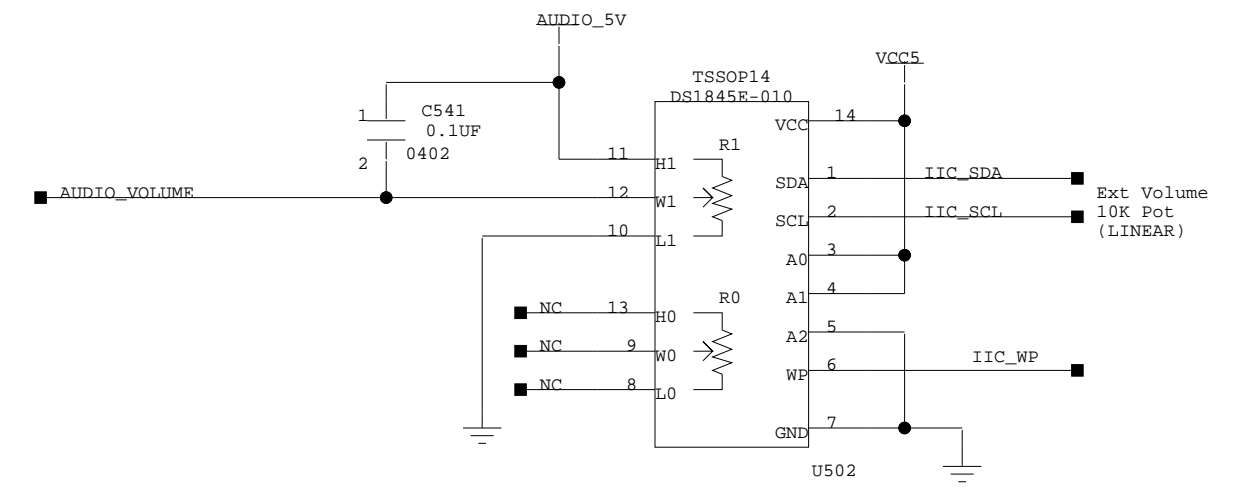
These signals (FPGA\_DXP, FPGA\_DNX) should be routed as differential signals, and isolated from other signals as much as possible



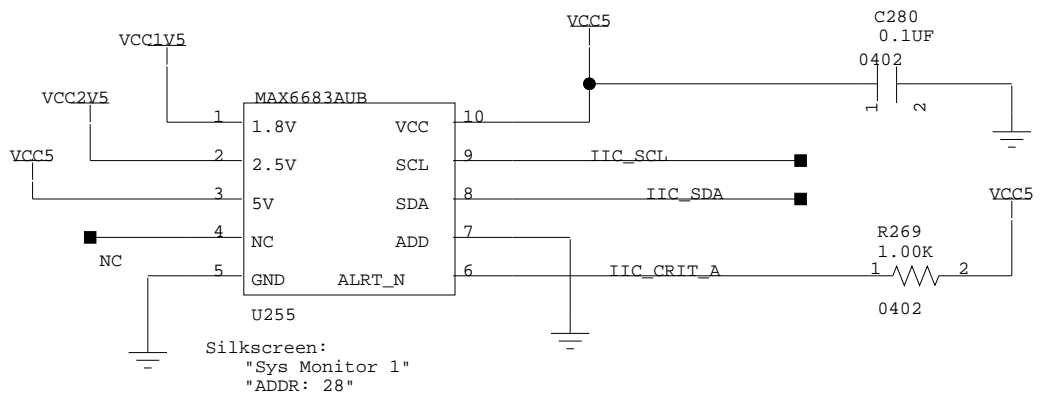
Silkscreen:  
"Ambient Temp Sensor"  
"ADDR: 96"



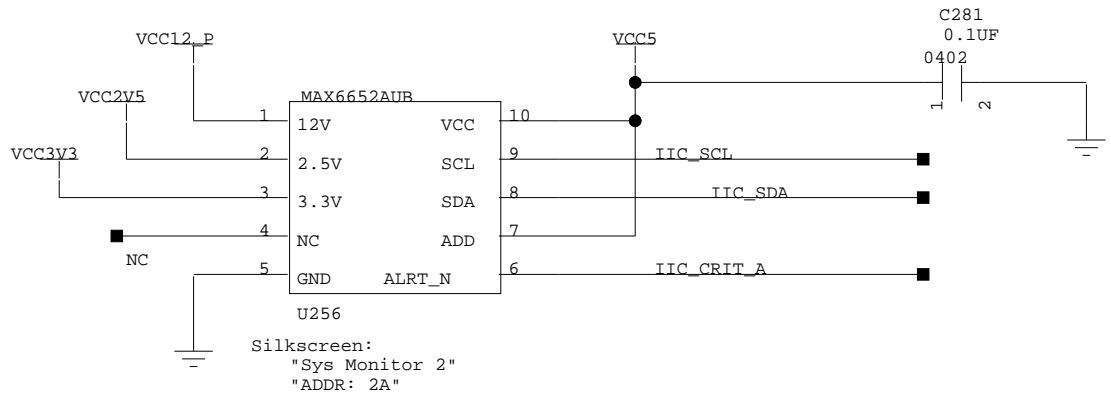
Silkscreen:  
"IIC EEPROM"  
"ADDR: A0"



Silkscreen:  
"Audio Trimpot"  
"ADDR: A6"



Silkscreen:  
"Sys Monitor 1"  
"ADDR: 28"



Silkscreen:  
"Sys Monitor 2"  
"ADDR: 2A"

IC	BOARD	REF	DESCRIPTION	ADDR
MAX6683AUB	ML300_CPU	U255	System Monitor 1	28/29
MAX6652AUB	ML300_CPU	U256	System Monitor 2	2A/2B
MAX6652AUB	ML300_PWR_IO	U4	System Monitor 4	2E/2F
MAX6683AUB	ML300_PWR_IO	U2	System Monitor 3	2C/2D
MAX1617	ML300_CPU	U251	FPGA Die/Ambient Temp	30/31
LM76C32A/SN	ML300_CPU	U252	Ambient Temp	96/97
24LC32A/SN	ML300_CPU	U253	32Kbit EEPROM	A0/A1
DS1845E-010	ML300_CPU	U502	Audio Trimpot	A6/A7
DS1845E-010	ML300_PWR_IO	U3	TFT Touchscreen Trimpot	AC/AD
X1226S8	ML300_PWR_IO	U24	Real Time Clock 4Kbit EEPROM	AE/AF
X1226S8	ML300_PWR_IO	U24	Real Time Clock RTC	DE/DF

**NOTES:**

1. The IIC Bus has devices on both the CPU and PWR\_IO boards.

ML300 CPU  
Bank 3 (15) - IIC Bus



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

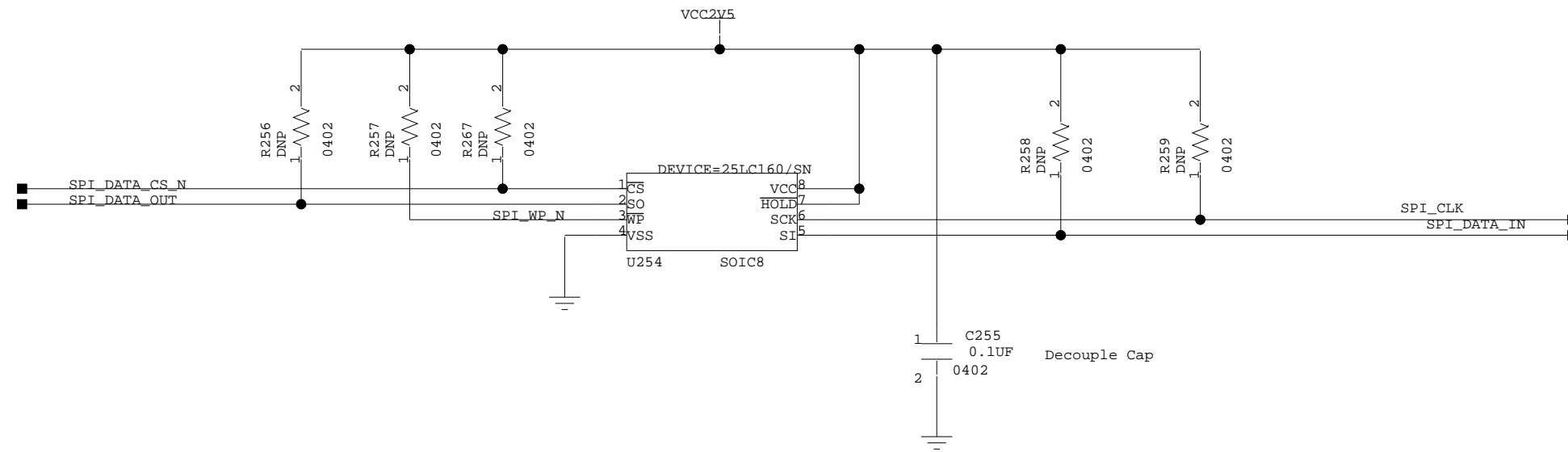
Title: ML300\_CPU

IIC Bus

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 40 of 56	Drawn By BP



# SPI ROM 2.5V- 5.5V



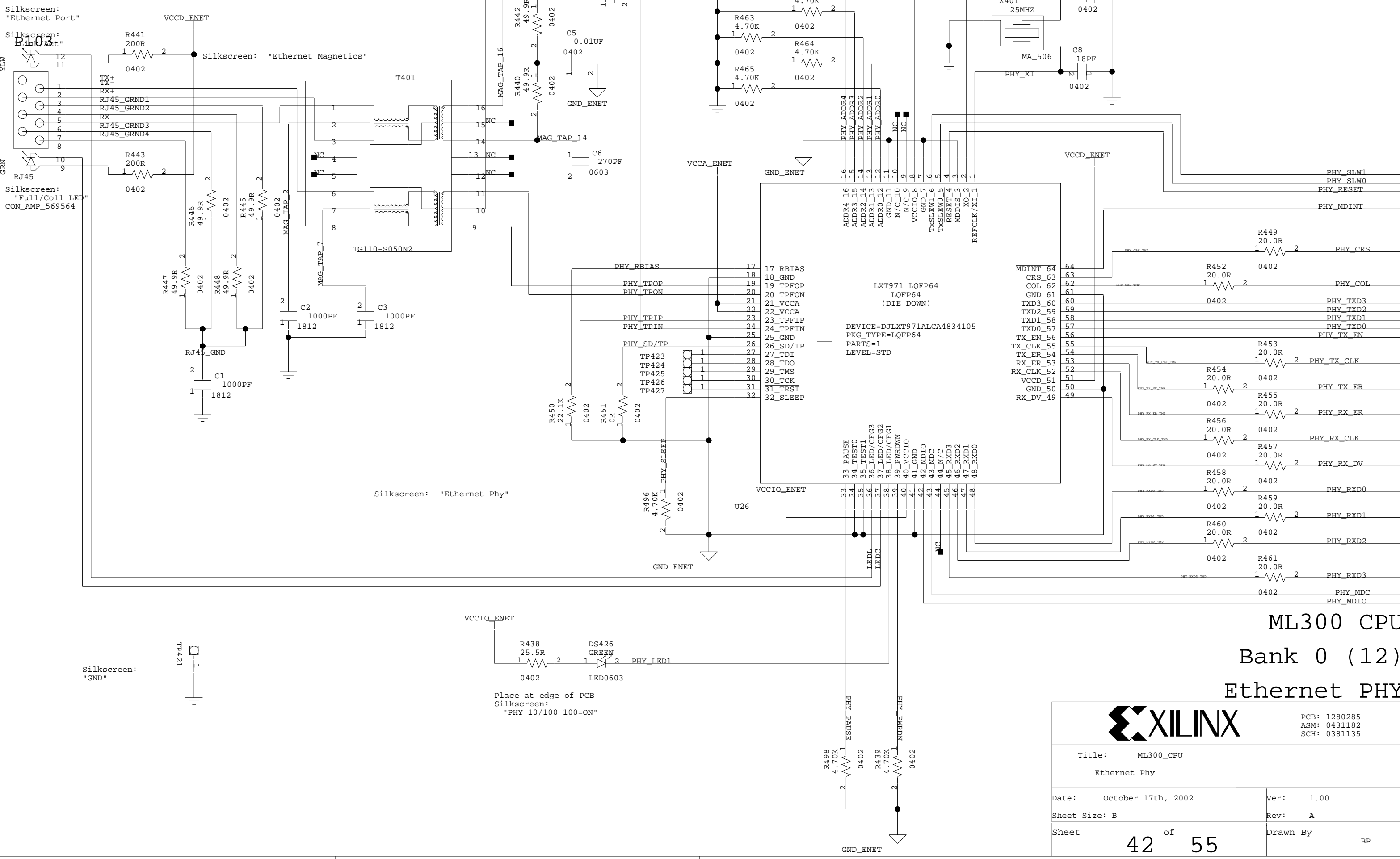
ML300 CPU  
Bank 4 (16)  
SPI



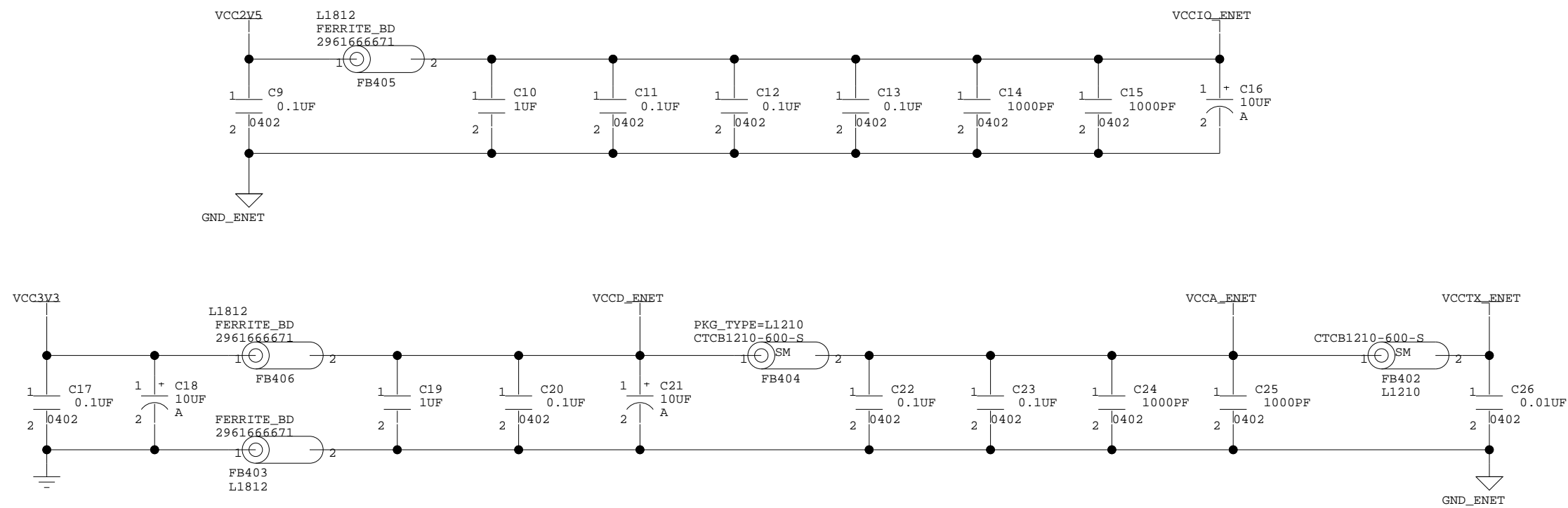
PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU SPI Bus	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 41 of 55	Drawn By BP

Connector is bottom view



		PCB: 1280285 ASM: 0431182 SCH: 0381135
Title: ML300_CPU Ethernet Phy		
Date: October 17th, 2002	Ver: 1.00	
Sheet Size: B	Rev: A	
Sheet 42 of 55	Drawn By BP	



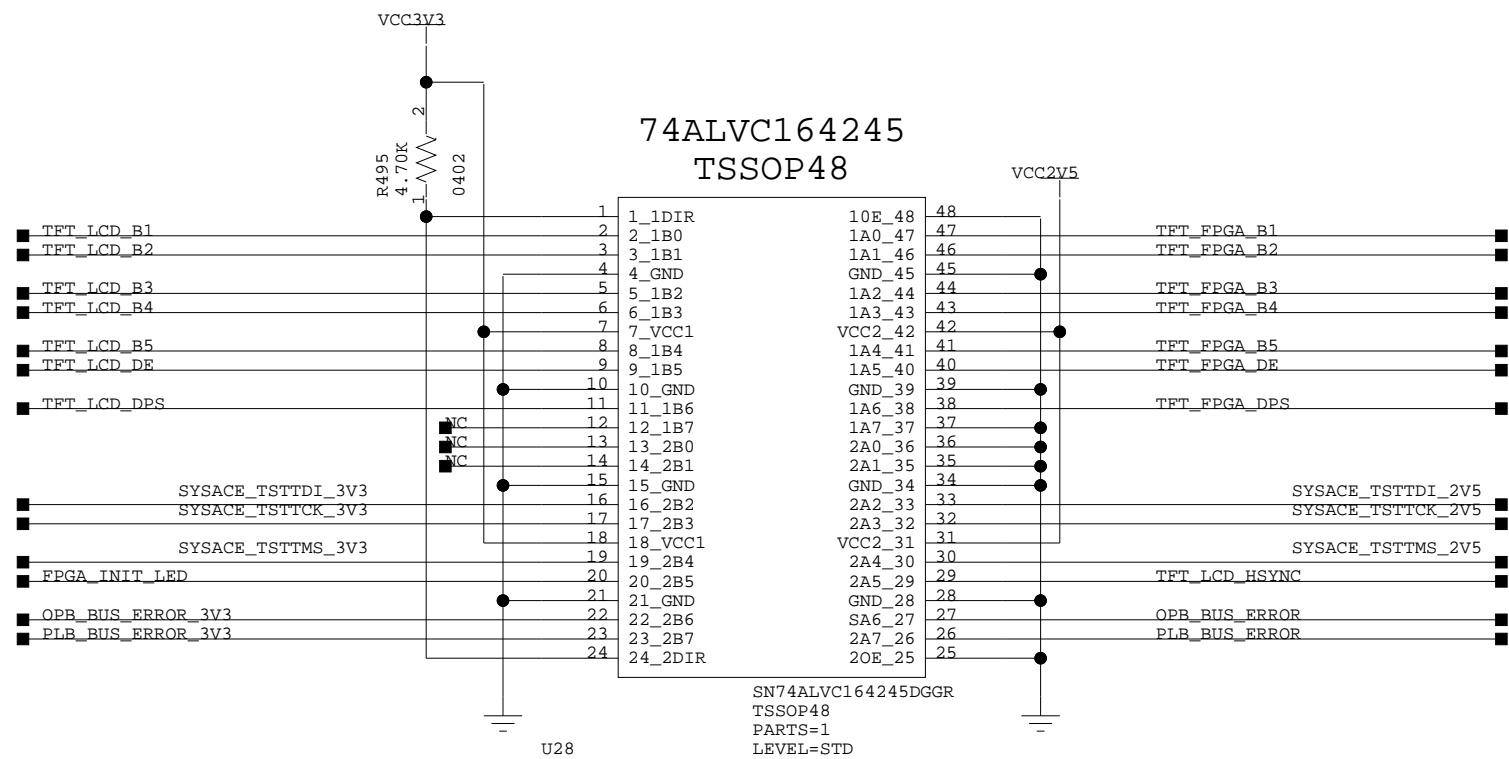
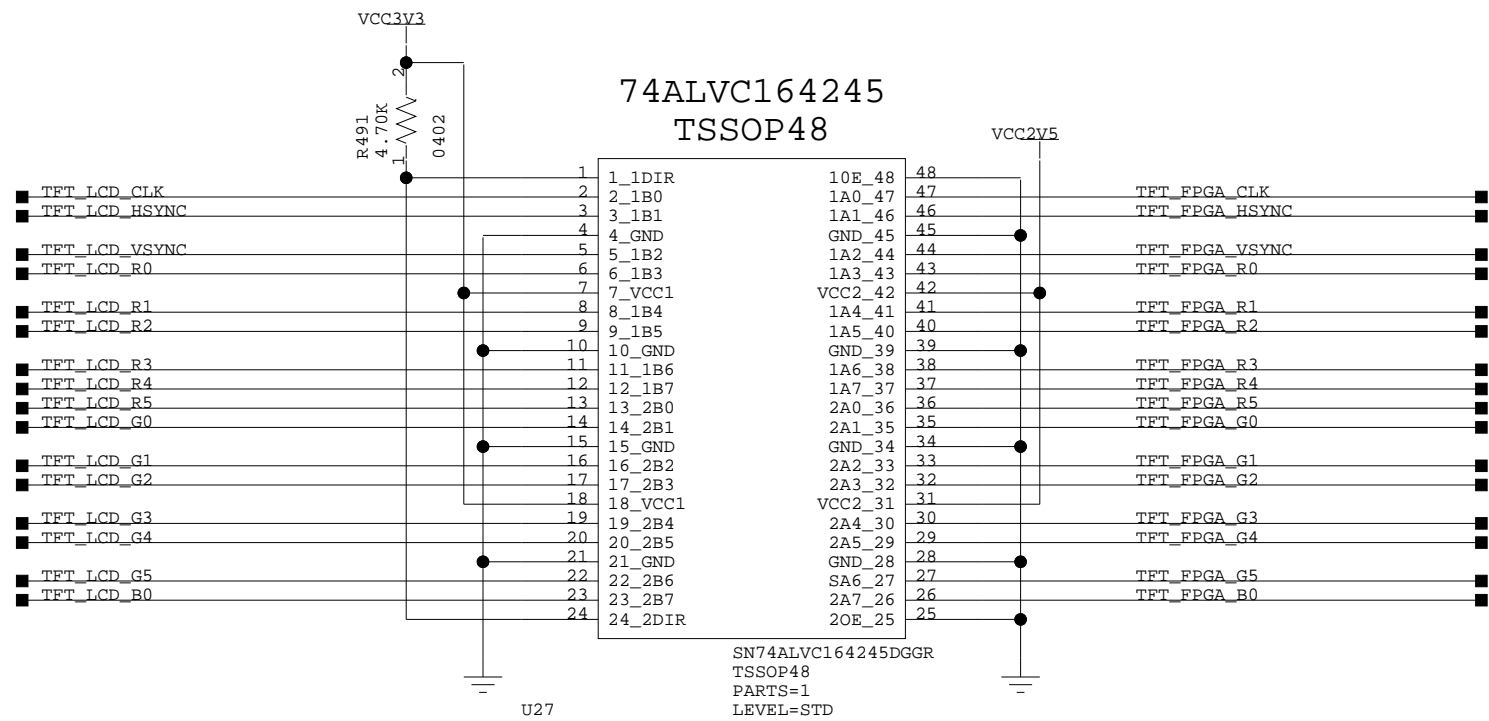
# ML300 CPU Ethernet Power Filter



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU Ethernet Power	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 43 of 55	Drawn By BP

LCD Level Shifters - 2.5V to 3.3V



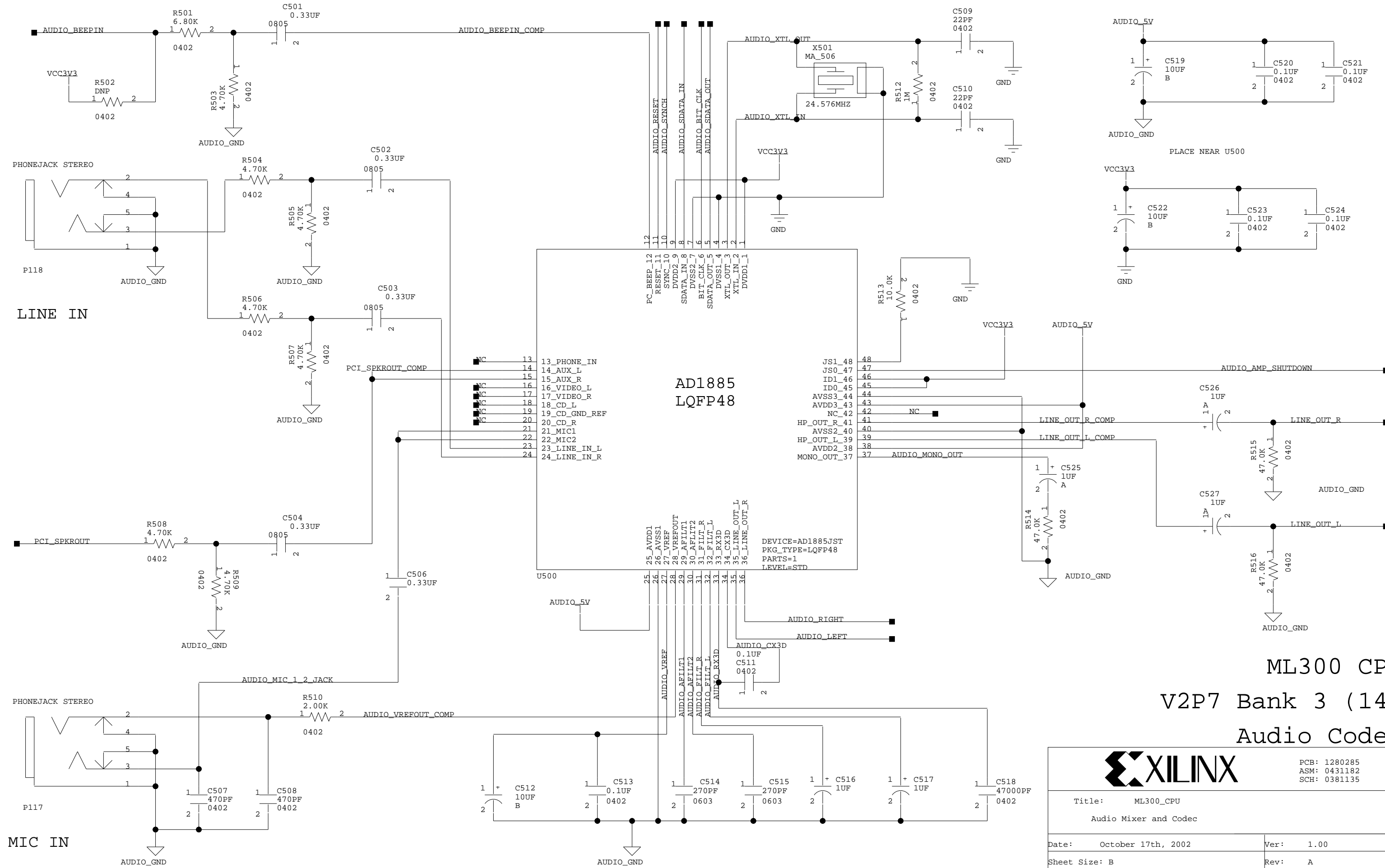
ML300 CPU  
V2P7 Bank 4 (16)  
TFT LCD



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300\_CPU  
TFT LCD - Level Shifter and Conn

Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 44 of 55	Drawn By BP



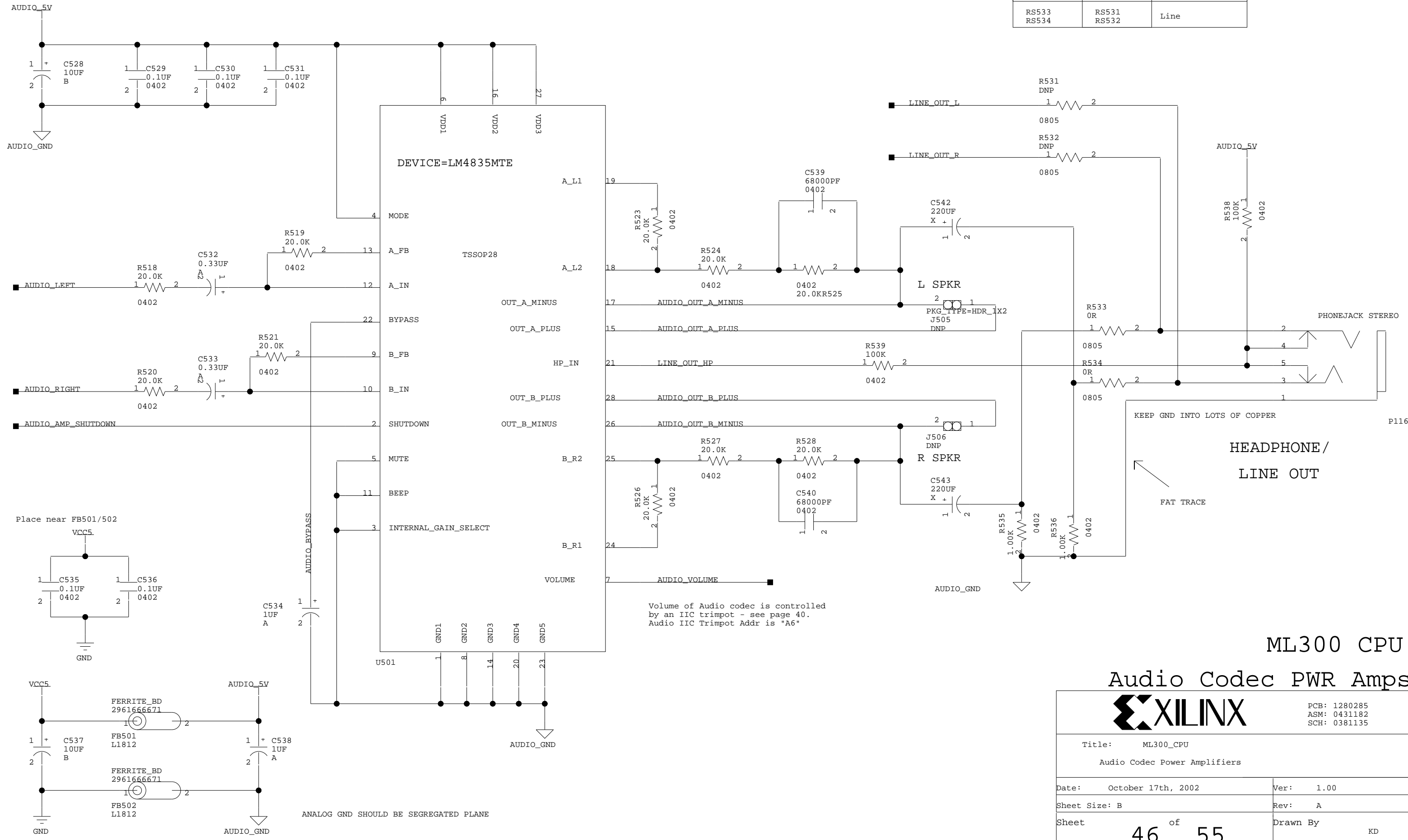
ML300 CPU  
V2P7 Bank 3 (14)  
Audio Codec



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU Audio Mixer and Codec	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 45 of 55	Drawn By KD

Rs Out	Rs In	Function
RS531 RS532	RS533 RS534	Headphone (Default)
RS533 RS534	RS531 RS532	Line



Volume of Audio codec is controlled by an IIC trimpot - see page 40. Audio IIC Trimpot Addr is "A6"

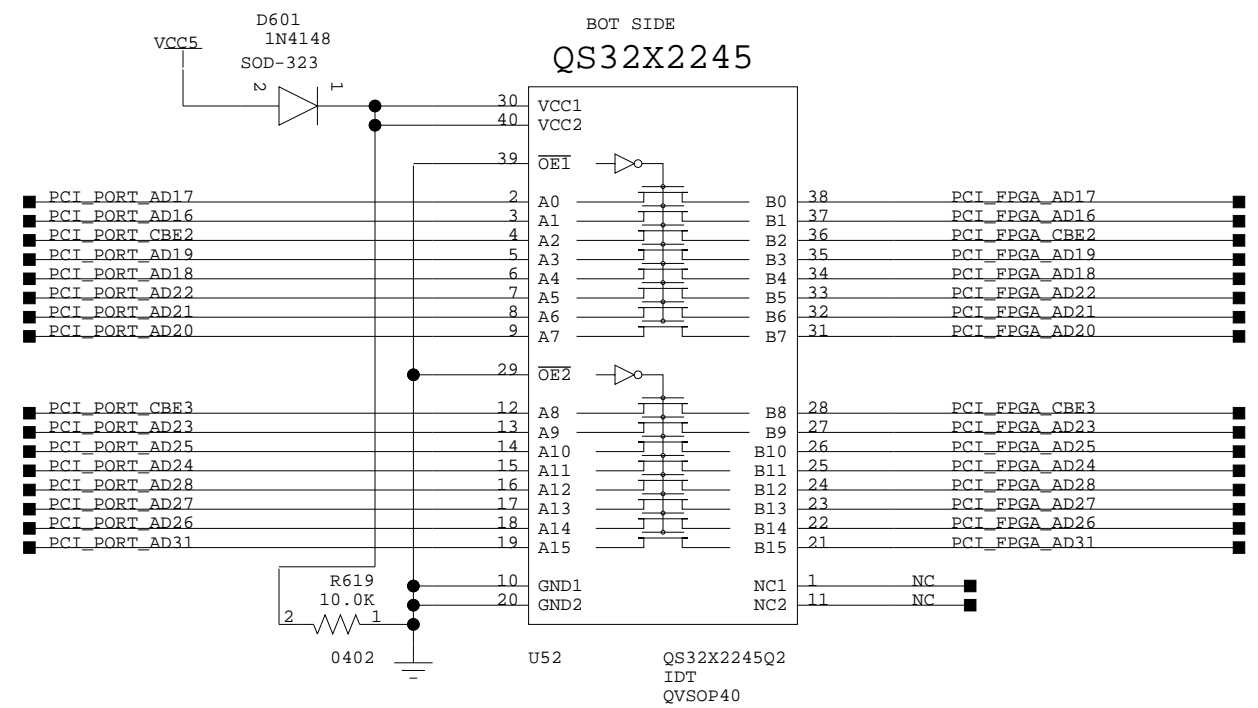
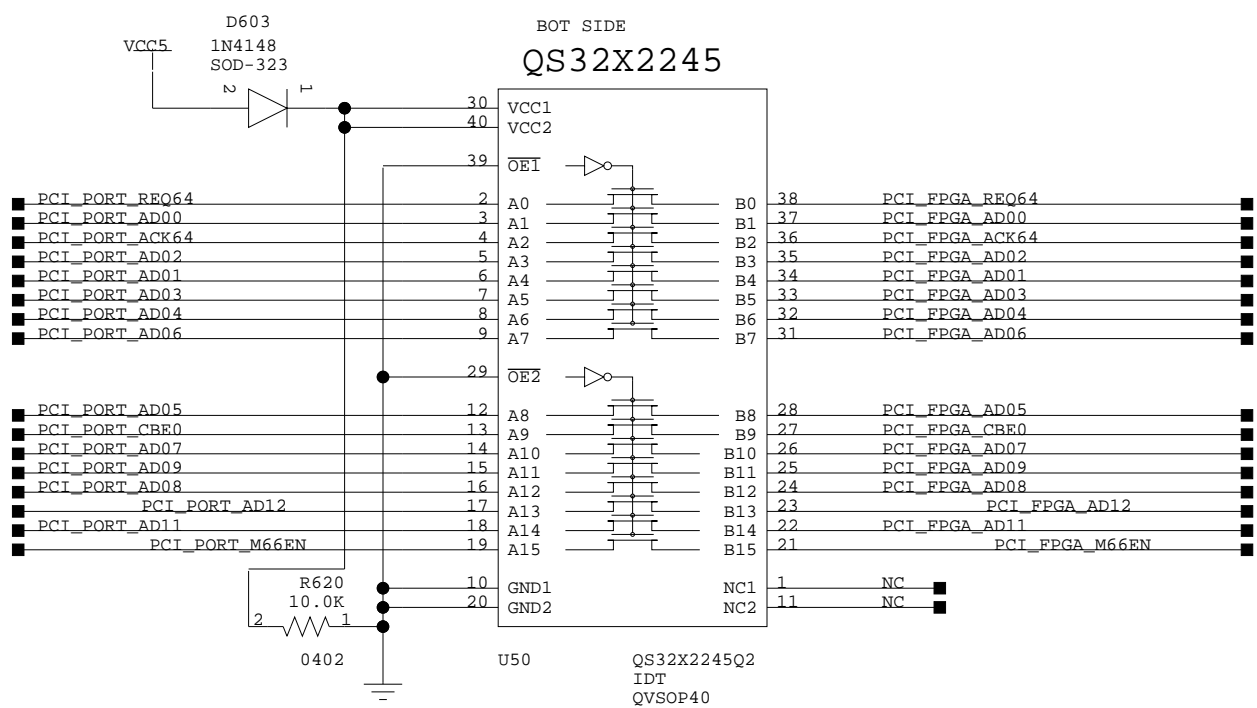
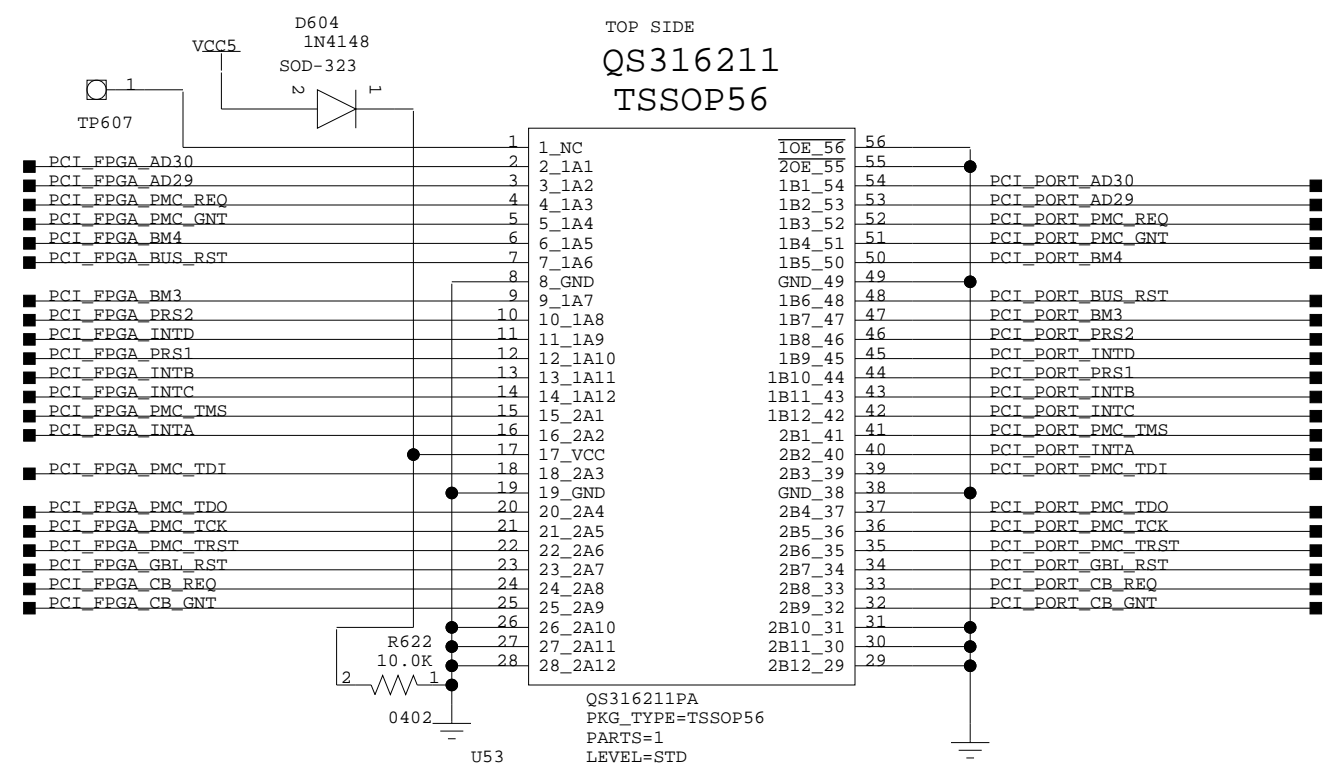
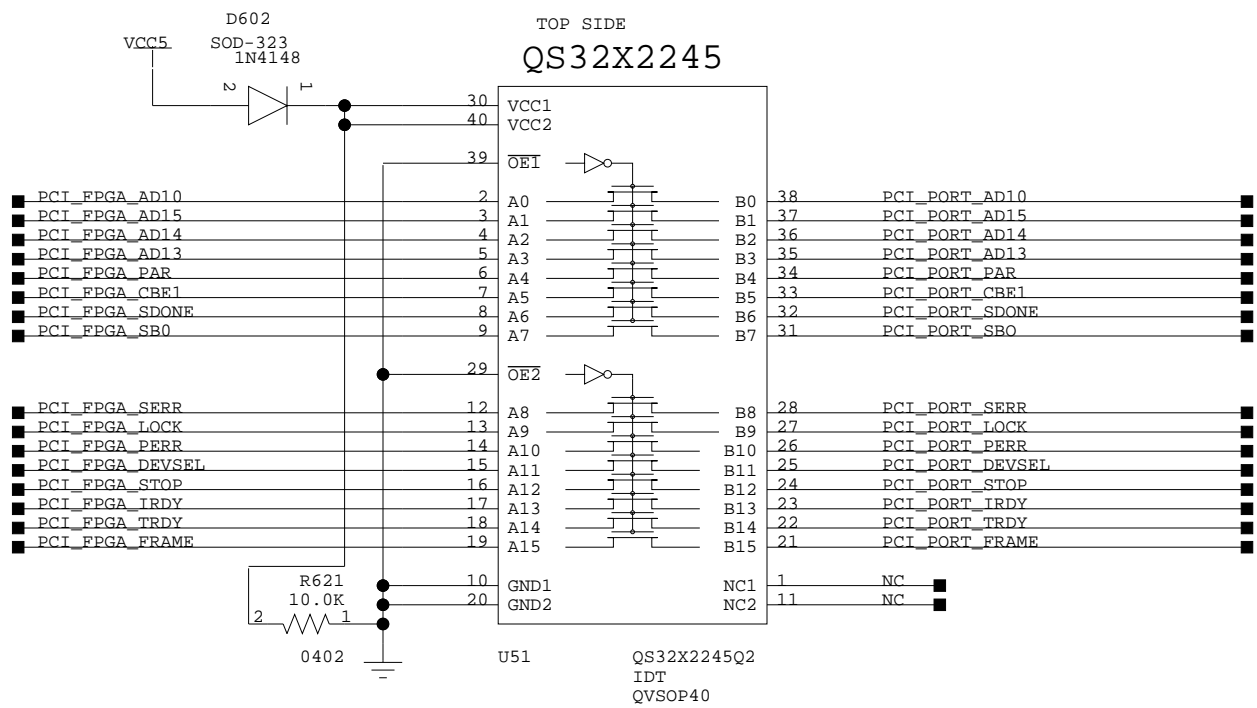
# ML300 CPU Audio Codec PWR Amps



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU Audio Codec Power Amplifiers	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 46 of 55	Drawn By KD

ANALOG GND SHOULD BE SEGREGATED PLANE

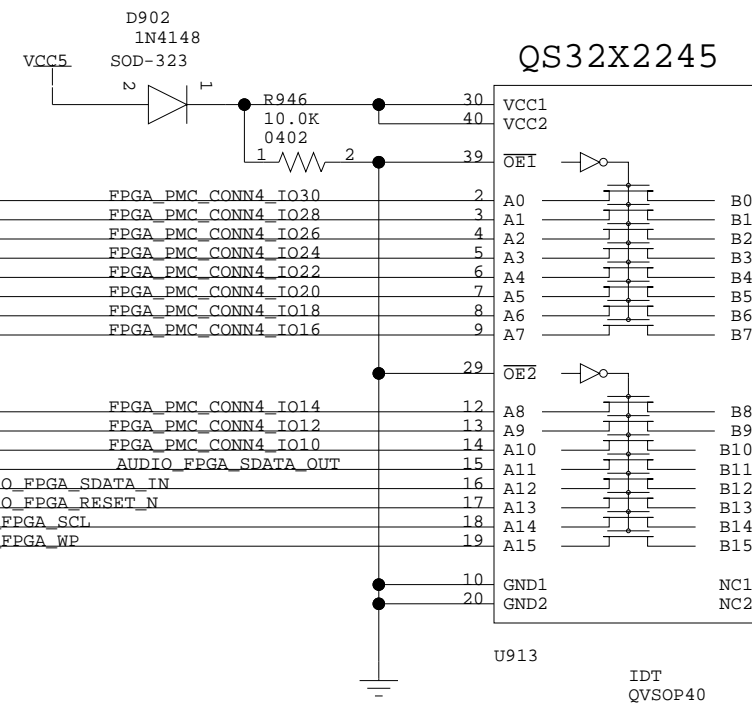


ML300 CPU  
Bank 2/3 (14/15)  
PCI Clamps

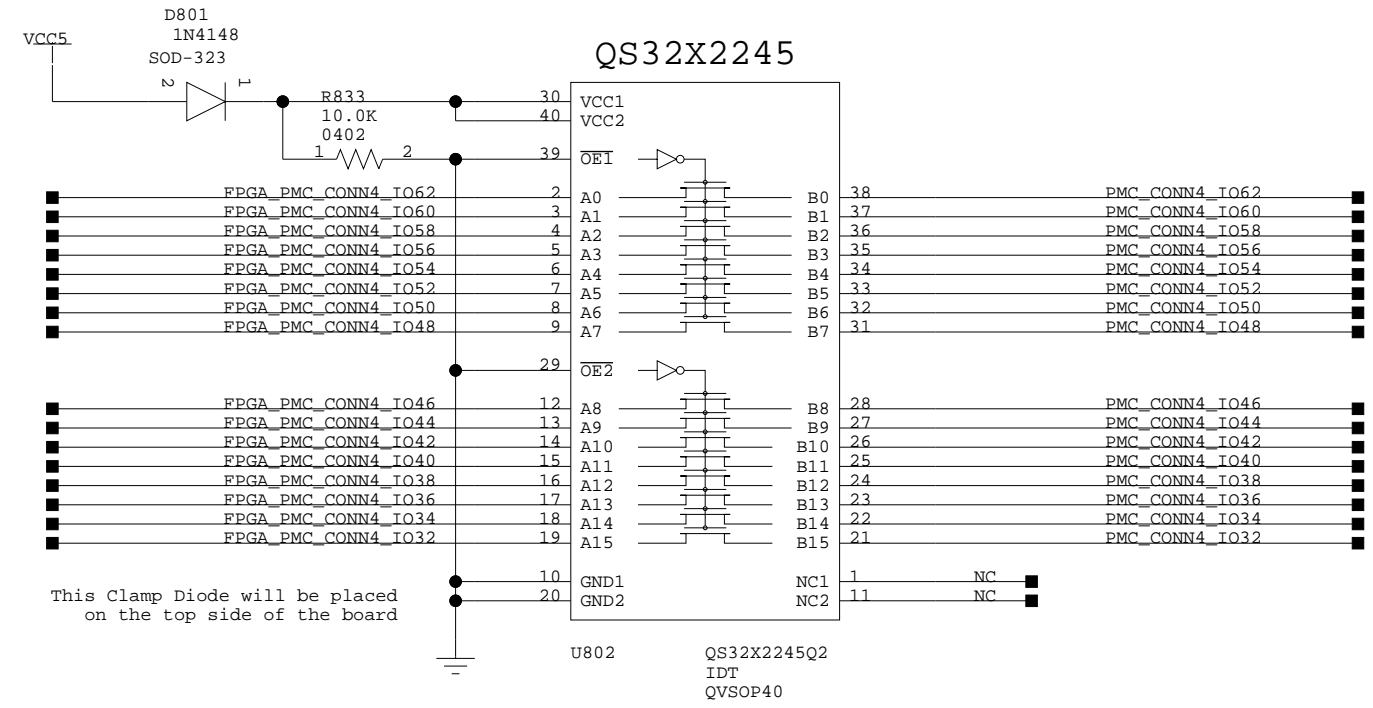


PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU PCI Clamp Diodes for 5V Compliance	
Date: 04th, 2002	Ver: 0.90
Sheet Size: B	Rev: A
Sheet 47 of 55	Drawn By BP/GB

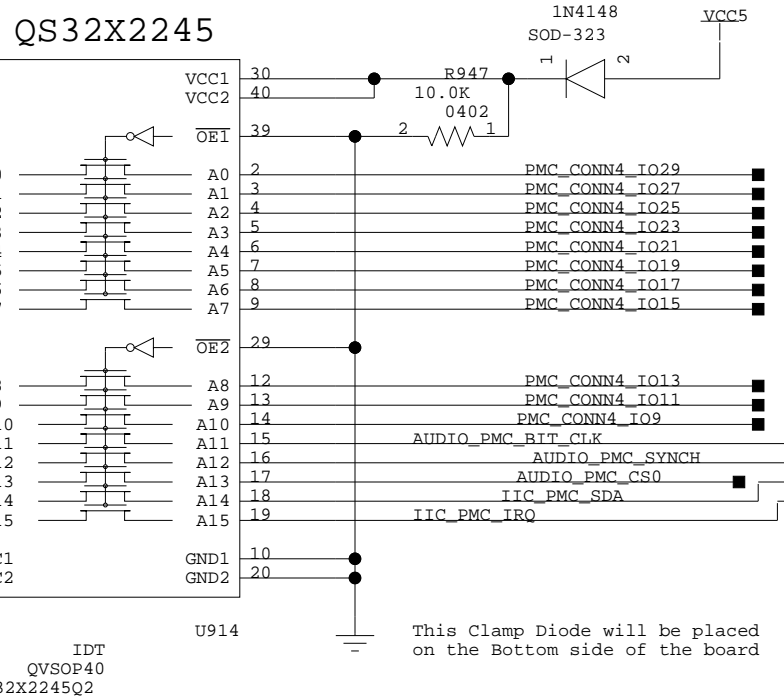


U913 IDT QVSOP40  
This Clamp Diode will be placed on the top side of the board

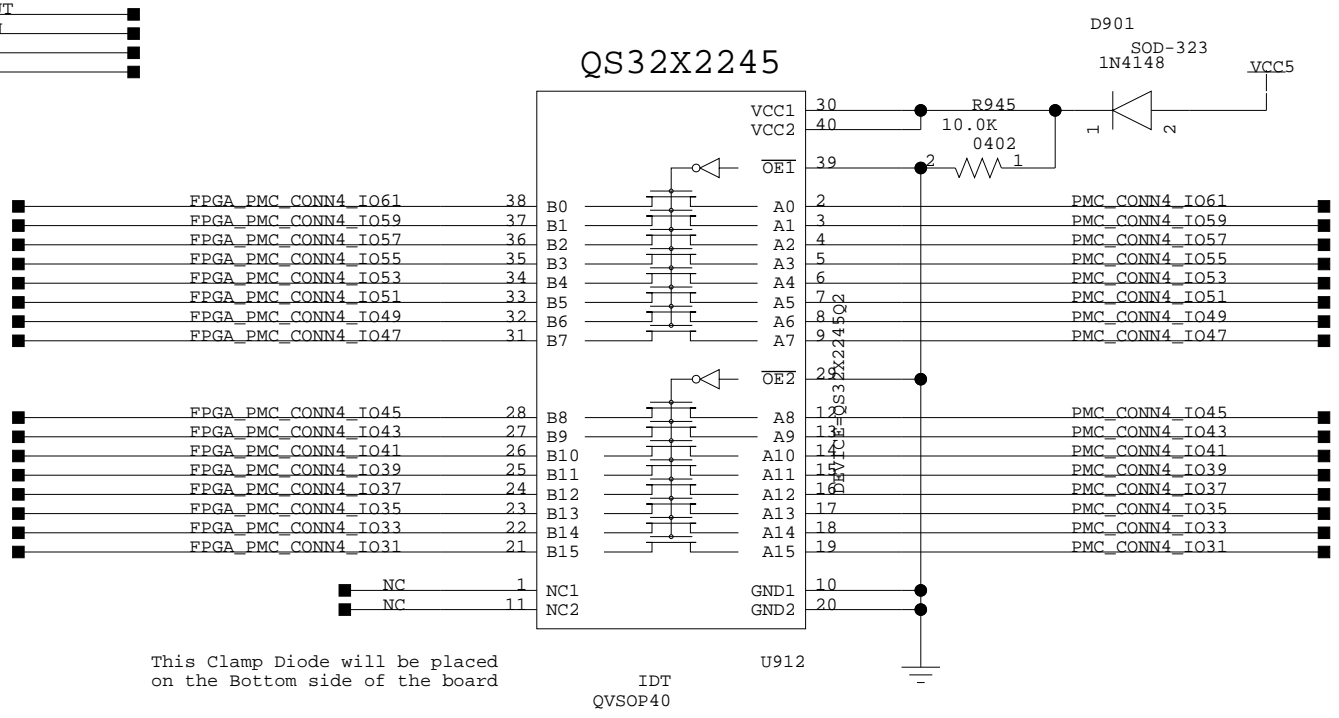


This Clamp Diode will be placed on the top side of the board

U802 QS32X2245Q2 IDT QVSOP40



U914 IDT QVSOP40 QS32X2245Q2  
This Clamp Diode will be placed on the Bottom side of the board



This Clamp Diode will be placed on the Bottom side of the board

U912 IDT QVSOP40

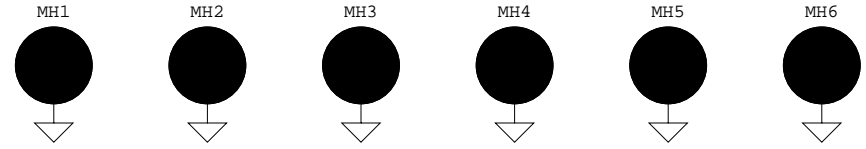
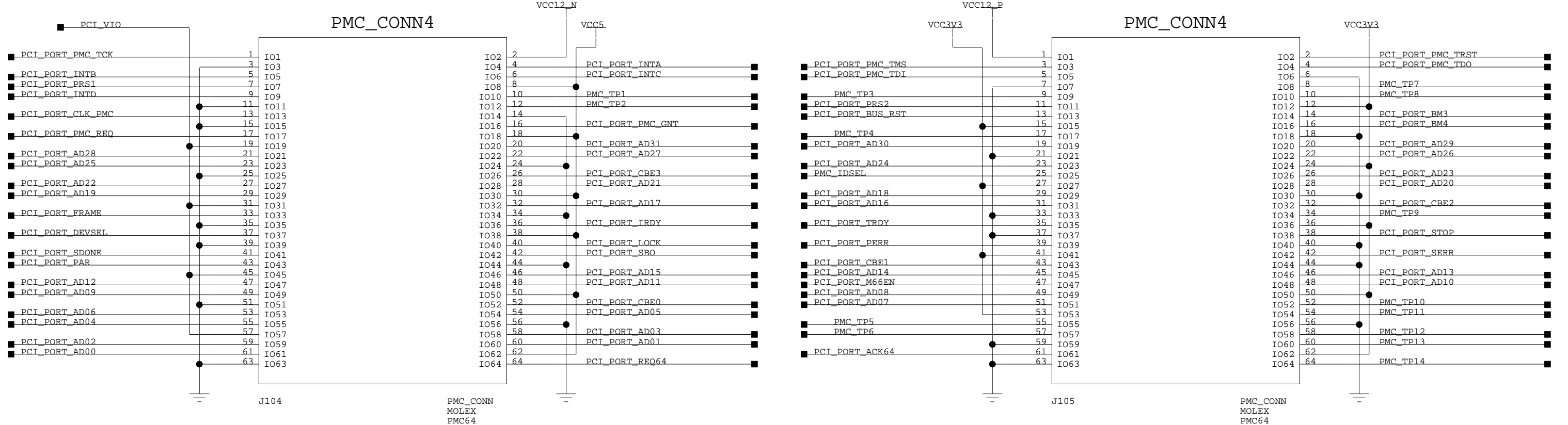
ML300 CPU  
Bank 2/3 (14/15)  
PMC Clamps



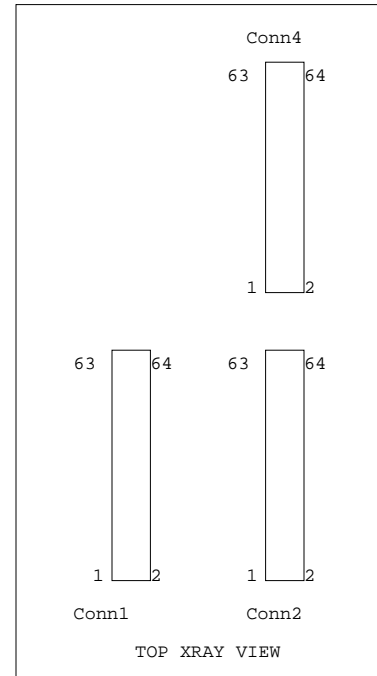
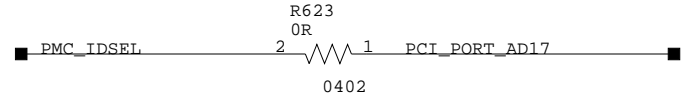
PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU Clamp Diodes for PMC	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 48 of 55	Drawn By BP

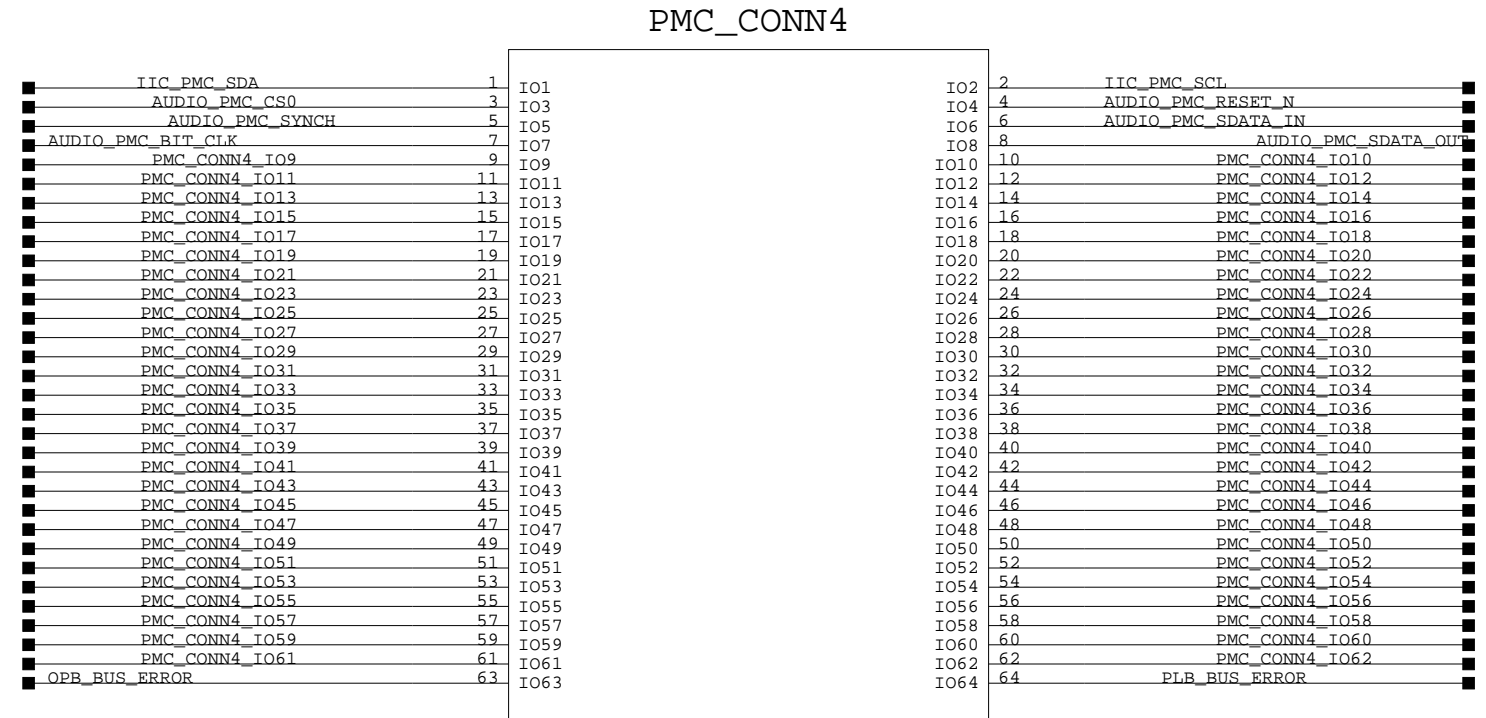




PMC Mounting Holes



PMC\_CONN4\_IO61 should be used as a clock if clocking is needed for PMC\_CONN4



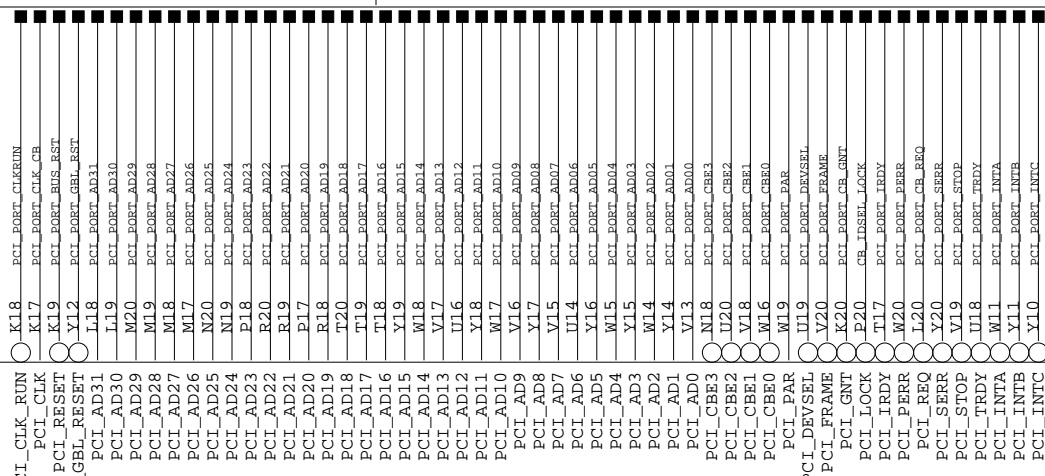
J106 PMC\_CONN MOLEX PMC64

ML300 CPU  
Bank 1/2 (13/14)  
PMC Connectors



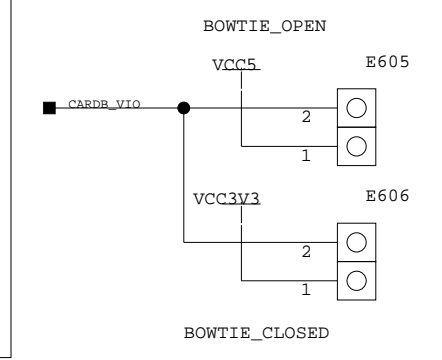
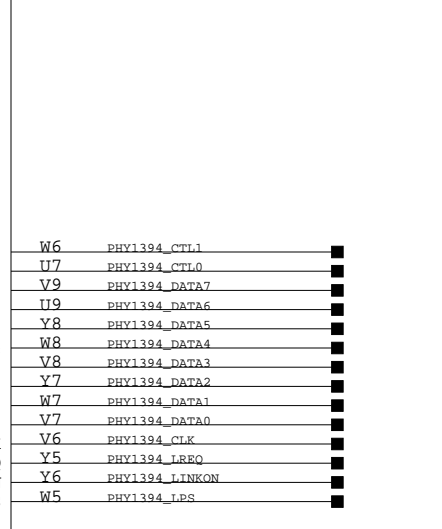
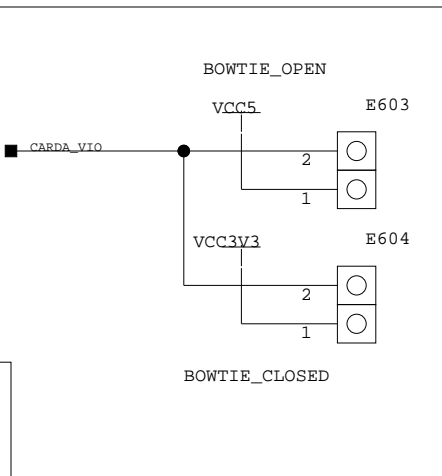
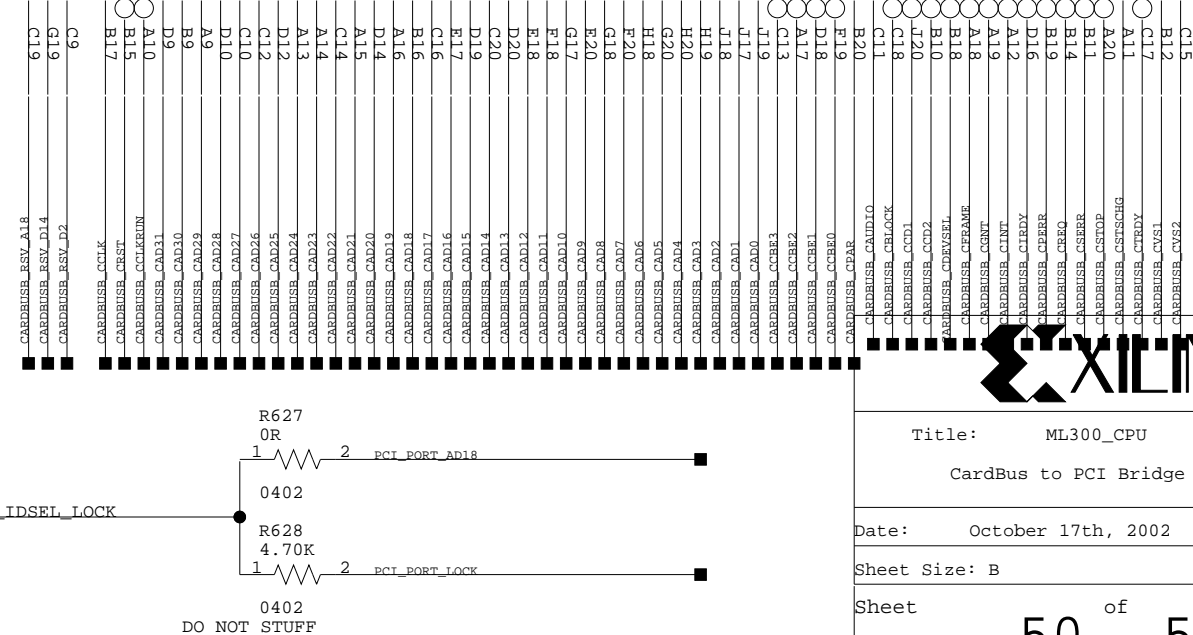
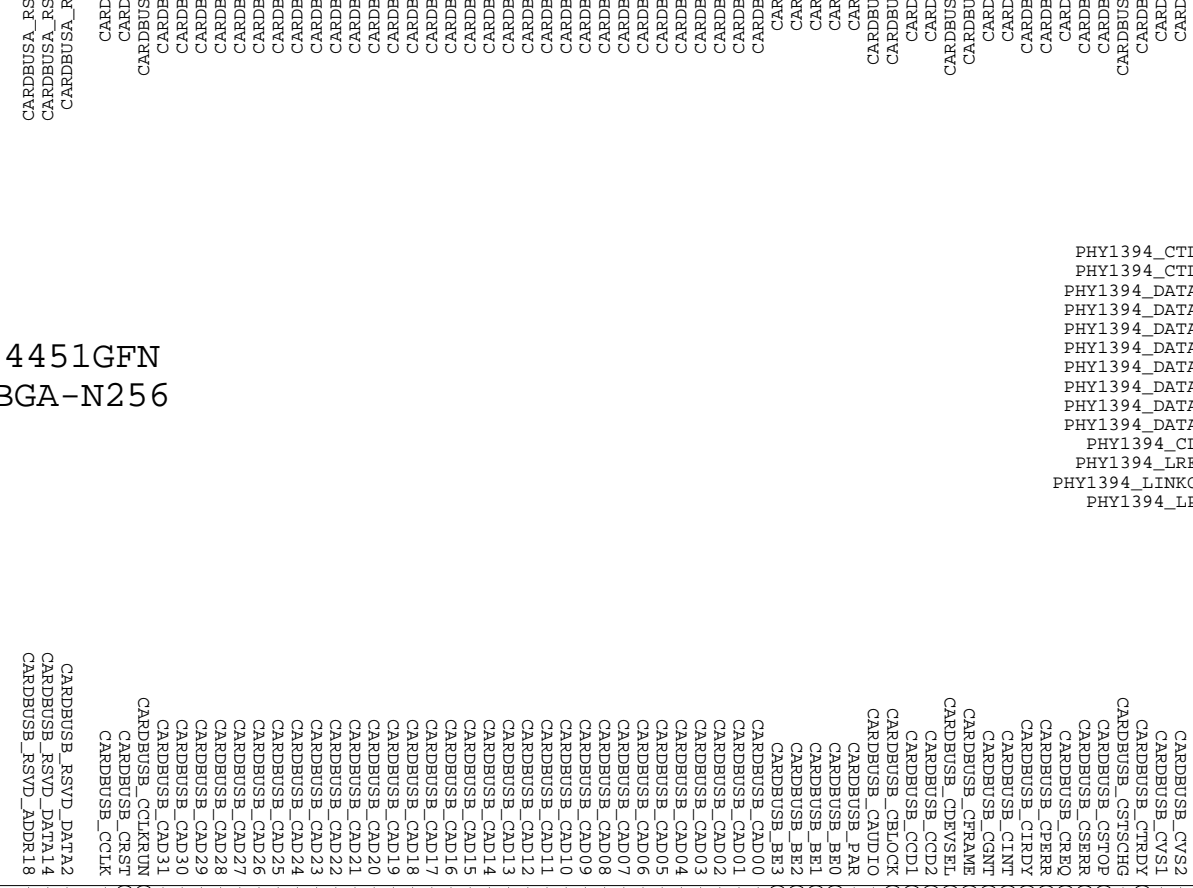
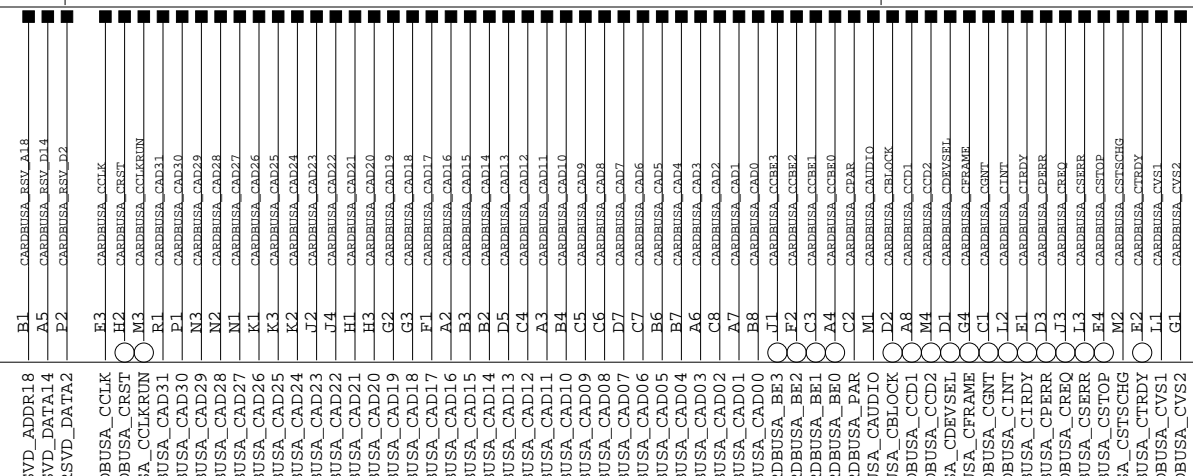
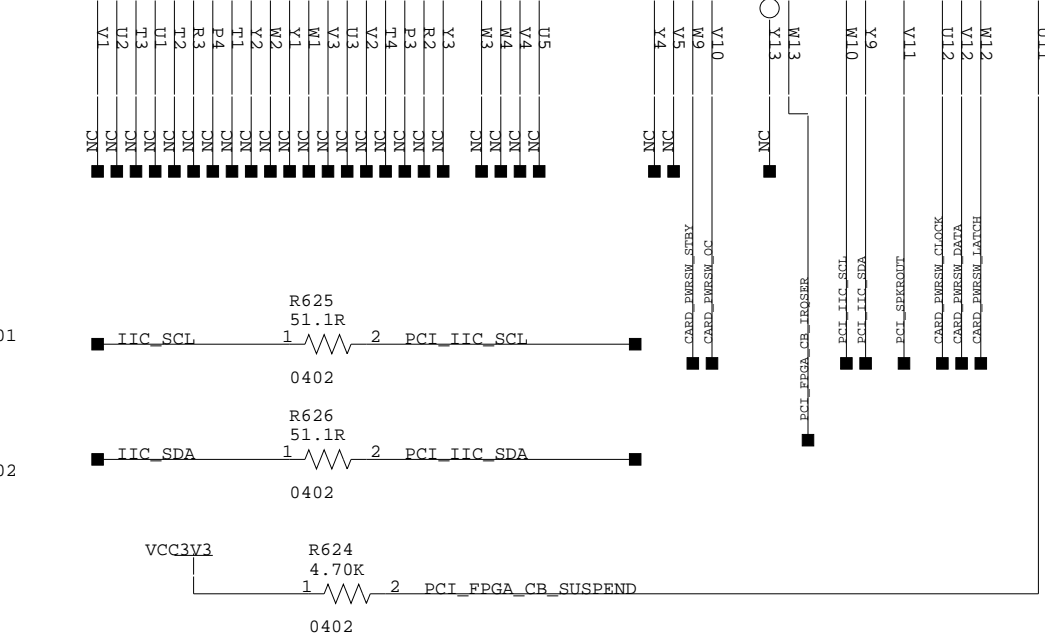
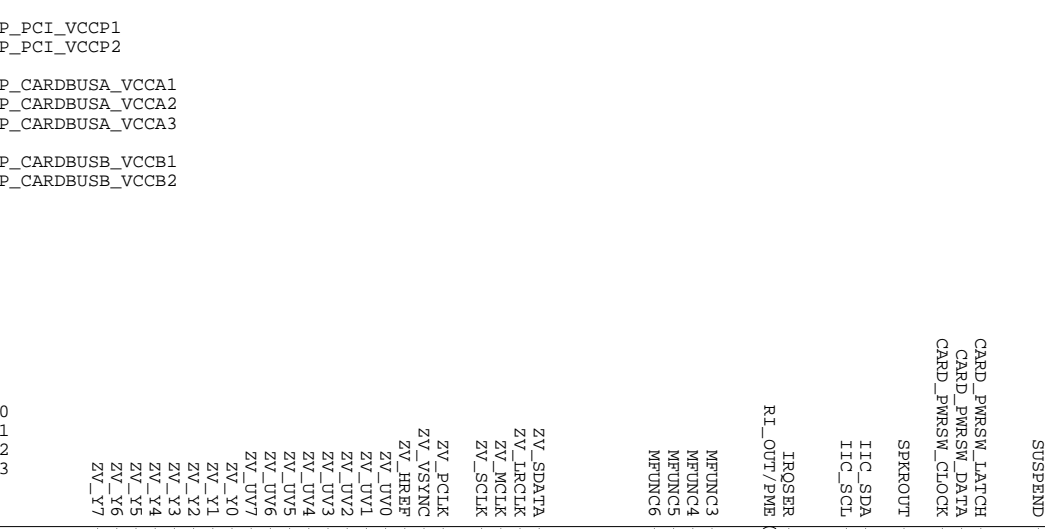
PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU PMC Connectors	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 49 of 55	Drawn By BP/GB



5V Exxx	3V Exxx	What	Default
E601 OPEN	E602 CLOSED	FPGA PCI 3V	Default
E601 CLOSED	E602 OPEN	FPGA PCI 5V	Default
E603 OPEN	E604 CLOSED	LOWER PCI 3V	Default
E603 CLOSED	E604 OPEN	LOWER PCI 5V	Default
E605 OPEN	E606 CLOSED	UPPER PCI 3V	Default
E605 CLOSED	E606 OPEN	UPPER PCI 5V	Default

PCI4451GFN  
S-PBGA-N256



Title: ML300_CSPU CardBus to PCI Bridge	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 50 of 55	Drawn By GB

Bnk 1/2  
Pg 8/9  
PCI 2  
CardBus

PCB: 1280285  
ASM: 0431182  
SCH: 0381135

DO NOT STUFF

CARDBUS\_CONN  
Upper Slot

51	CARD35_GND
52	CARD36_CD1#
53	CARD37_AD2
54	PAGND17
55	CARD38_AD4
56	CARD39_AD6
57	PAGND18
58	CARD40_RSVD_D14
59	CARD41_AD8
60	PAGND19
61	CARD42_AD10
62	CARD43_VS1
63	PAGND20
64	CARD44_AD13
65	CARD45_AD15
66	PAGND21
67	CARD46_AD16
68	CARD47_RSVD_A18
69	PAGND22
70	CARD48_BLOCK
71	CARD49_STOP#
72	PAGND23
73	CARD50_DEVSEL#
74	CARD51_VCC
75	PAGND24
76	PAGND25
77	CARD52_VFP2
78	CARD53_TRDY#
79	PAGND26
80	CARD54_FRAME#
81	CARD55_AD17
82	PAGND27
83	CARD56_AD19
84	CARD57_VS2
85	PAGND28
86	CARD58_RST#
87	CARD59_SERR#
88	PAGND29
89	CARD60_REO#
90	CARD61_CBE3#
91	PAGND30
92	CARD62_AUDIO
93	CARD63_STSCHG
94	PAGND31
95	CARD64_AD28
96	CARD65_AD30
97	PAGND32
98	CARD66_AD31
99	CARD67_CD2#
100	CARD68_GND

1	GND_CA01
2	CARD01_CA02
3	CARD01_CA03
4	PAGND1
5	CARD02_CA04
6	CARD02_CA05
7	PAGND2
8	CARD03_CA06
9	CARD03_CA07
10	PAGND3
11	CARD04_CA08
12	CARD04_CA09
13	PAGND4
14	CARD05_CA10
15	CARD05_CA11
16	PAGND5
17	CARD06_CA12
18	CARD06_CA13
19	PAGND6
20	CARD07_CA14
21	CARD07_CA15
22	PAGND7
23	CARD08_CA16
24	CARD08_CA17
25	PAGND8
26	PAGND9
27	CARD09_CA18
28	CARD09_CA19
29	PAGND10
30	CARD10_CA20
31	CARD10_CA21
32	PAGND11
33	CARD11_CA22
34	CARD11_CA23
35	PAGND12
36	CARD12_CA24
37	CARD12_CA25
38	PAGND13
39	CARD13_CA26
40	CARD13_CA27
41	PAGND14
42	CARD14_CA28
43	CARD14_CA29
44	PAGND15
45	CARD15_CA30
46	CARD15_CA31
47	PAGND16
48	CARD16_RSVD_D2
49	CARD16_CCLKRUN
50	GND_CA34

P110

PKG\_TYPE=FCI71240-340CA

CARDBUS\_CONN  
Lower Slot

151	CB35_GND
152	CB36_CD1#
153	CB37_AD2
154	PBGN17
155	CB38_AD4
156	CB39_AD6
157	PBGN18
158	CB40_RSVD_D14
159	CB41_AD8
160	PBGN19
161	CB42_AD10
162	CB43_VS1
163	PBGN20
164	CB44_AD13
165	CB45_AD15
166	PBGN21
167	CB46_AD16
168	CB47_RSVD_A18
169	PBGN22
170	CB48_BLOCK#
171	CB49_STOP#
172	PBGN23
173	CB50_DEVSEL#
174	CB51_VCC
175	PBGN24
176	PBGN25
177	CB52_VFP2
178	CB53_TRDY#
179	PBGN26
180	CB54_FRAME#
181	CB55_AD17
182	PBGN27
183	CB56_AD19
184	CB57_VS2
185	PBGN28
186	CB58_RST#
187	CB59_SERR#
188	PBGN29
189	CB60_REO#
190	CB61_CBE3#
191	PBGN30
192	CB62_AUDIO
193	CB63_STSCHG
194	PBGN31
195	CB64_AD28
196	CB65_AD30
197	PBGN32
198	CB66_AD31
199	CB67_CD2#
200	CB68_GND

101	GND_CB01
102	AD0_CB02
103	AD1_CB03
104	PBGN1
105	AD3_CB04
106	AD5_CB05
107	PBGN2
108	AD7_CB06
109	AD9_CB07
110	PBGN3
111	AD11_CB08
112	AD13_CB09
113	PBGN4
114	AD15_CB10
115	AD17_CB11
116	PBGN5
117	AD19_CB12
118	AD21_CB13
119	PBGN6
120	AD23_CB14
121	AD25_CB15
122	PBGN7
123	AD27_CB16
124	AD29_CB17
125	PBGN8
126	PBGN9
127	AD31_CB18
128	AD33_CB19
129	PBGN10
130	AD35_CB20
131	AD37_CB21
132	PBGN11
133	AD39_CB22
134	AD41_CB23
135	PBGN12
136	AD43_CB24
137	AD45_CB25
138	PBGN13
139	AD47_CB26
140	AD49_CB27
141	PBGN14
142	AD51_CB28
143	AD53_CB29
144	PBGN15
145	AD55_CB30
146	AD57_CB31
147	PBGN16
148	AD59_CB32
149	AD61_CB33
150	GND_CB34

P110

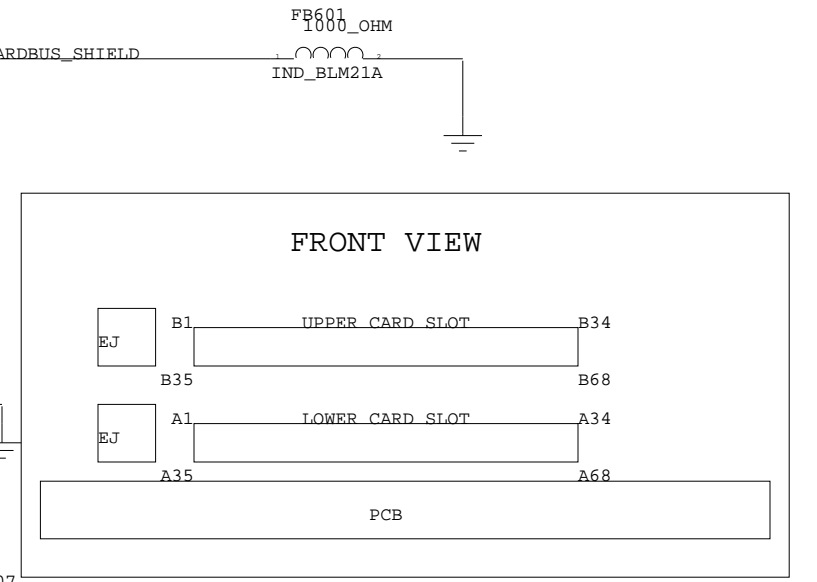
PKG\_TYPE=FCI71240-340CA

ML300 CPU  
PCI Bridge  
Cardbus Conn



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

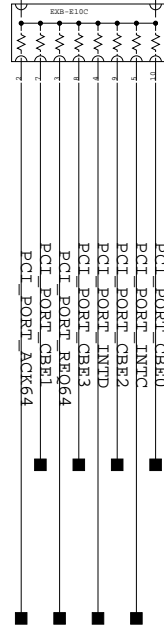
Title: ML300_CPU CardBus Connectors	
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 51 of 55	Drawn By BP/GB



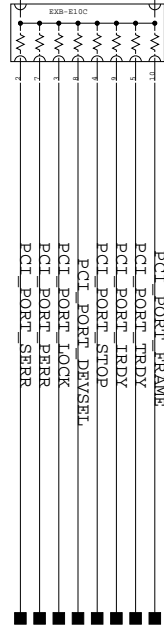
Notes:  
1. Power Supply for CardBus found on page 53.

VCC3V3

RP601  
4.7K



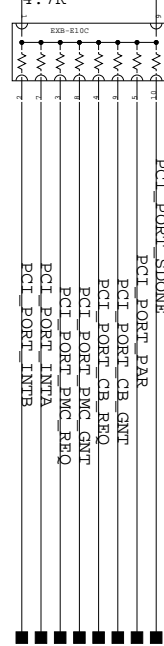
RP602  
4.7K



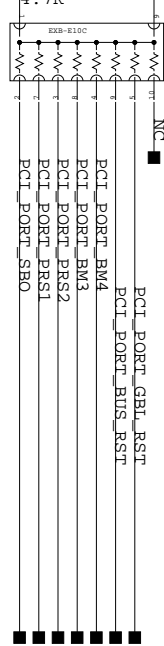
R649  
DNP  
0402

R675  
4.70K  
0402

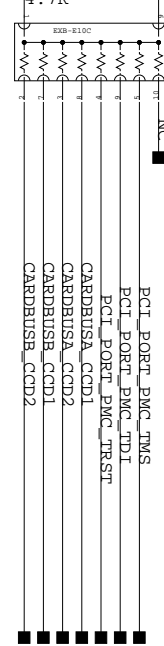
RP604  
4.7K



RP605  
4.7K



RP606  
4.7K



R647  
4.70K  
0402

R659  
4.70K  
0402

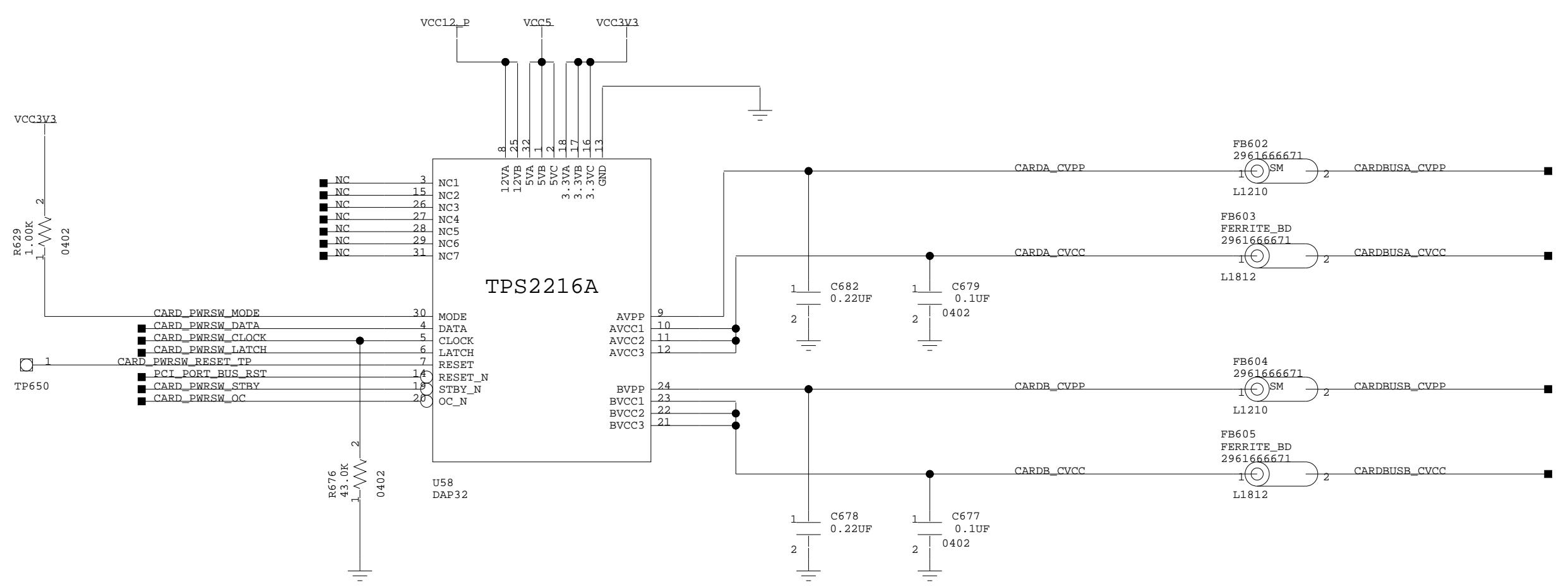
# ML300 CPU PCI Termination



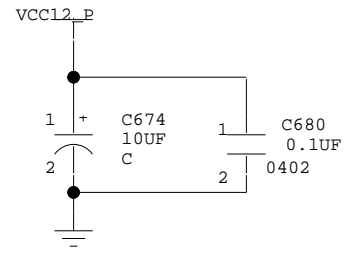
PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300\_CPU  
PCI Termination

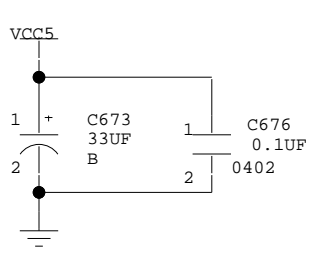
Date: October 17th, 2002	Ver: 1.00
Sheet Size: B	Rev: A
Sheet 52 of 56	Drawn By BP



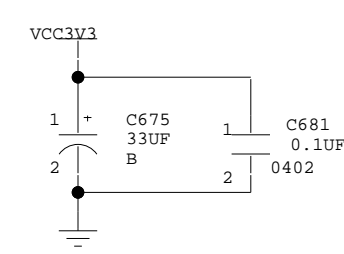
Place Near 12VX of U58



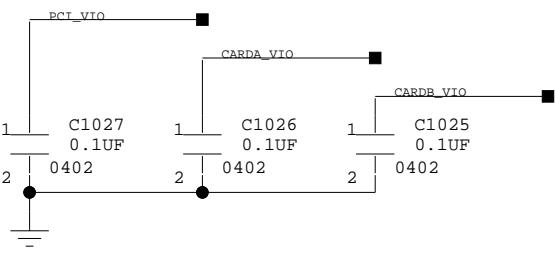
Place Near 5VX of U58



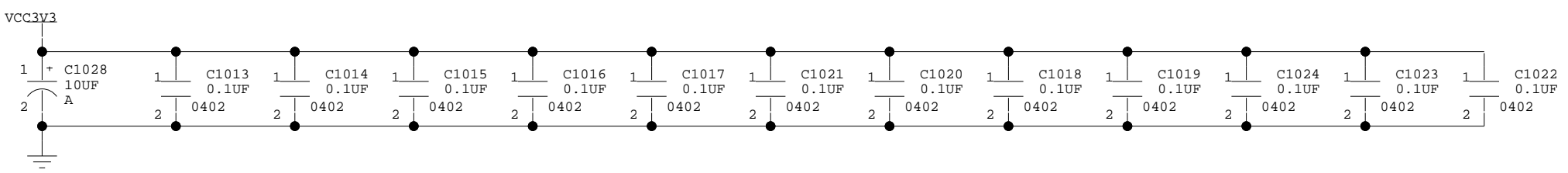
Place Near 3.3VX of U58



Place Near VCCIO PCI pins on U601



Place Near VCC Pins of U601

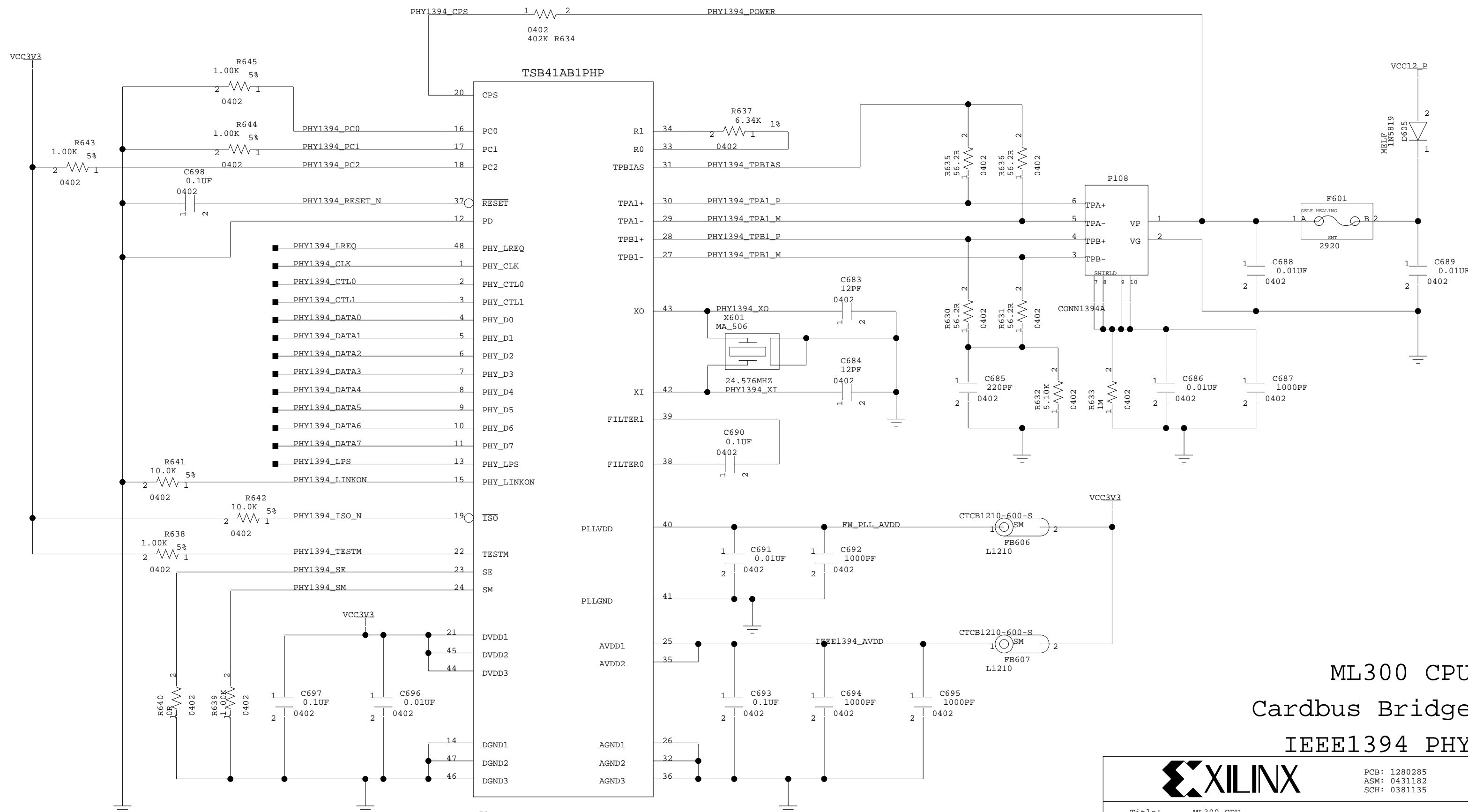


# ML300 CPU Power Supply



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU CardBus Power Supply	
Date: October 17th, 2002	Ver: 1.00
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ML300 CPU  
Cardbus Bridge  
IEEE1394 PHY

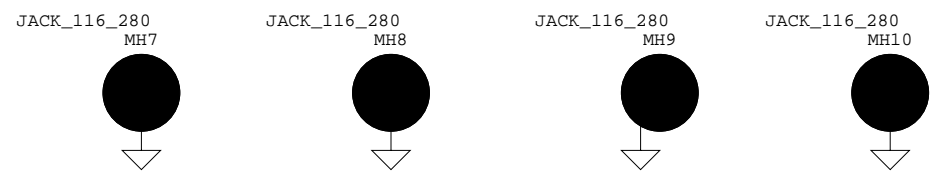
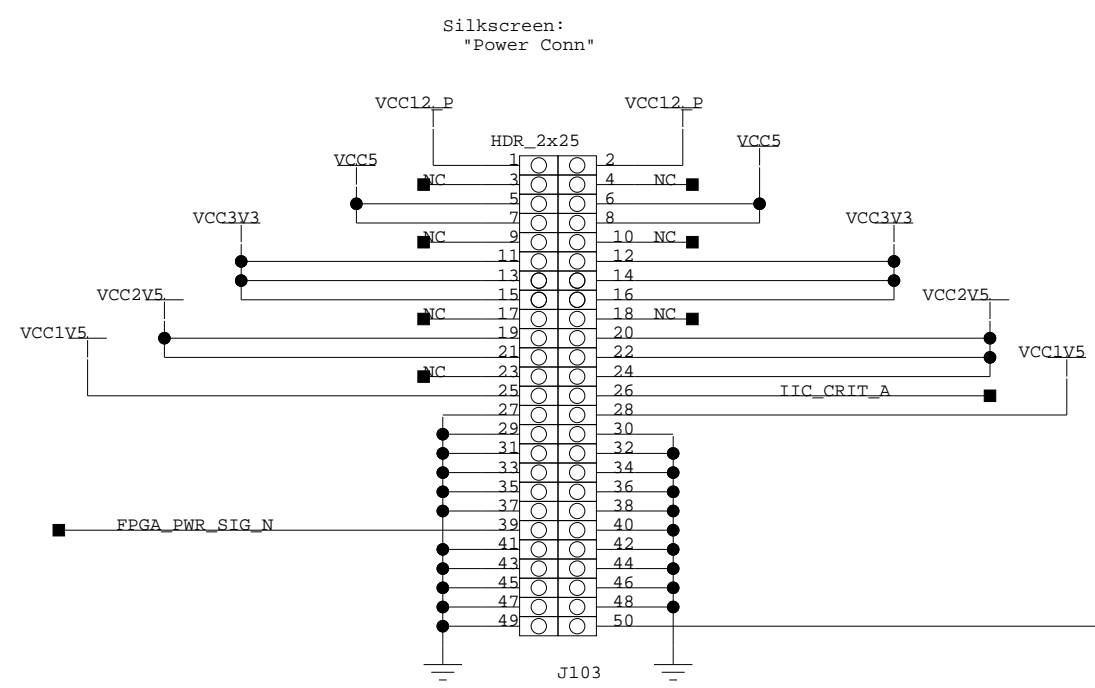
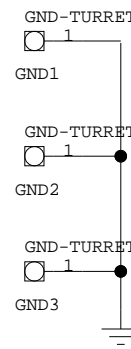
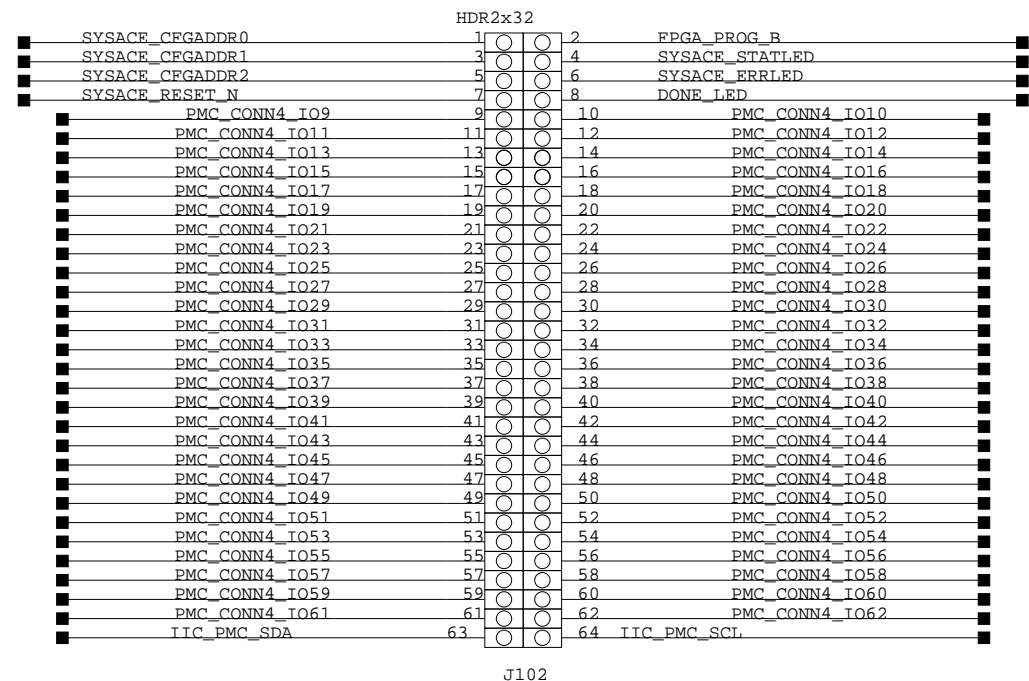
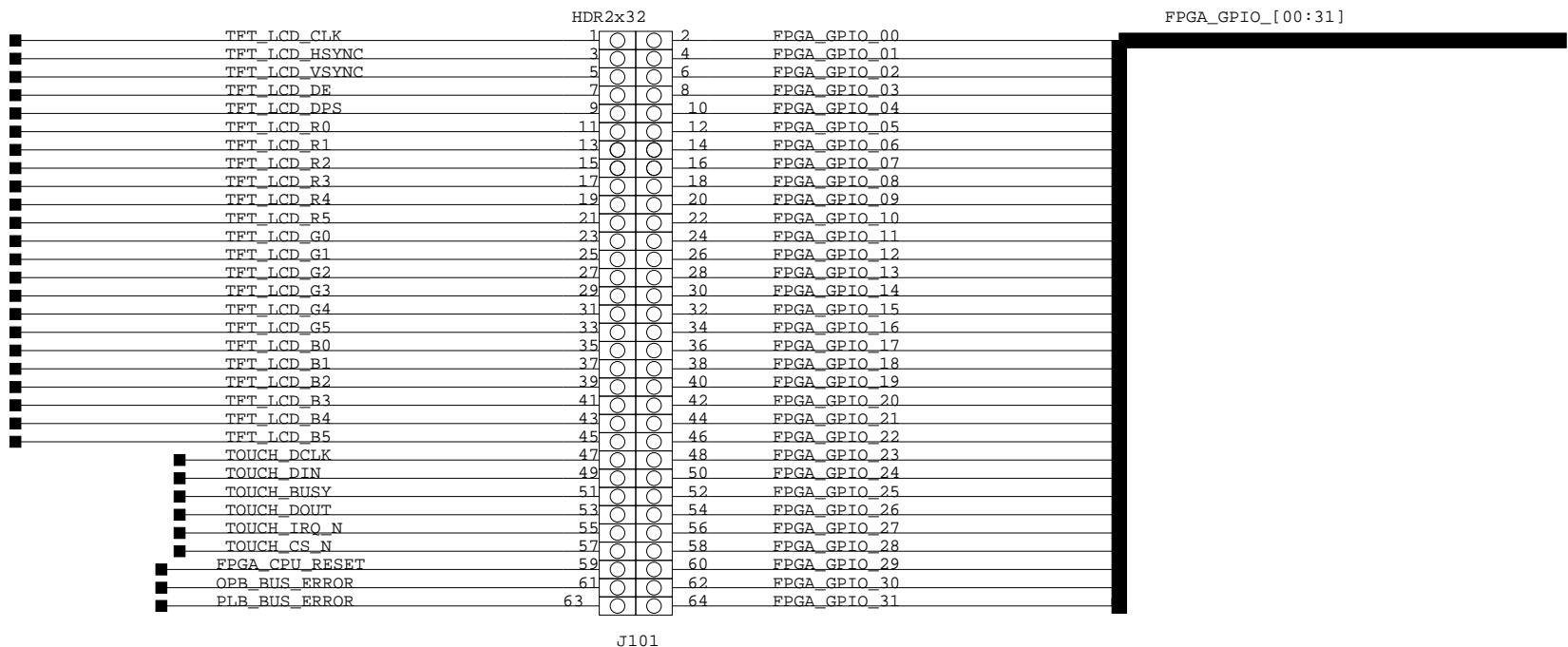


PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU IEEE1394 (FireWire) PHY	
Date: October 17th, 2002	Ver: 1.00
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Silkscreen:  
"Digital Conn 1"

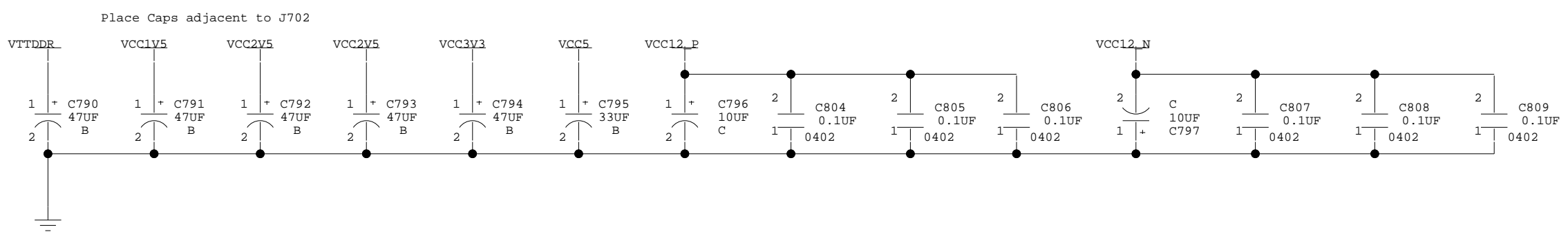
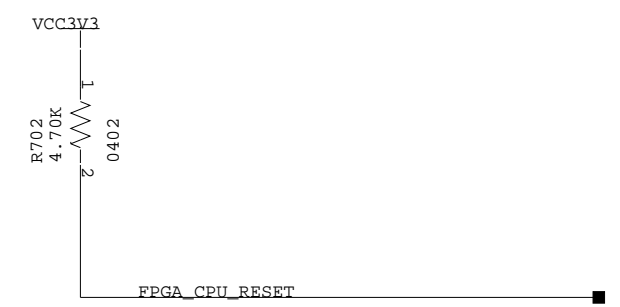
Silkscreen:  
"Digital Conn 2"



Powerboard Mounting Holes



Fabrication Fiducials  
Three per Side



# ML300 CPU Mezz Connector



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300_CPU Mezzanine Power and I/O Connectors	
Date: October 17th, 2002	Ver: 1.00
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Net Class Routing Rules

1	NET_CLASS   DDR_CNTRL_FPGA + DDR_CNTRL_RES Route Order U1 - U15 through (RP362,RP363).	< 6000 mils   thru resistors   + ignore tralength to termination resistor Termination Resistor(RP329,RP331) not part of overall length.	
2	NET_CLASS   DDR_CNTRL_REG + DDR_CNTRL_MEM Route Order U15 - U9,U8,U7,U6 through (RP308,RP311).	< 4500 mils   thru resistors   + ignore tralength to termination resistor Termination Resistor(RP336) not part of overall length.	
3	NET_CLASS   DDR_ADDR_FPGA + DDR_ADDR_RES Route Order U1 - U14 through (RP359,RP360,RP361,RP362).	< 6000 mils   thru resistors   + ignore tralength to termination resistor Termination Resistor(RP330,RP331) not part of overall length.	
4	NET_CLASS   DDR_ADDR_REG + DDR_ADDR_MEM Route Order U14 - U6,U7,U8,U9 through (RP302,RP303,RP304,RP311).	< 4500 mils   thru resistors   + ignore tralength to termination resistor Termination Resistor(RP338,RP339) not part of overall length.	
5	NET_CLASS   DDR_DQS_FPGA + DDR_DQS_RES + DDR_DQS_MEM Route Order U1 - U6,U7,U8,U9 through (RP326,RP324,R311-R314).	< 3300 mils   thru resistors   + ignore tralength to termination resistor Termination resistor (RP340,RP341,R315-R318) not part of overall length.	
6	NET_CLASS   DDR_DATA_FPGA + DDR_DATA_RES + DDR_DATA_MEM Route Order U1 - U6,U7,U8,U9 through (RP315-RP322 and RP347,RP348,RP350,RP351,RP353,RP354,RP356,RP357). Termination resistor (RP349,RP352,RP355,RP358,RP603,RP346,RP344,RP345) not part of overall length.	< 3750 mils   thru resistors   + ignore tralength to termination resistor	
7	NET_CLASS   DDR_CLK_FPGA + DDR_CLK_RES Route Order U1 - U16 through (R307, R308). DDR_CLK_*** PT 1: Route Order U1.U21 through resistor R308 to U16.13 (ignore tralength to term R302) DDR_CLK_*** PT 2: Toute Order U1.U21 through resistor R308 back to U1.AC14 (ignore tralength to R309). DDR_CLK_***_N PT 1: Route Order U1.U22 through resistor R307 to U16.14 (ignore tralength to term R303). DDR_CLK_***_N PT 2: Route Order U1.U22 through resistor R307 to C366 (ignore tralength to R310).	Matched lengths +/- 6 mil   + ignore tralength to termination resistor Termination resistor (R302,R303,R309) not part of overall length.	
8	NET_CLASS   DDR_CLK_PLL + DDR_CLK_MEM Route Order U16 - U6,U7,U8,U9 through (RP328,RP327,RP325).	Matched lengths +/- 60 mils   thru resistors + ignore tralength to term res Term resistor (RP340,RP341,RP330,RP331,RP329) not part of overall length	
9	NET_CLASS   CLK_27MHZ_FPGA + CLK_27MHZ_COMP Route Order U1 - U601,J104 through (R1007,R108). U1 to U601 through R1007 U1 to J104 through R108	Matched length +/- 60 mil   thru resistors	
10A	NET_CLASS   ENET_PHY	Matched Length +/- 1000 mil	Tight
10B	NET_CLASS   ENET_PHY_COMP	Tight	Tight
11	NET_CLASS   PS2_1	No Issues	
12	NET_CLASS   PS2_2	No Issues	
13	NET_CLASS   CPU_DEBUG Route Order U1 - P14, P109.	Matched Length +/- 1250 mil	Tight
14	NET_CLASS   CPU_TRACE	Matched Length +/- 50 mil	Tight
15	NET_CLASS   SYSACE_FLASH	Tight	Tight
16	NET_CLASS   SYSACE_MPU	Tight	Tight
17A	NET_CLASS   SYSACE_JTAG_2V5	Tight	Tight
17B	NET_CLASS   SYSACE_JTAG_3V3	Tight	Tight
18	Deleted to remove redundancy		
19	NET_CLASS   TFT_CNTRL_FPGA	Tight	These go from the FPGA to a level shifter
20	NET_CLASS   TFT_CNTRL_LCD	Tight	These go from level shifter to TFT conn to PWRI0
21	NET_CLASS   TFT_CLR_FPGA	Tight	These go from the FPGA to a level shifter
22	NET_CLASS   TFT_CLR_LCD	Tight	These go from level shifter to TFT conn to PWRI0
23	NET_CLASS   PCI_FPGA_CONN	Tight	These go from the FPGA to clamp diodes
24	NET_CLASS   PCI_PORT_CONN Route Order U50,U51,U52,U53 - J104,J105, U601. Term Res (RP601, RP602, RP604, RP605, RP606 R649, R675, R647, R659) not part of length.	Tight	These go from clamp diodes to the PMC and PCI4451
25	NET_CLASS   CARDBUSA	Tight	these go from the PCI4451 to the Cardbus connectors
26	NET_CLASS   CARDBUSB	Tight	these go from the PCI4451 to the Cardbus connectors
27	NET_CLASS   AUDIO_DIG_FPGA	Tight	these go from the FPGA to the clamp Diodes
28	NET_CLASS   AUDIO_DIG_PMC	Tight	These go from the clamp diodes to conn and res pack
29	NET_CLASS   AUDIO_DIG_COMP	Tight	These go from the resistor pack to the AD1885 comp
30	NET_CLASS   PMC_FPGA_CONN4	Tight	These go from the FPGA to clamp diodes
31	NET_CLASS   PMC_PMC_CONN4 Route Order U802,U912,U913,U914 - J106, J102	Tight	These go from clamp diodes to PMC4 and PWRI0 conn
32	NET_CLASS   IIC_FPGA	no Issues	These go from the FPGA to clamp diodes
33	NET_CLASS   IIC_PMC	no Issues	These go from clamp diodes to the IIC and conn
34	NET_CLASS   DDR_DM_FPGA + DDR_DM_MEM Route Order U1 - U6,U7,U8,U9 through (RP326,RP324).	< 4500 mils   thru resistors Termination resistor (RP340,RP341) not part of overall length.	+ ignore tralength to termination resistor



PCB: 1280285  
ASM: 0431182  
SCH: 0381135

Title: ML300\_CPU  
Net Classes

# ML300 CPU Net Classes

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