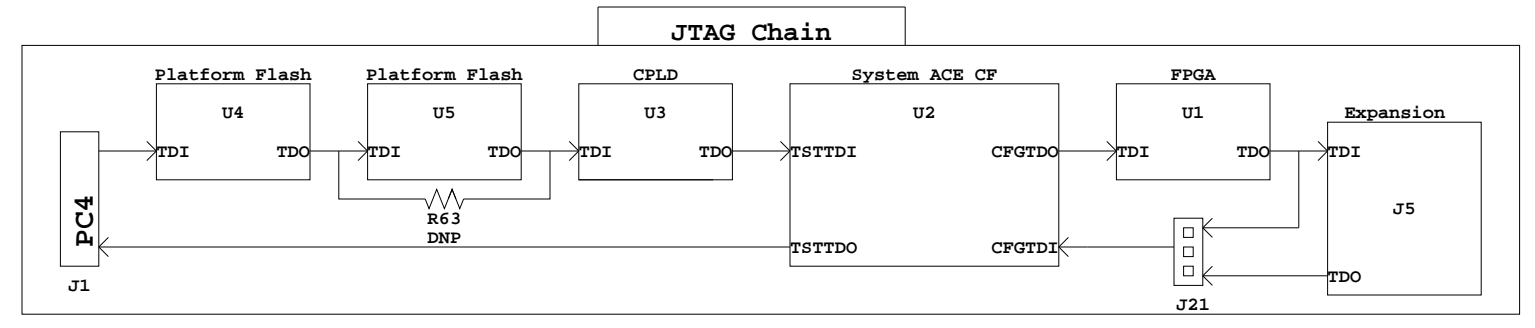
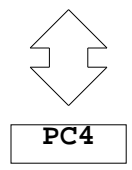
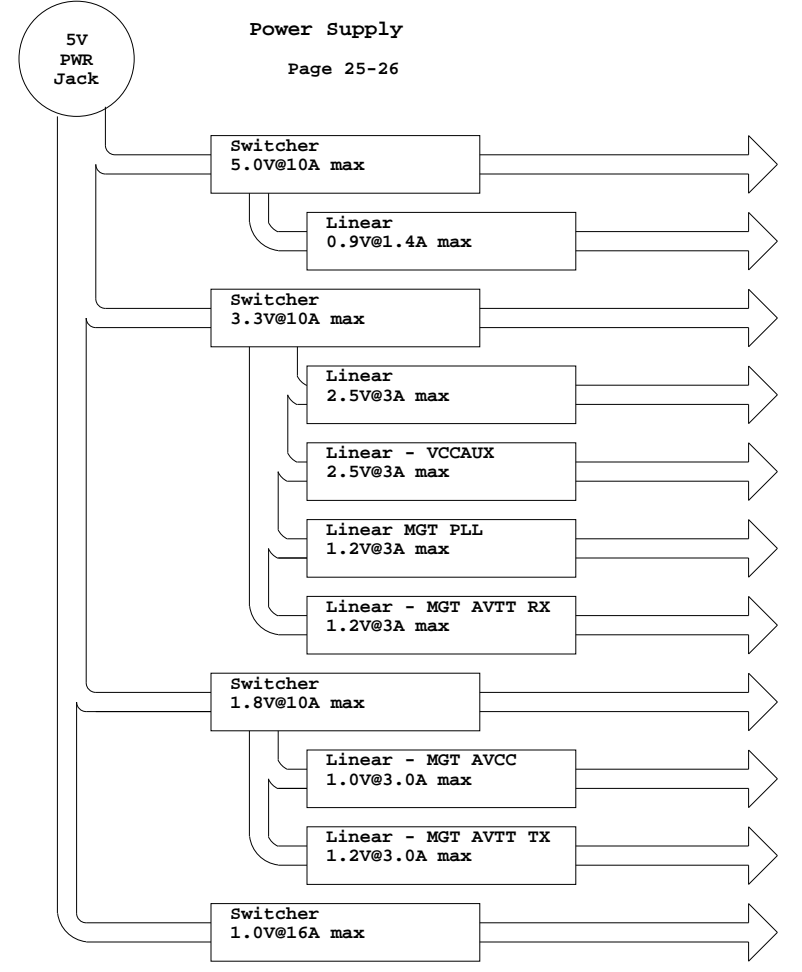
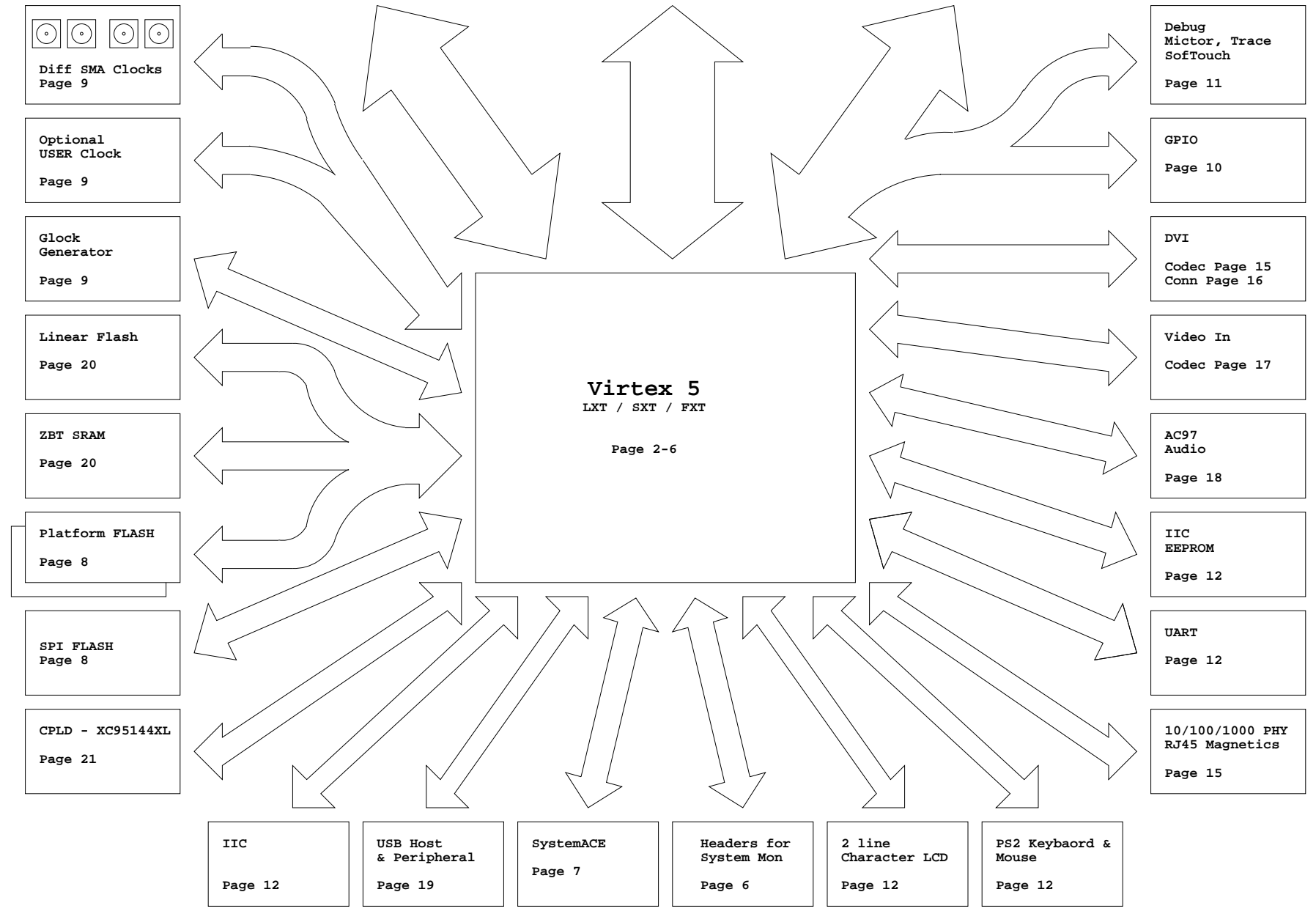


**GTPs**  
SATA, SFP and SGMII  
Page 22-24

**64 Bit DDR2 SODIMM**  
Page 13

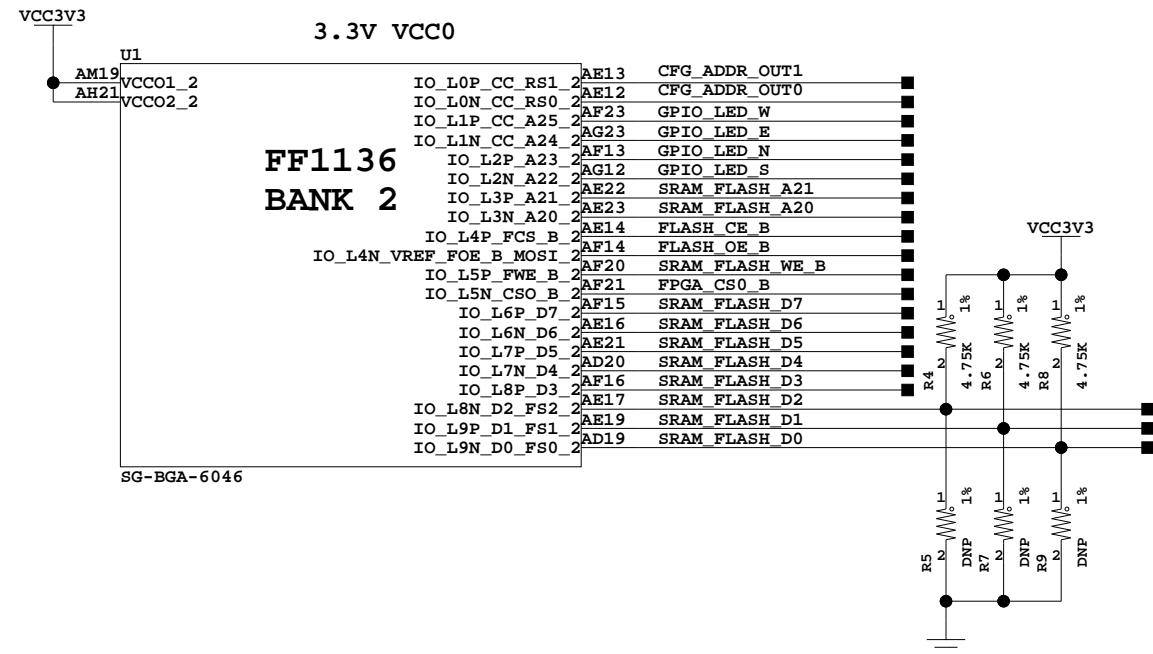
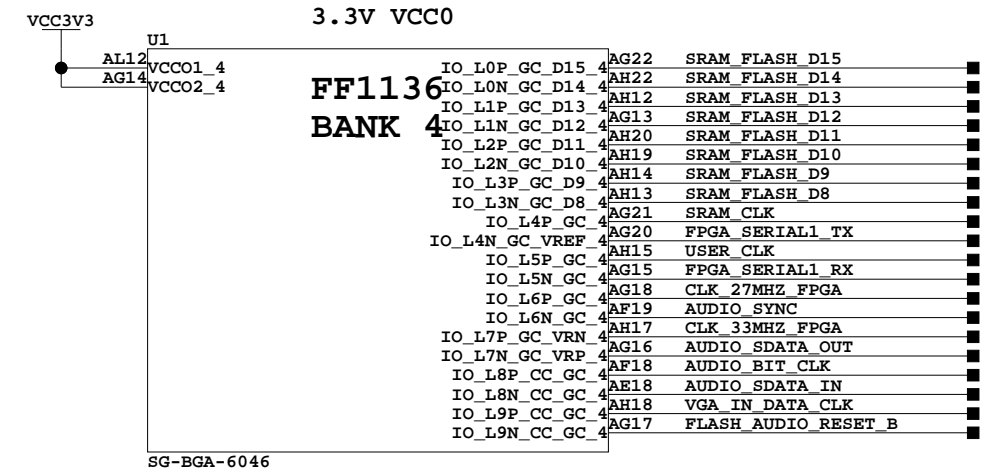
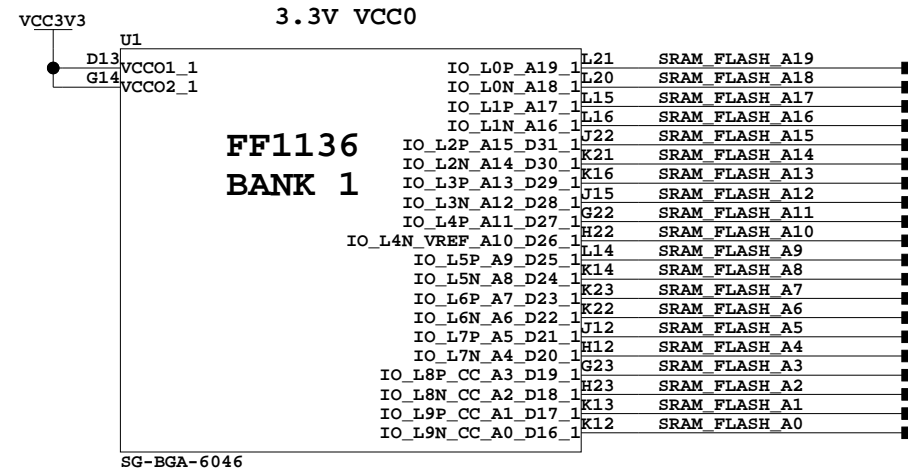
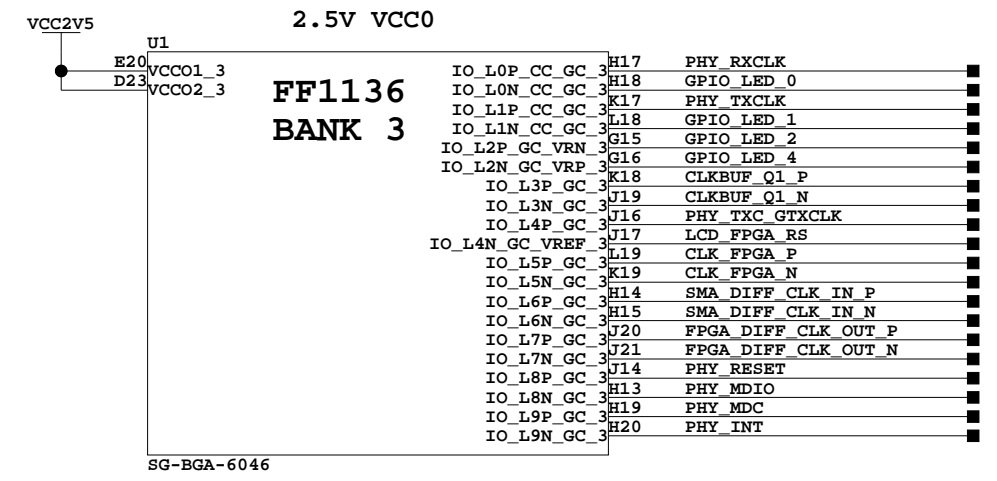
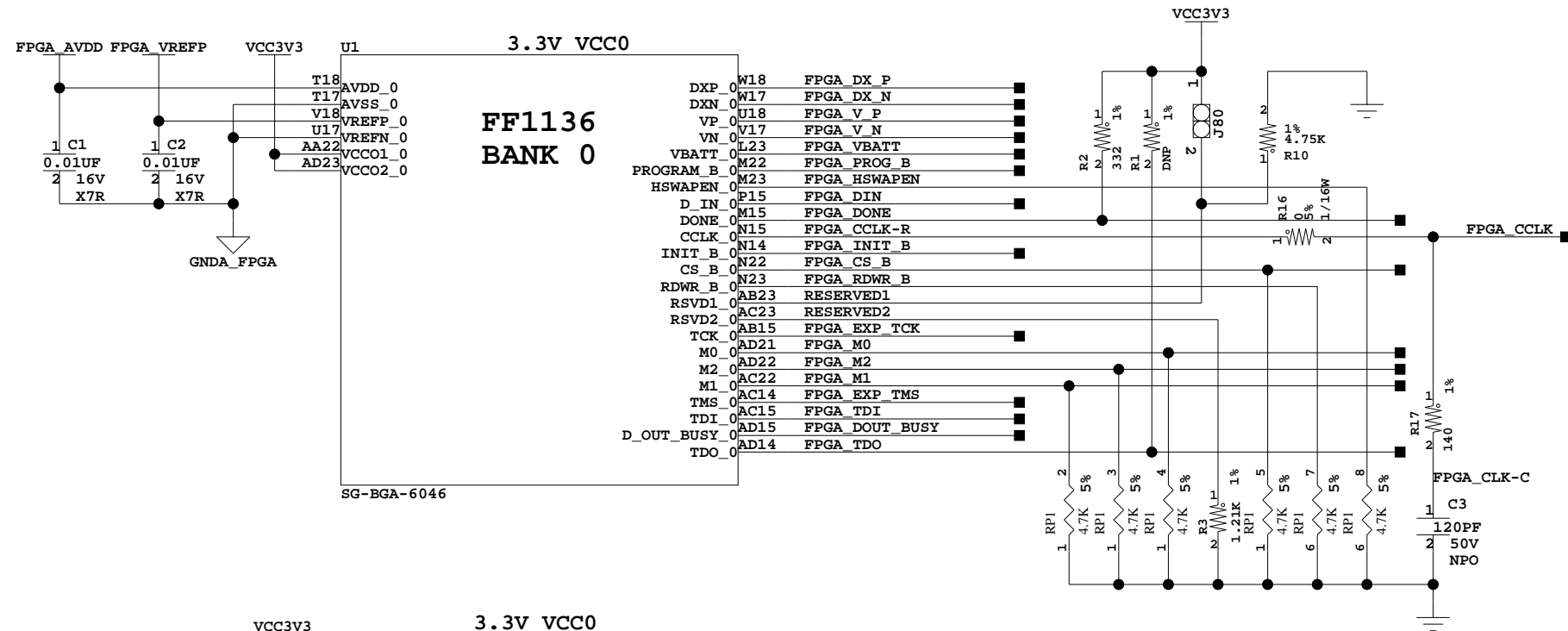
**Expansion Header**  
Page 11



**XILINX**

Title: ML505/6/7 Block Diagram SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241

Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet <b>1</b> of <b>27</b>	Drawn By BP

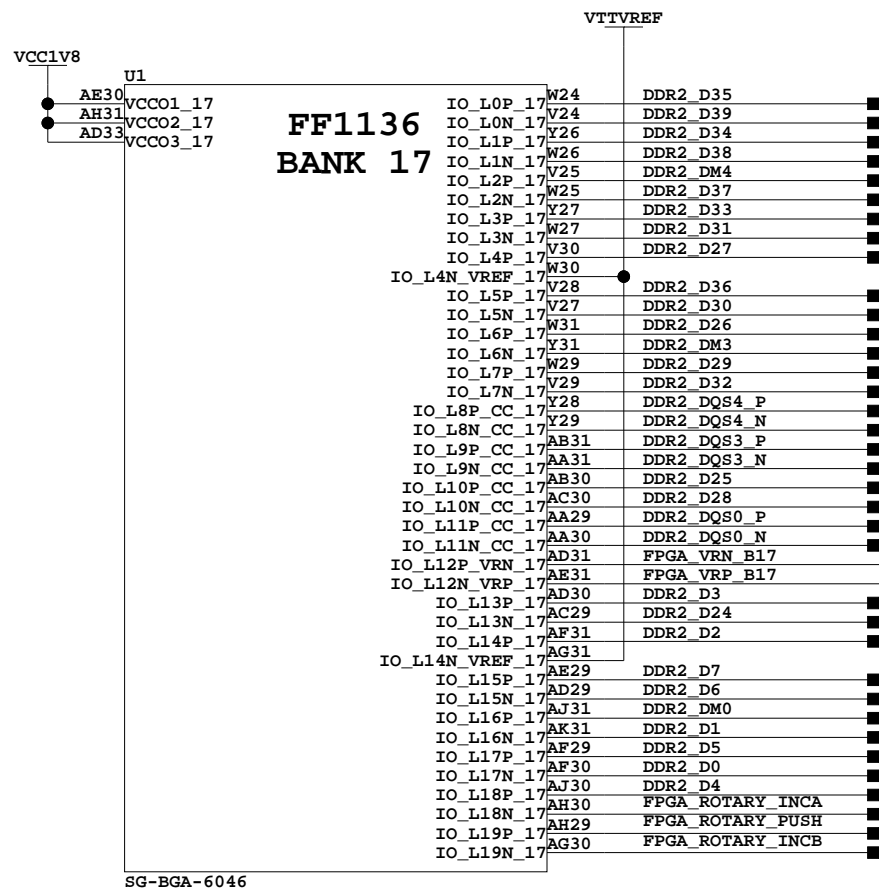
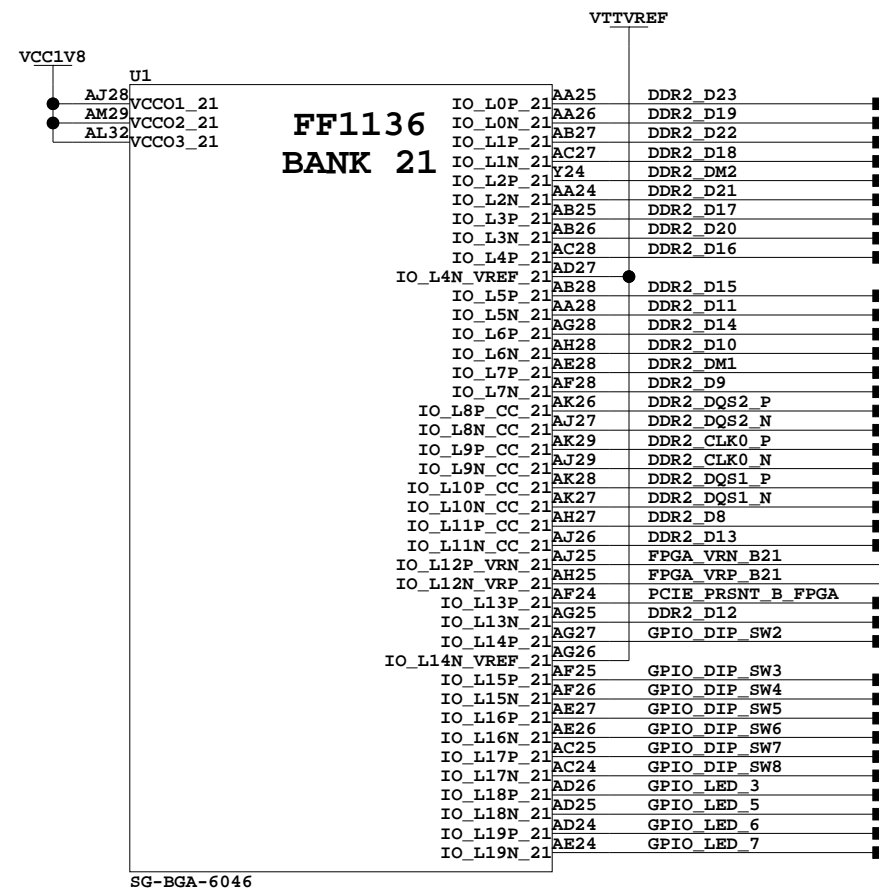
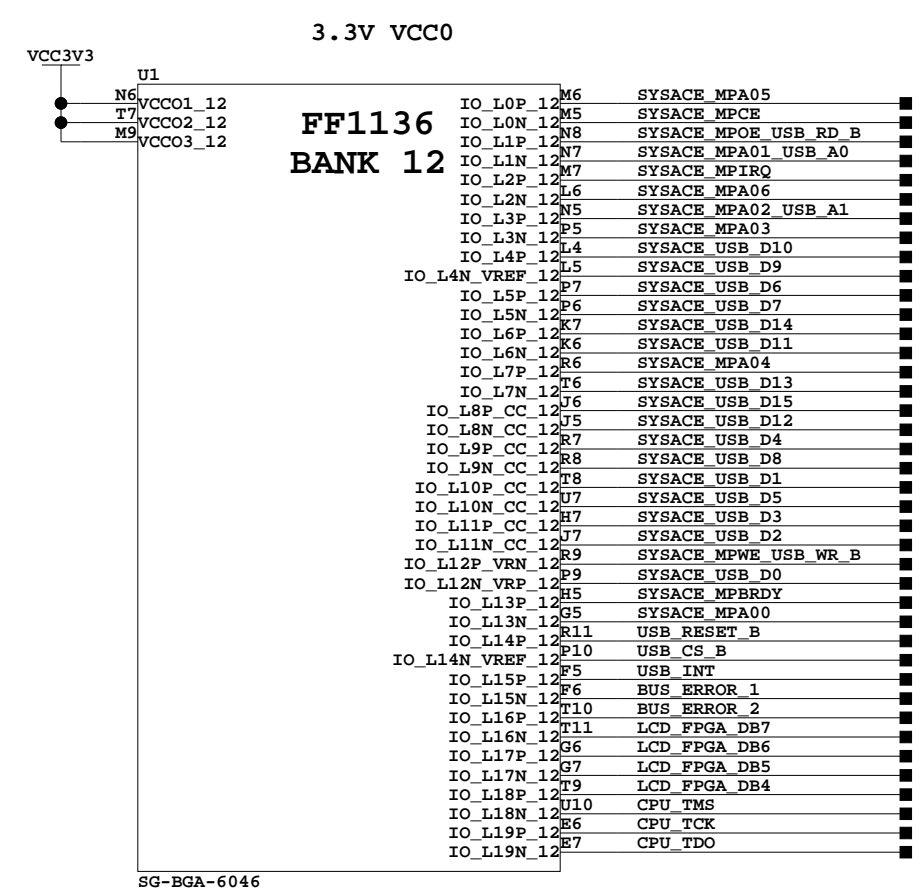
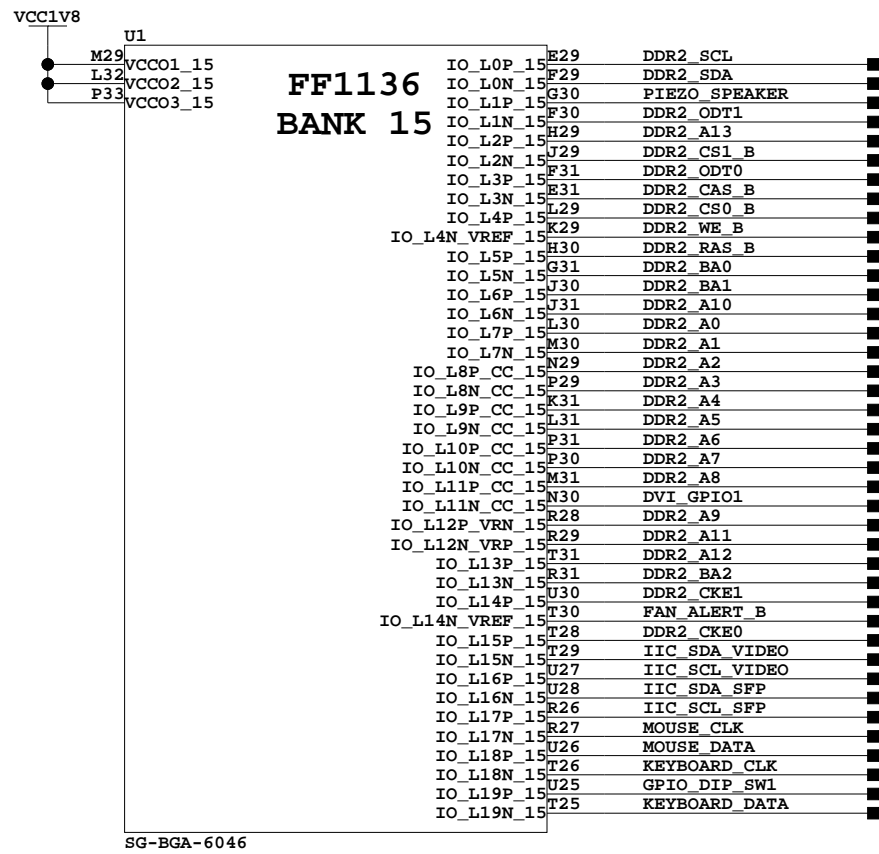
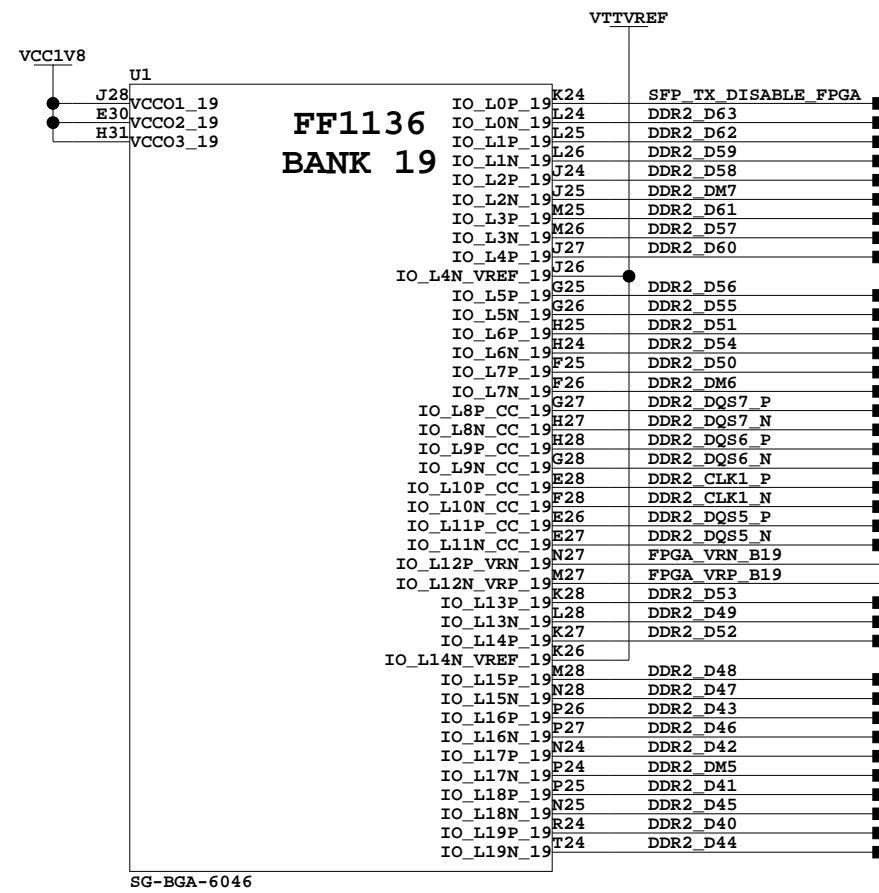


**Banks 0,1,2,3,4  
Config, FLASH, SRAM,  
GPIO, CLKs**



Title: FPGA Banks 0,1,2,3,4@config, FLASH, SRAM, GPIO, CLKs  
SCHEM, ROHS COMPLIANT  
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
0381241

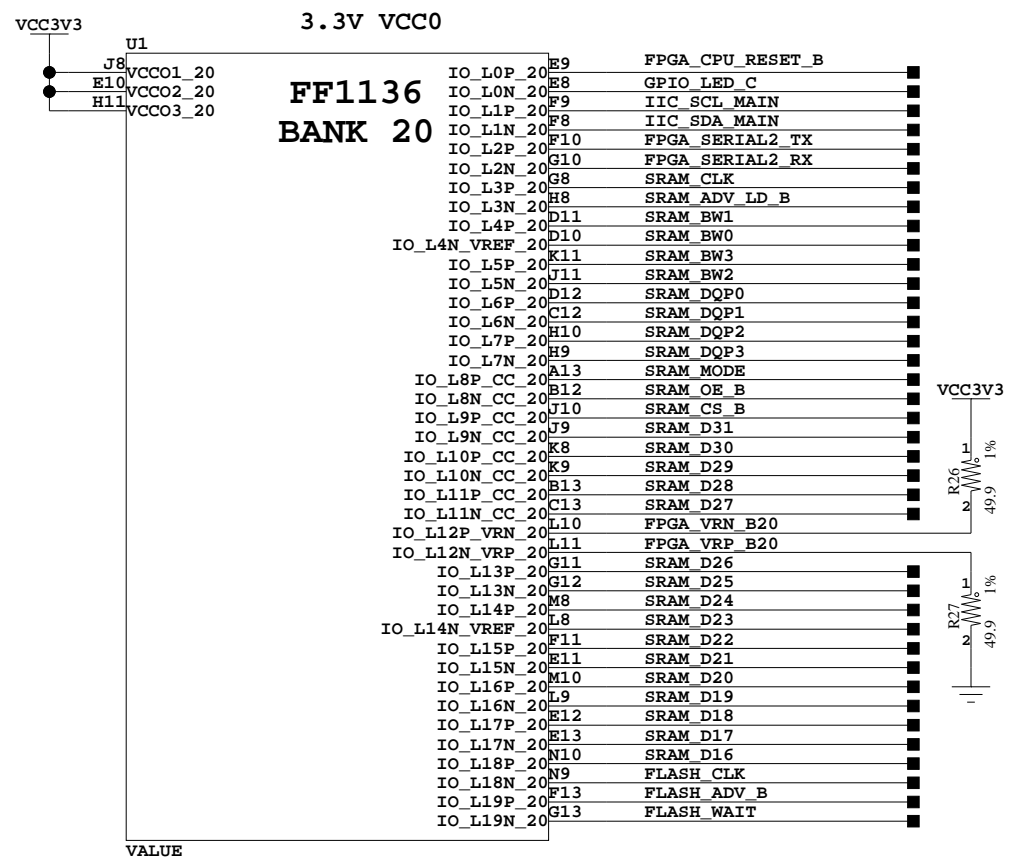
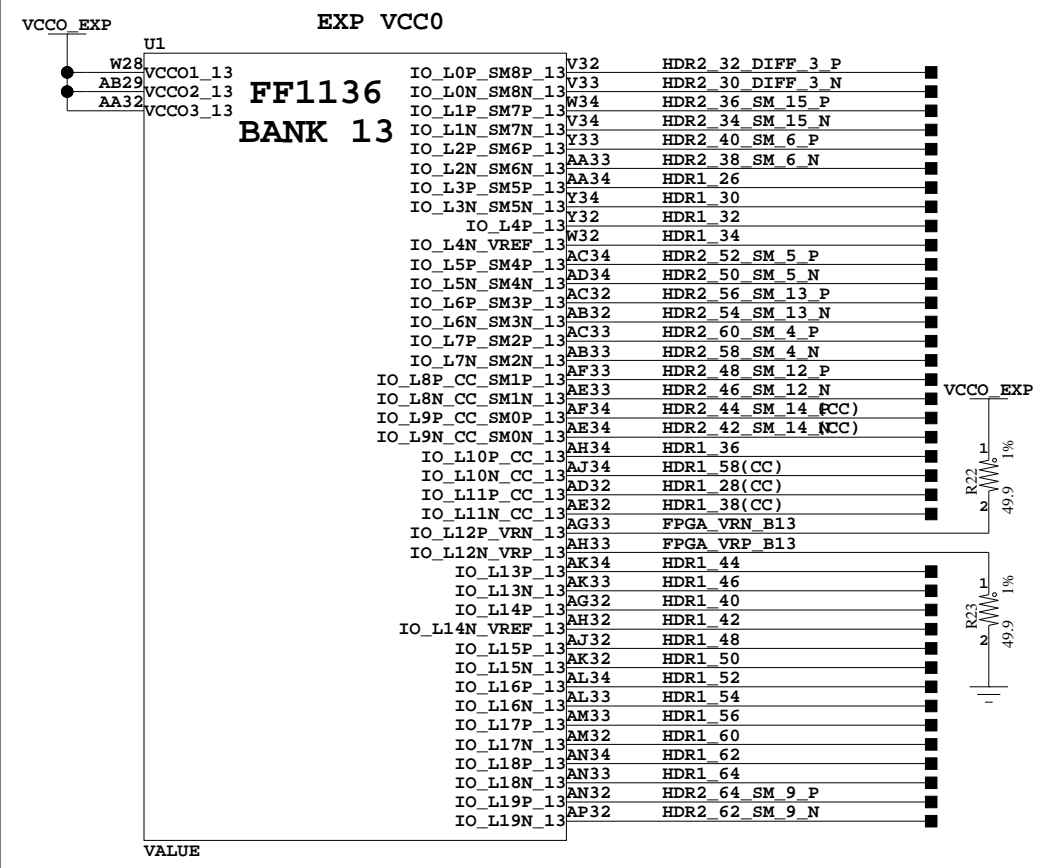
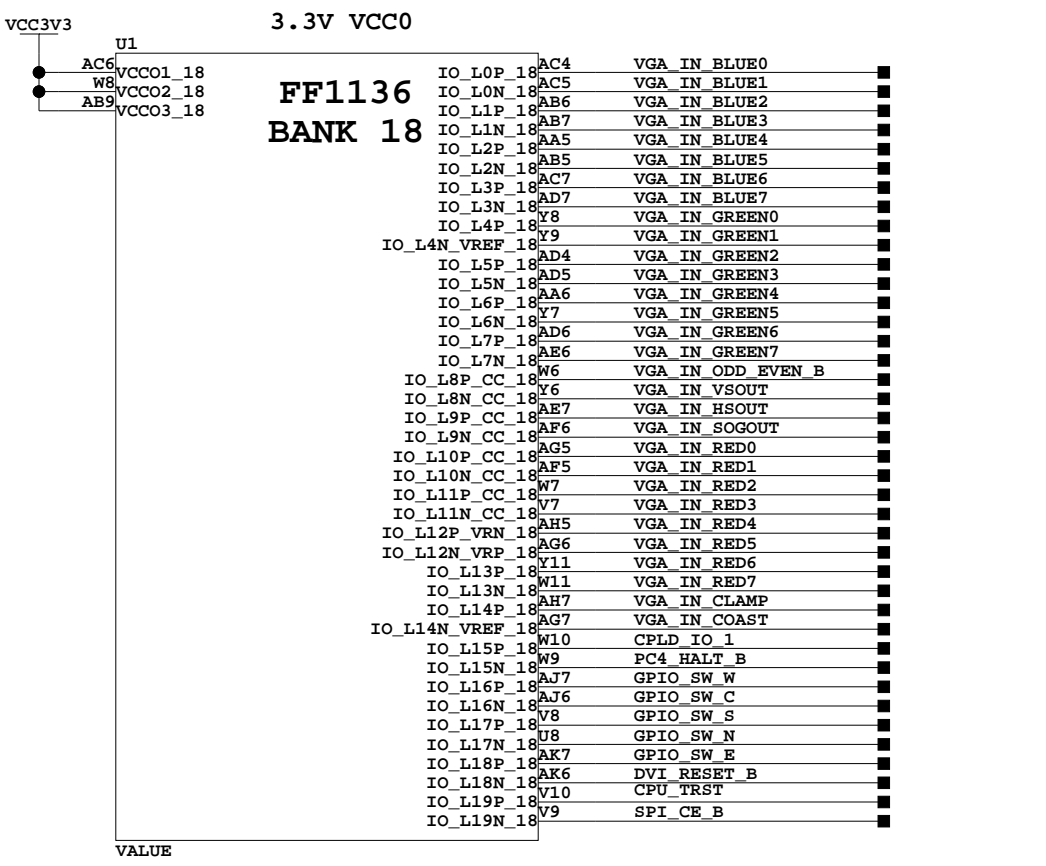
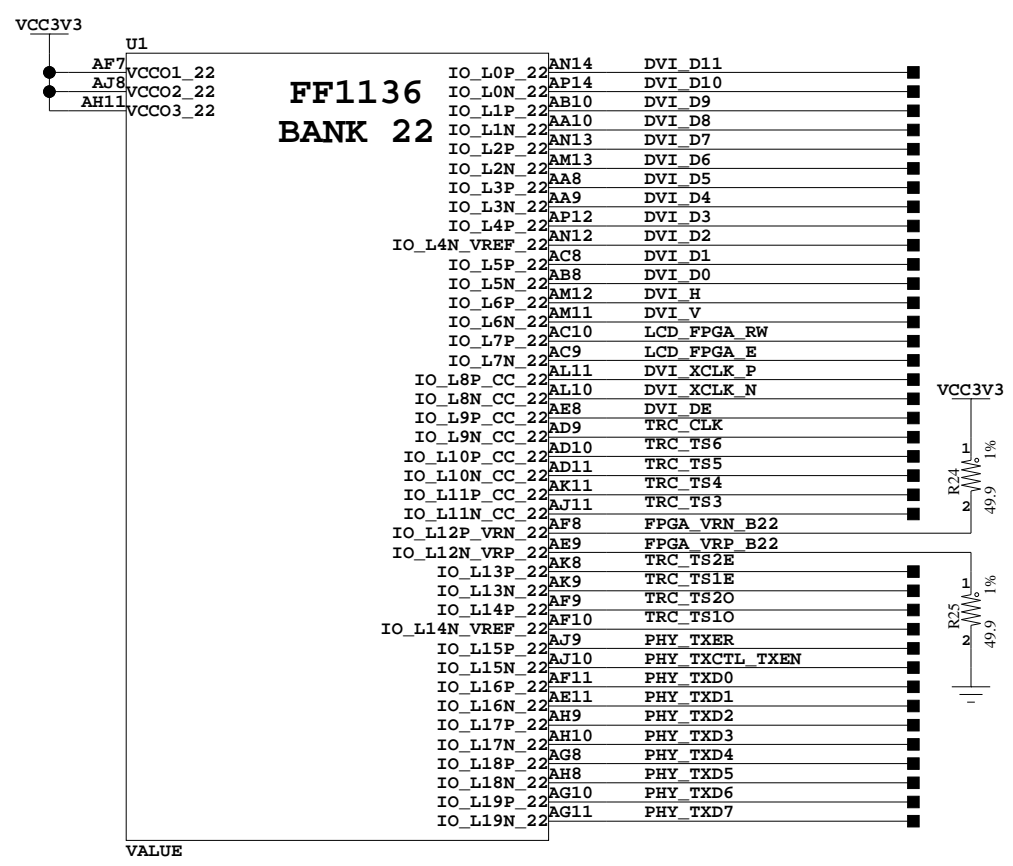
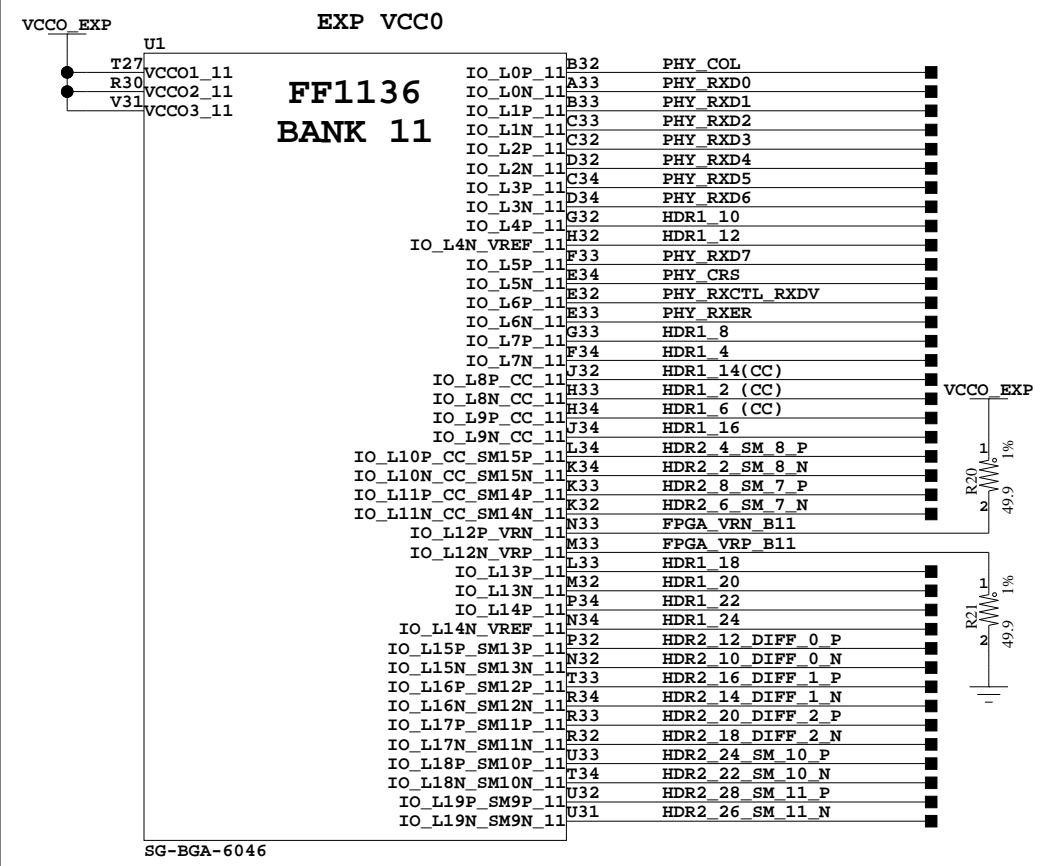
Date:	1-22-2008_14:51	Ver:	A
Sheet Size:	B	Rev:	02
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**Banks 14,16,18,21  
DDR2, PS2, GPIO**



Title: FPGA Bank 14, 16, 18, 21DDR2, PS2, GPIO SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet 3 of 27	Drawn By BP

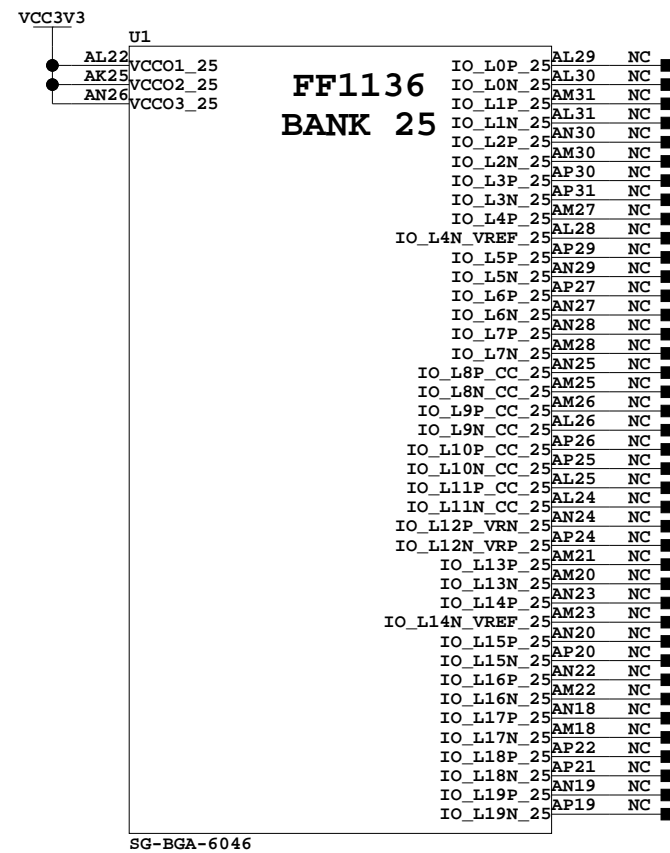
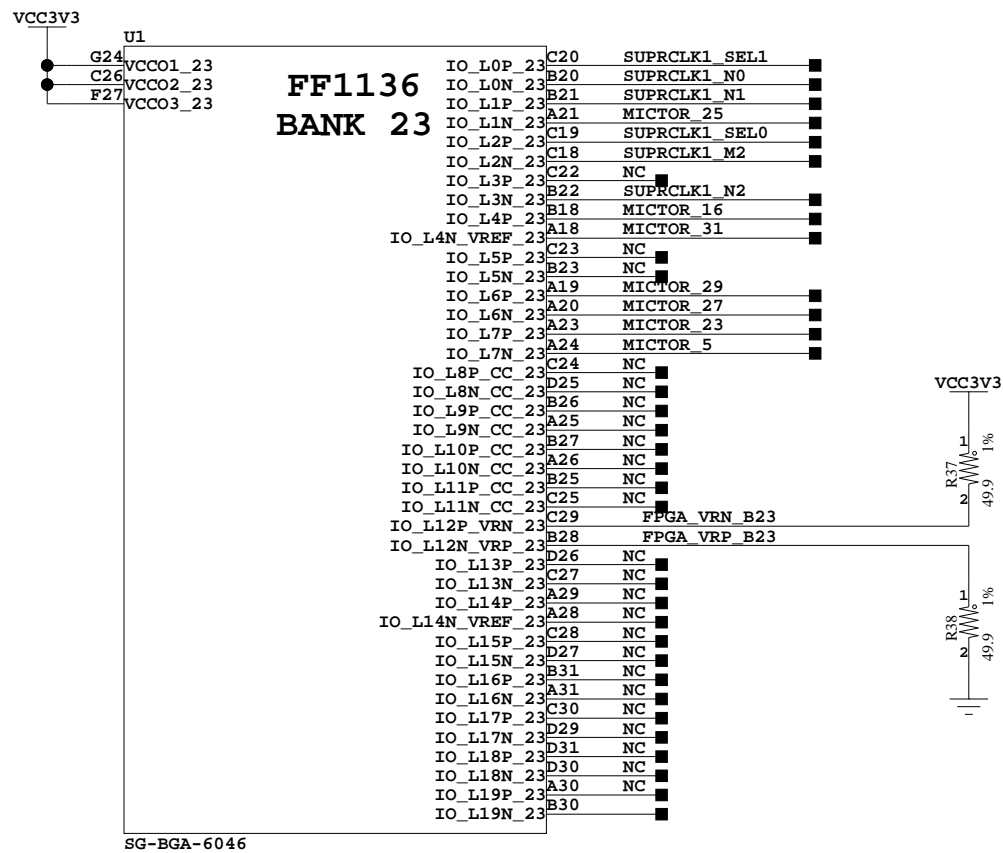
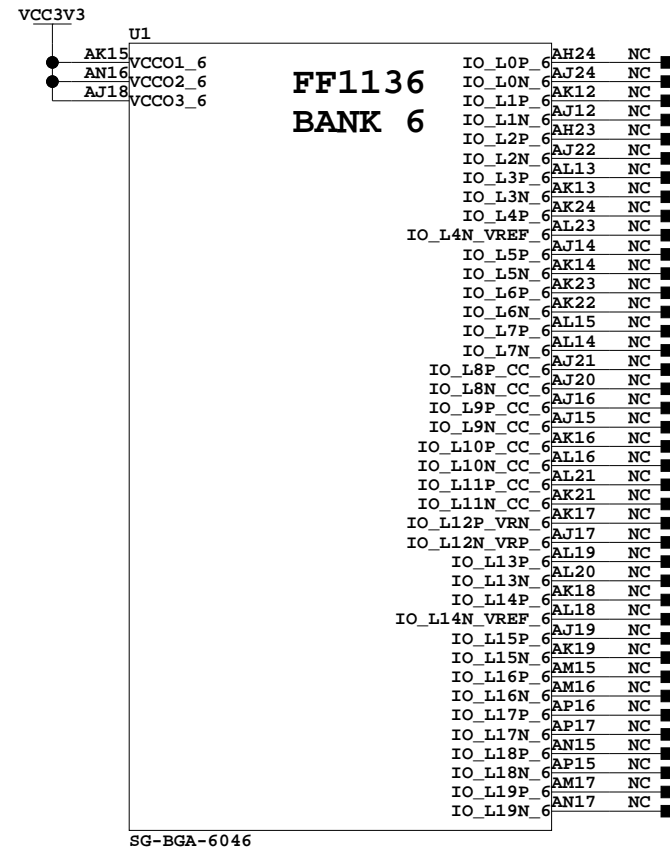
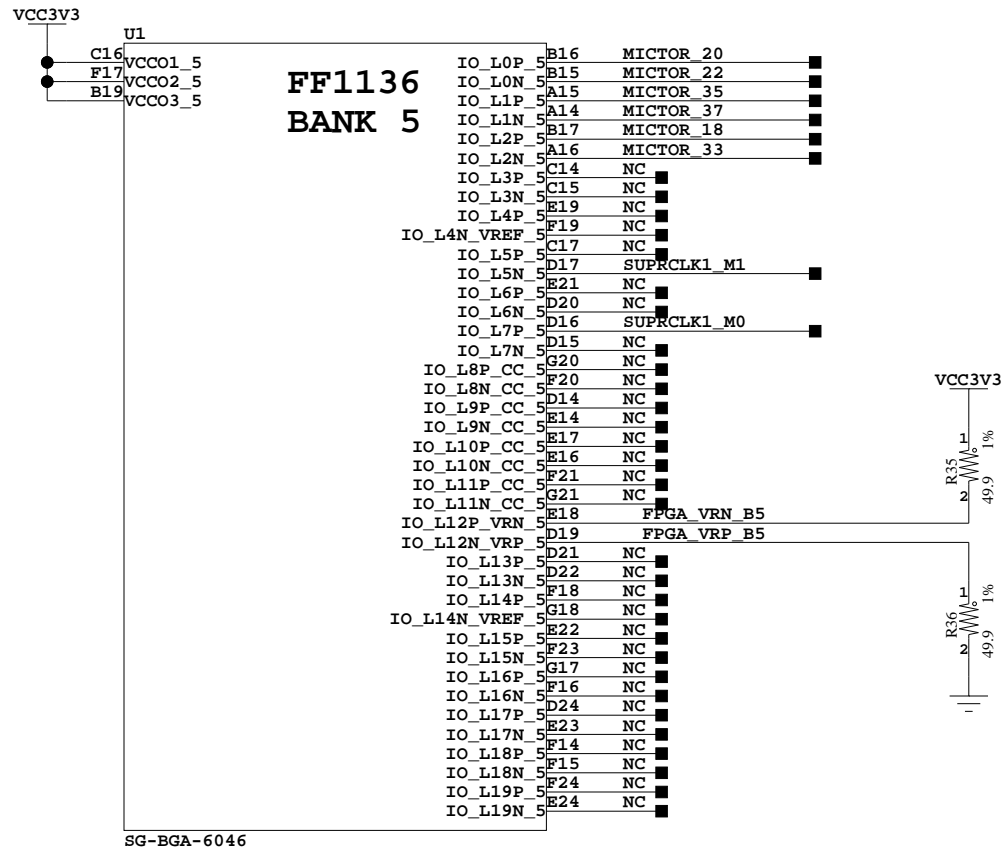


**Banks 11,12,13  
Sys ACE, XGI,  
PHY, LCD**



Title: Banks 11,12,13 Sys ACE, XGI, PHY, LCD SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
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Unused banks on the LX50T and SX50T

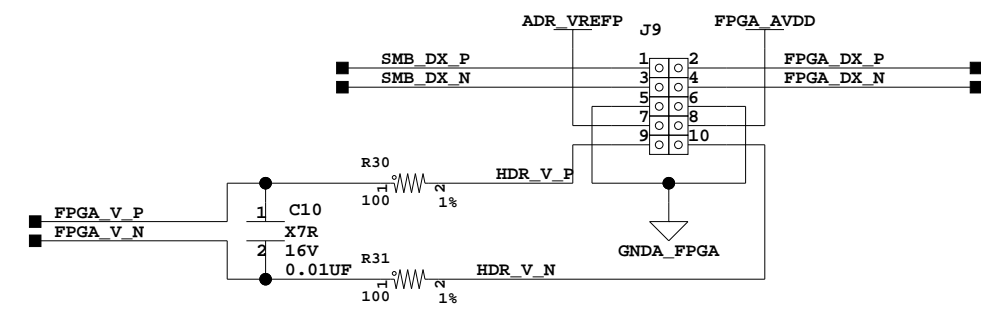


Banks 15, 17  
VGA, IIC, PHY  
SRAM, FLASH, GPIO

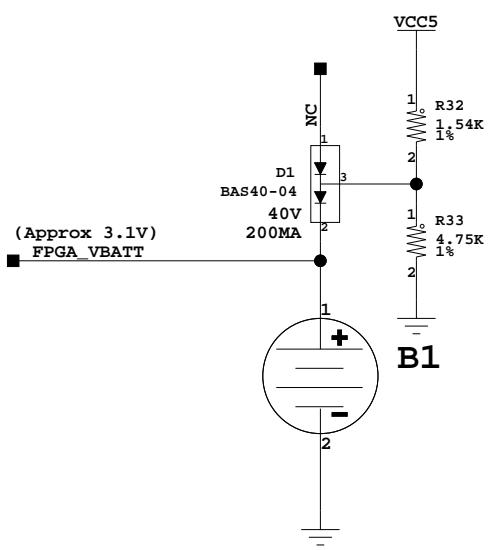


Title: Banks 11,12,13VGA, IIC, PHY, SRAM, GPIO SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
Sheet 5 of 27	Drawn By BP

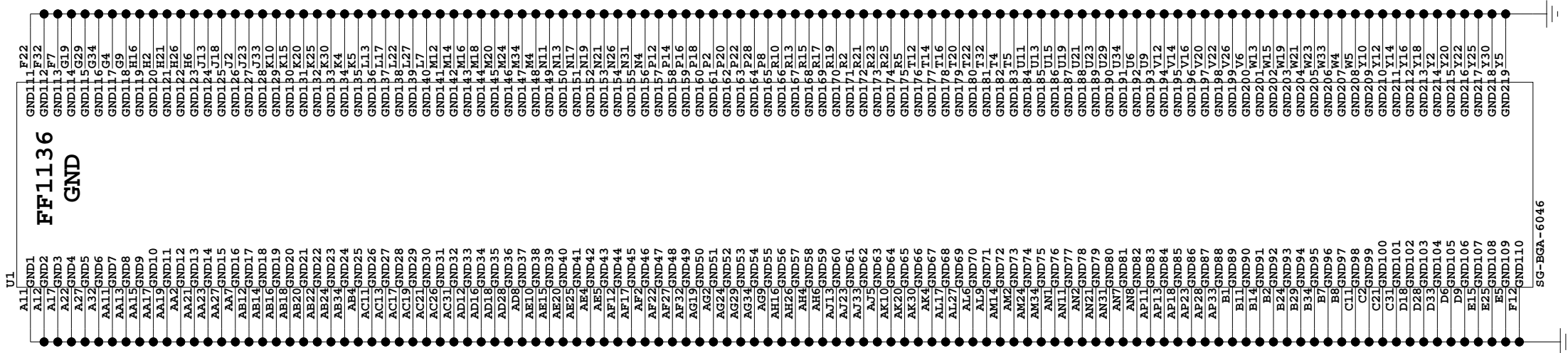
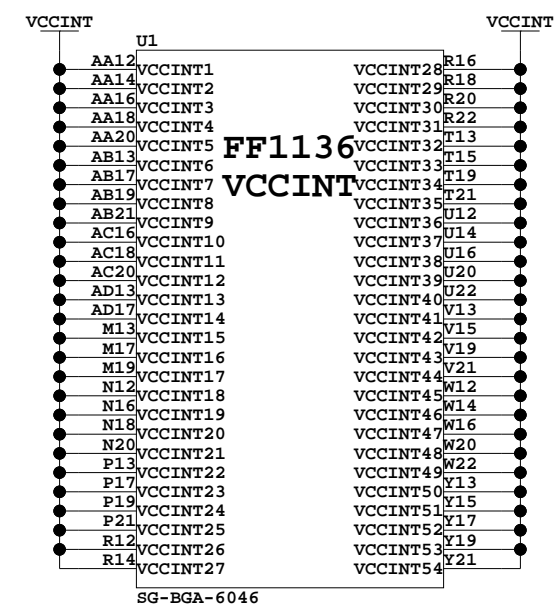
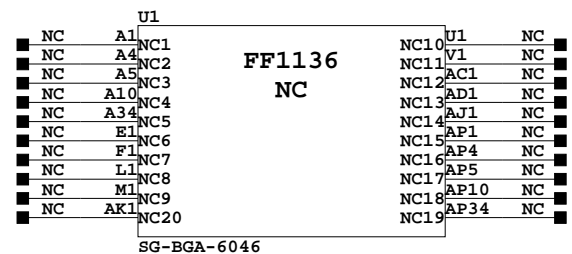
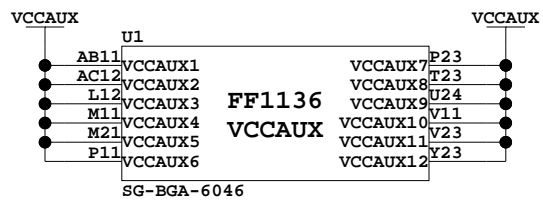
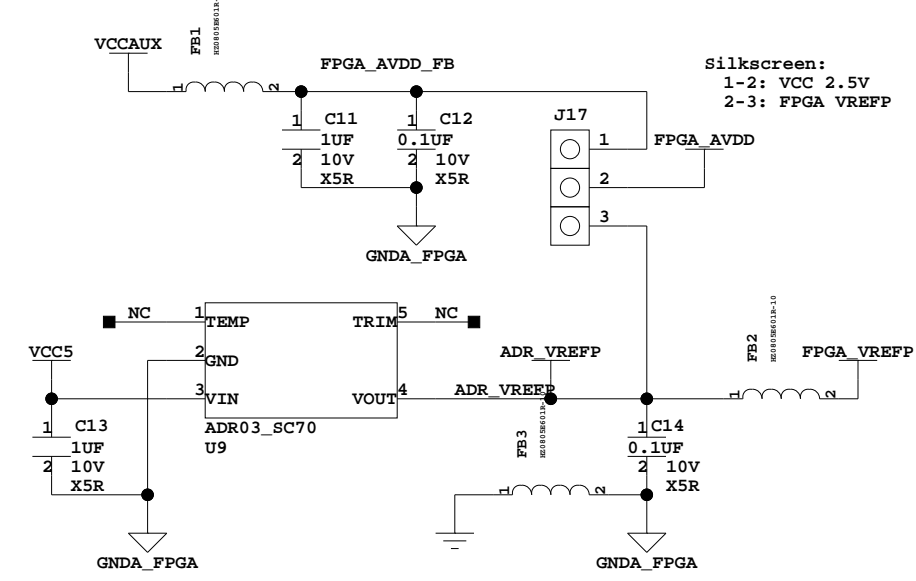
### System Monitor Header



### Rechargeable Battery



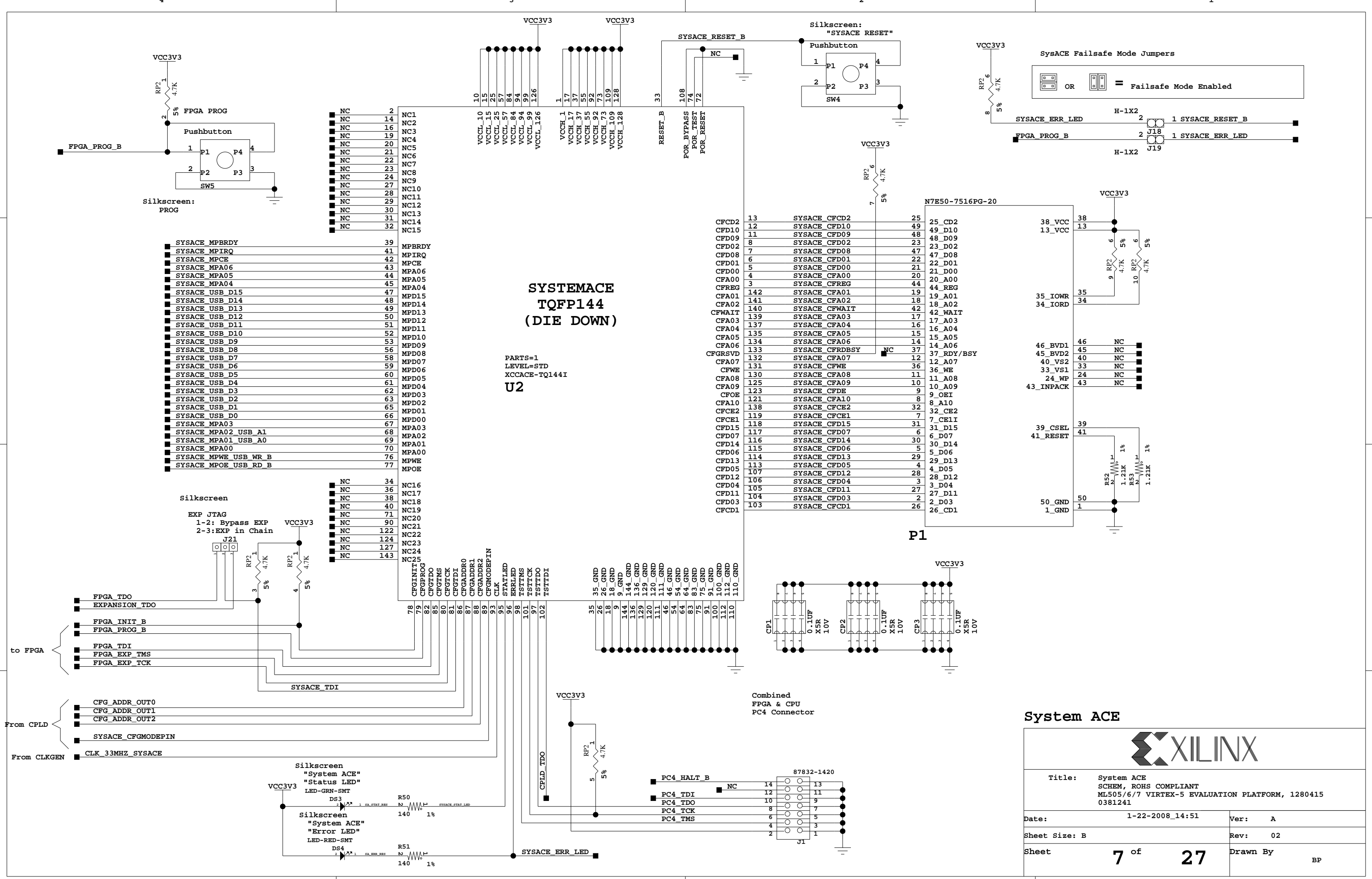
### FPGA AVDD Select



### Power and Misc FPGA Banks VCCINT, VCCAUX, NCs, GND Battery and System Monitor



Title: FPGA Misc, VCCINT, VCCAUX, GND, Sys Mon SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date: 1-22-2008_14:51	Ver: A	
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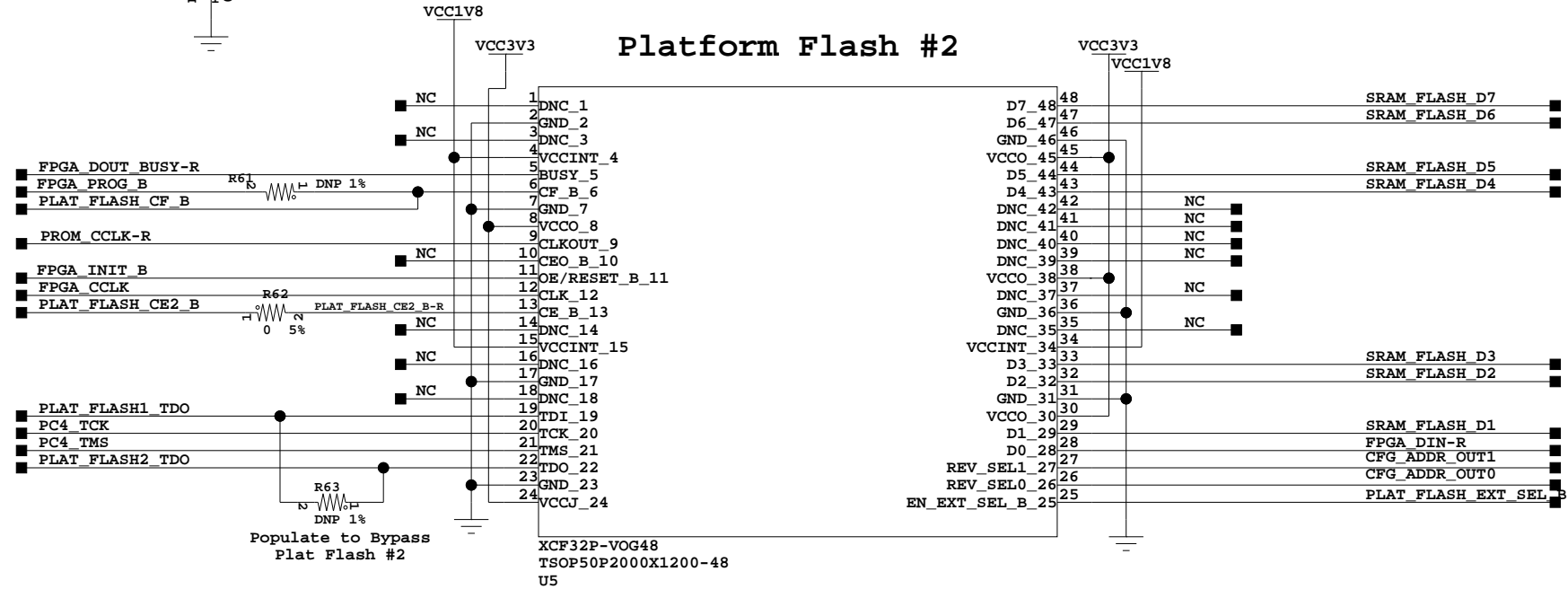
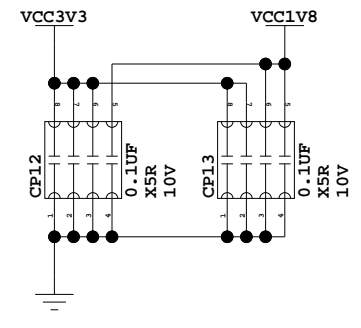
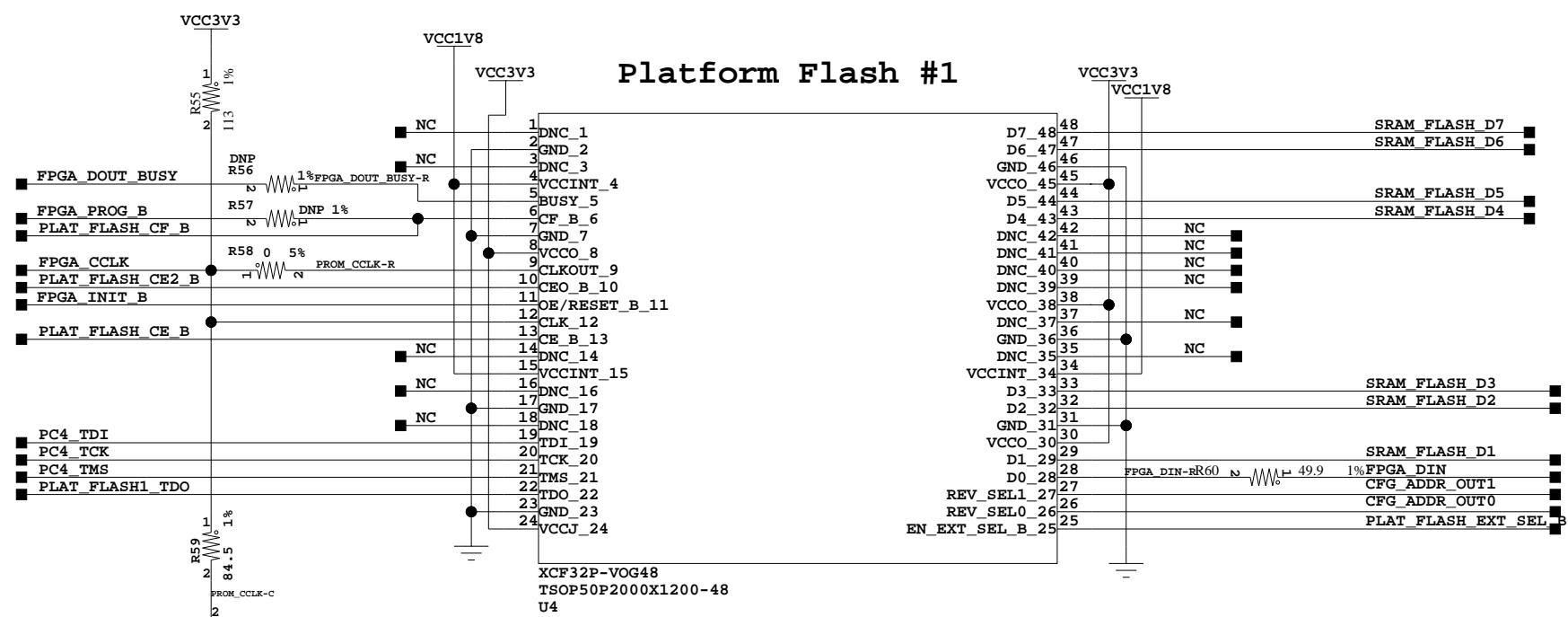
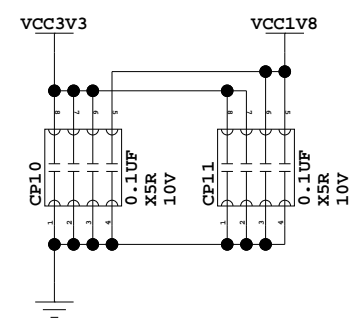
**System ACE**

Title: System ACE  
SCHEM, ROHS COMPLIANT  
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
0381241

Date: 1-22-2008\_14:51 Ver: A

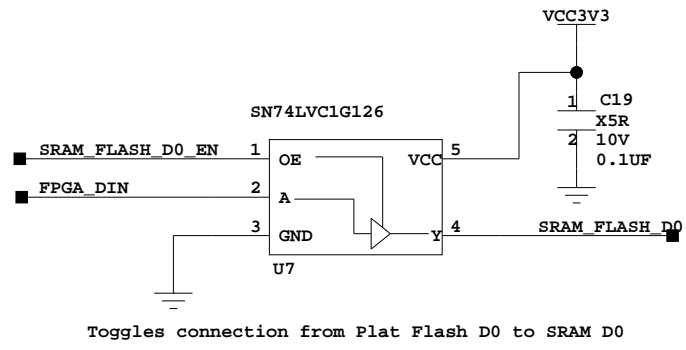
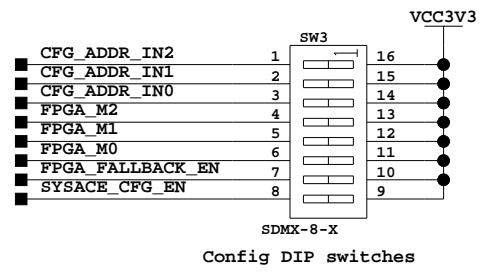
Sheet Size: B Rev: 02

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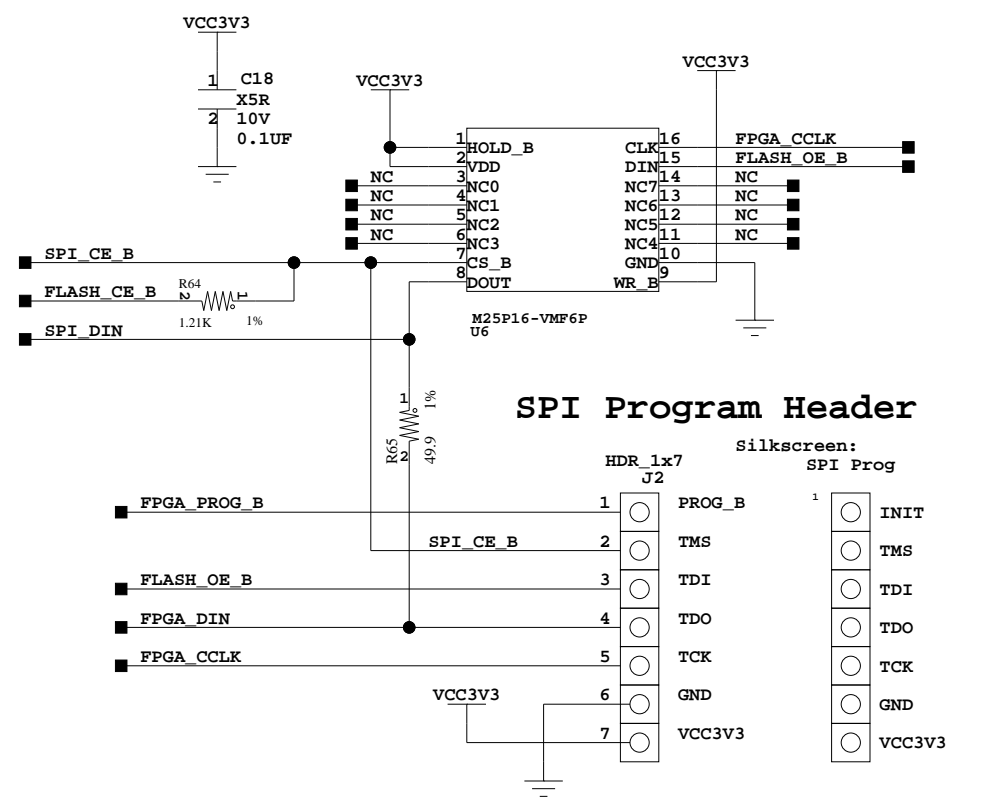


Populate to Bypass Plat Flash #2

Silkscreen:  
SysACE Config, Mode pins

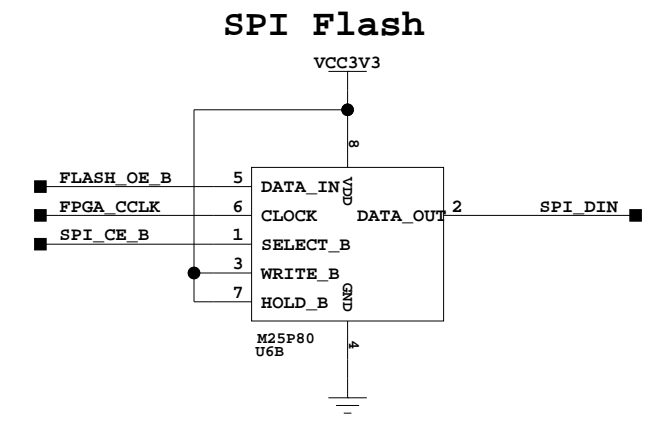
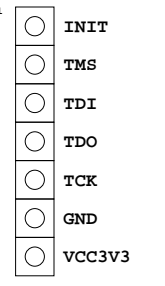


Toggles connection from Plat Flash D0 to SRAM D0



SPI Program Header

Silkscreen:  
SPI Prog



SPI Flash

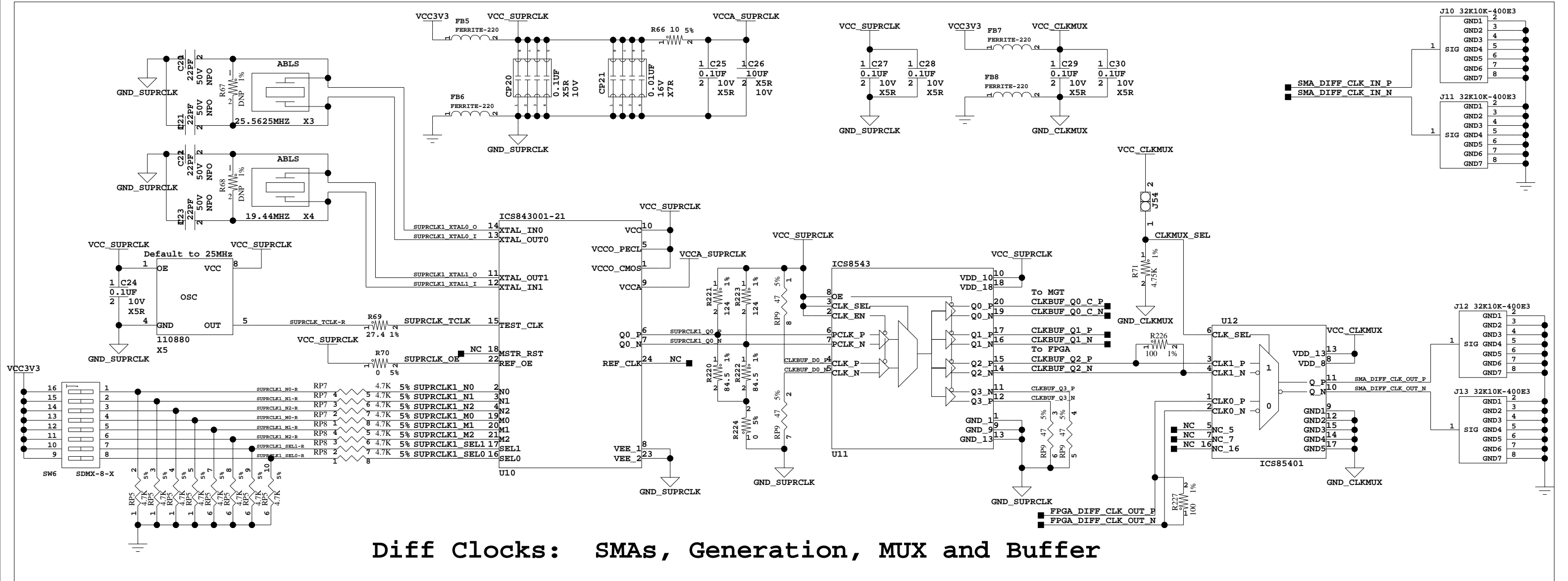
Misc Config  
Platform Flash,  
SPI Flash



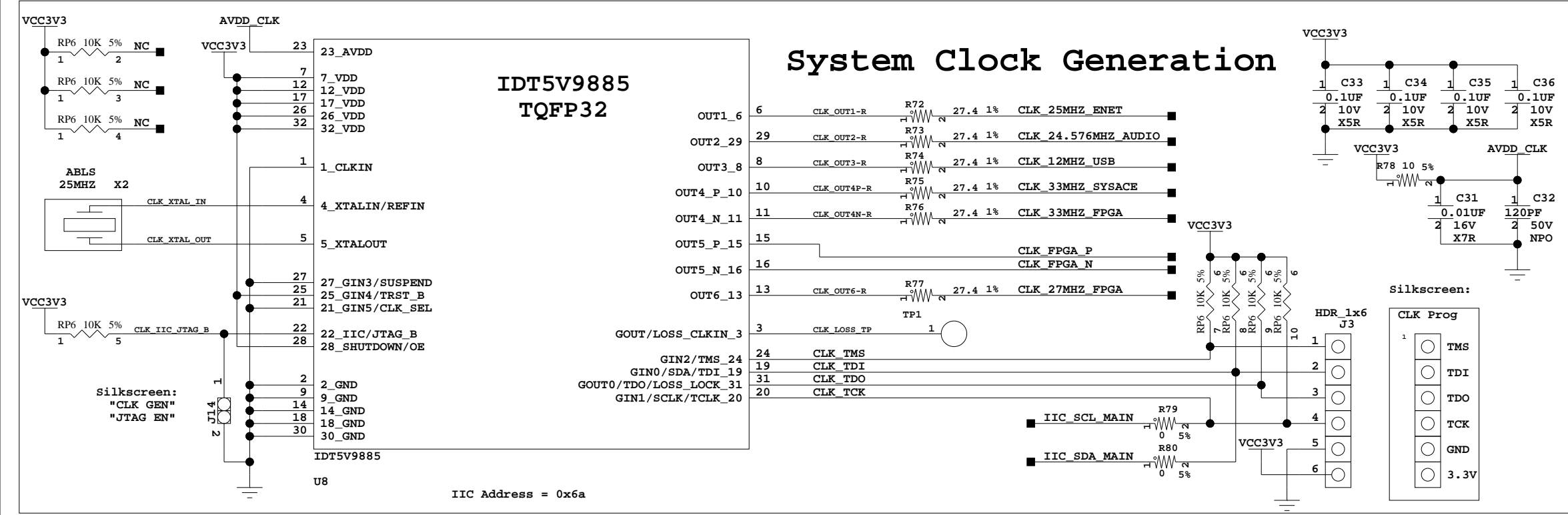
Title: Misc Config, Platform Flash, SPI Flash  
SCHEM, ROHS COMPLIANT  
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
0381241

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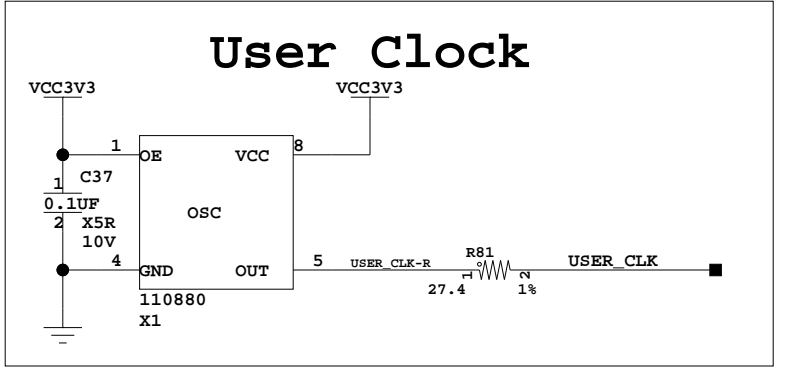




**Diff Clocks: SMAs, Generation, MUX and Buffer**



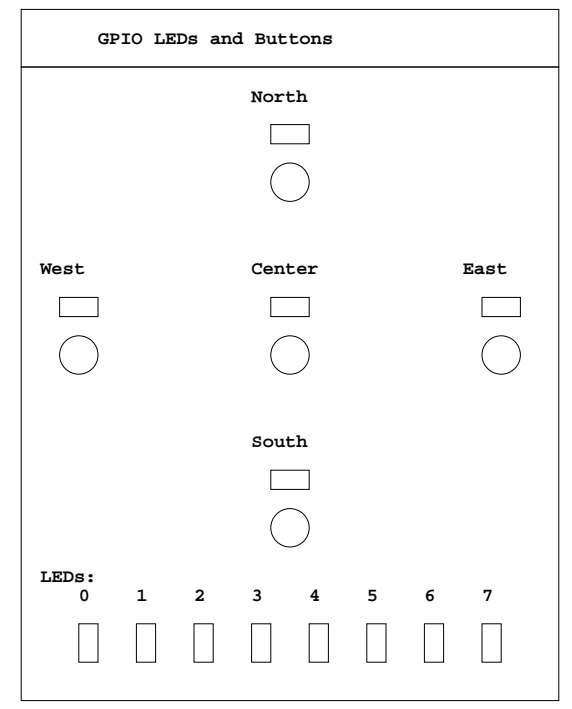
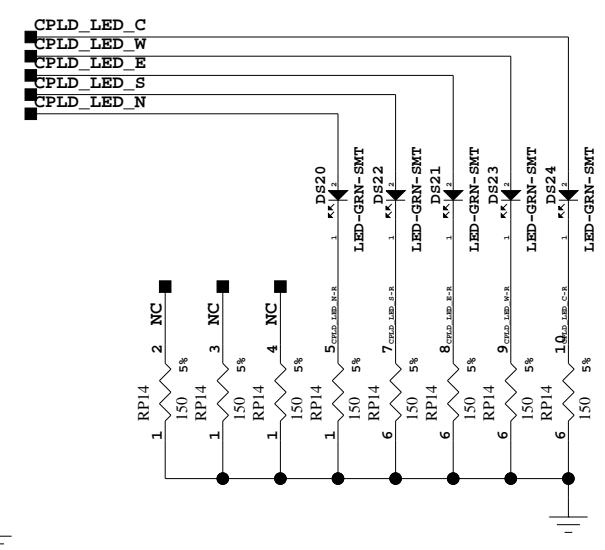
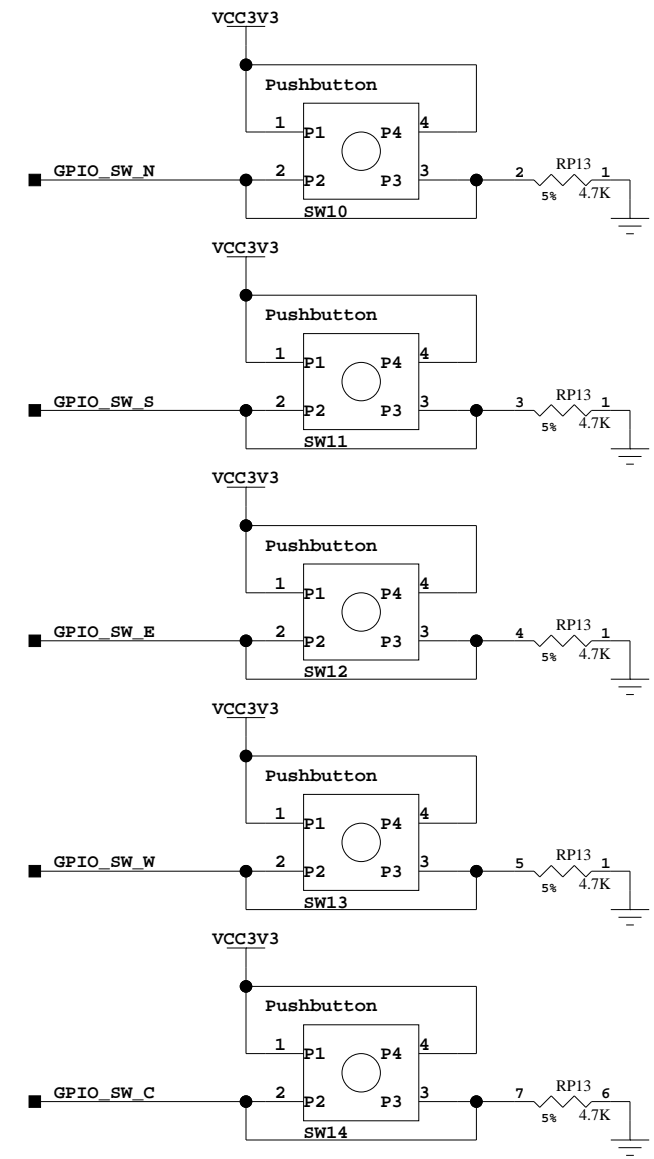
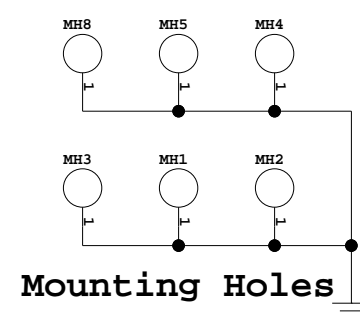
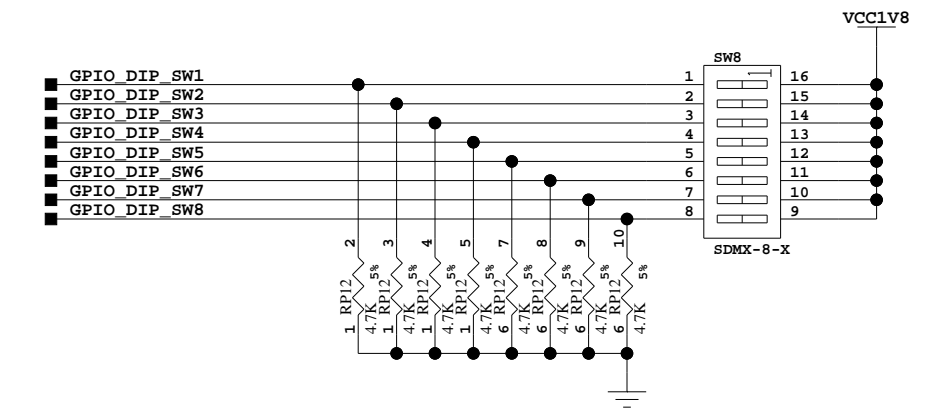
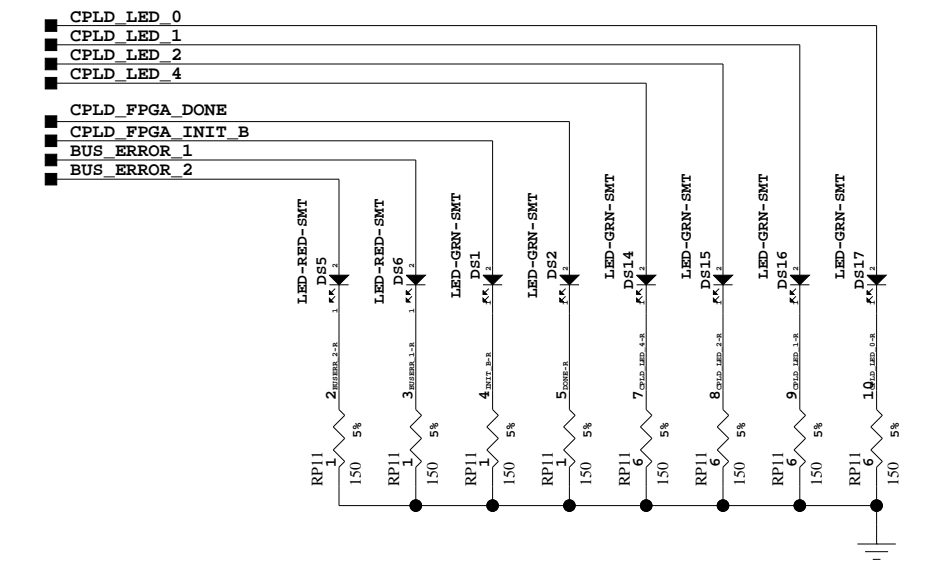
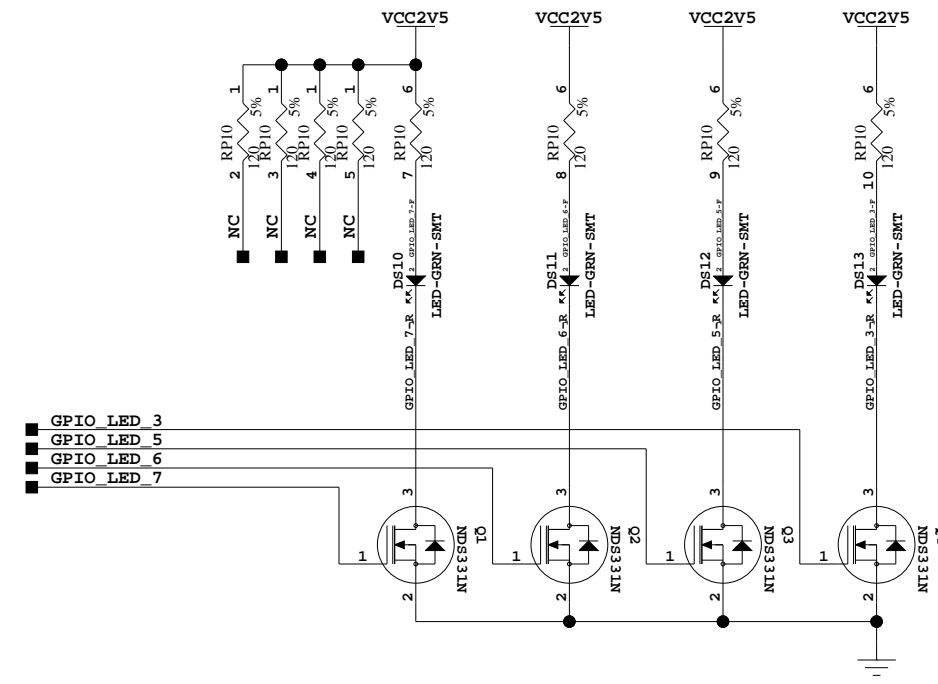
**System Clock Generation**



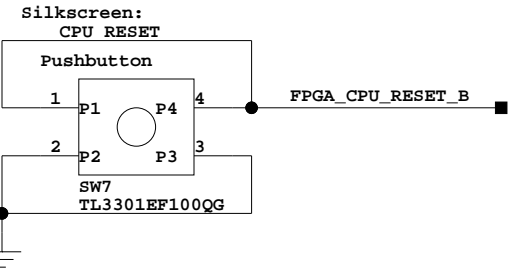
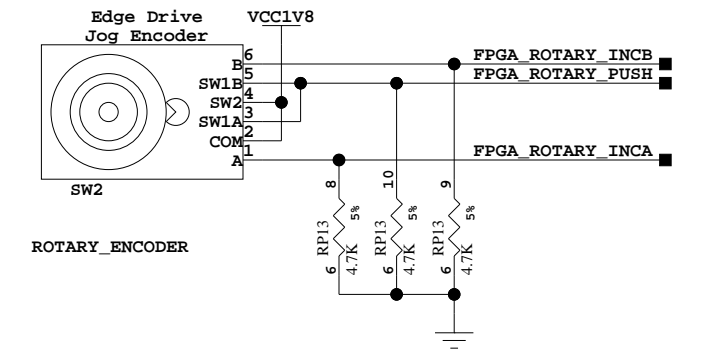
**Clocking - Differential Clock, System Clock & User Clock**



Title: Differential Clock, System Clock, User Clock SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date: 1-22-2008_14:51	Ver: A	
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**Edge Drive Jog Encoder Switch**

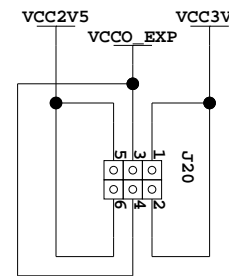
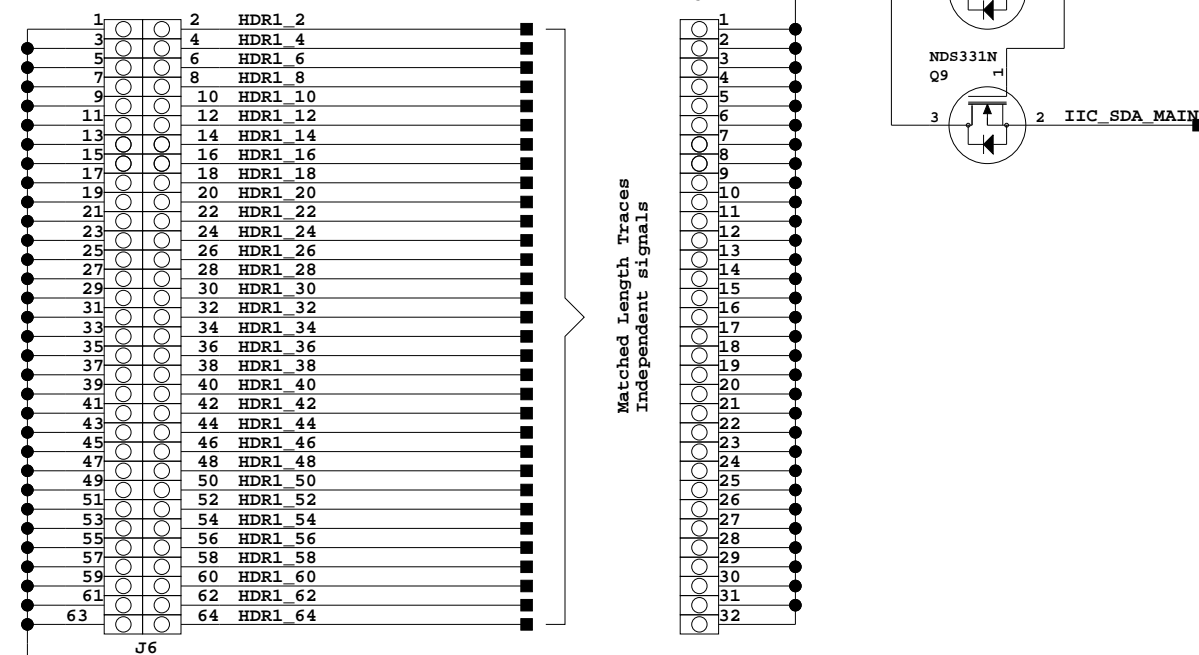
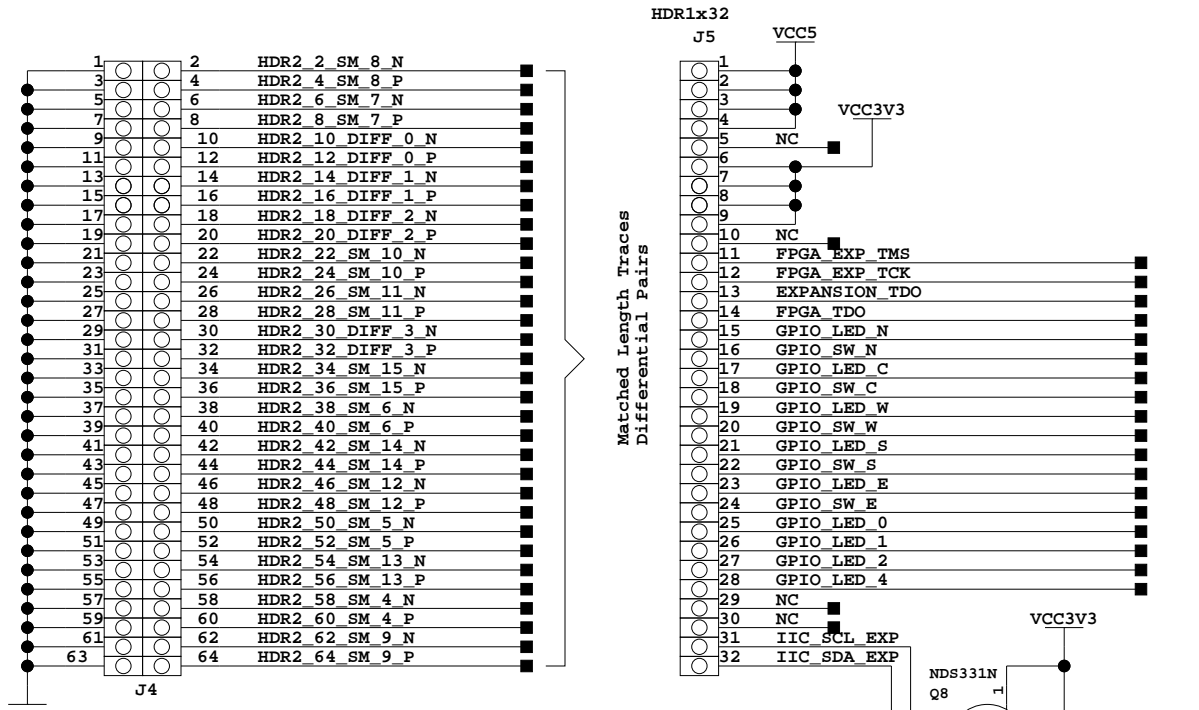


**GPIO - Buttons, LEDs, Switches**



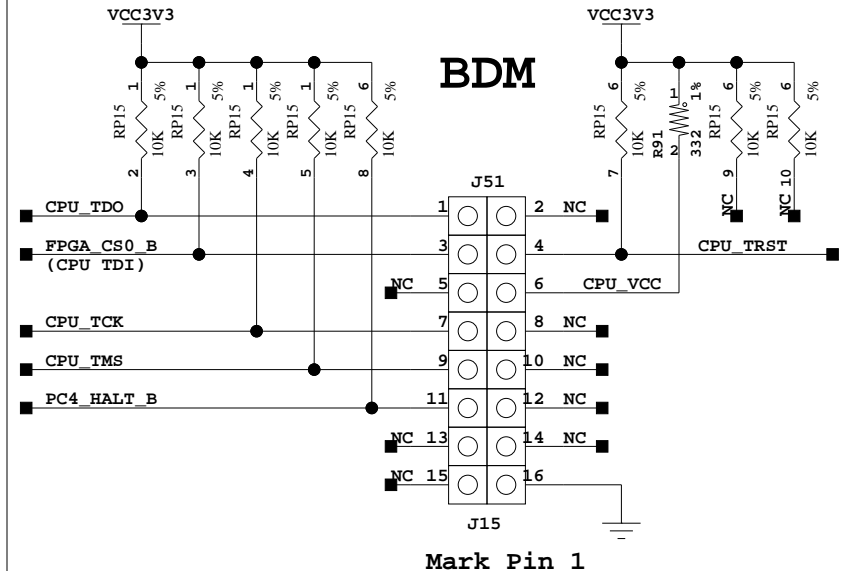
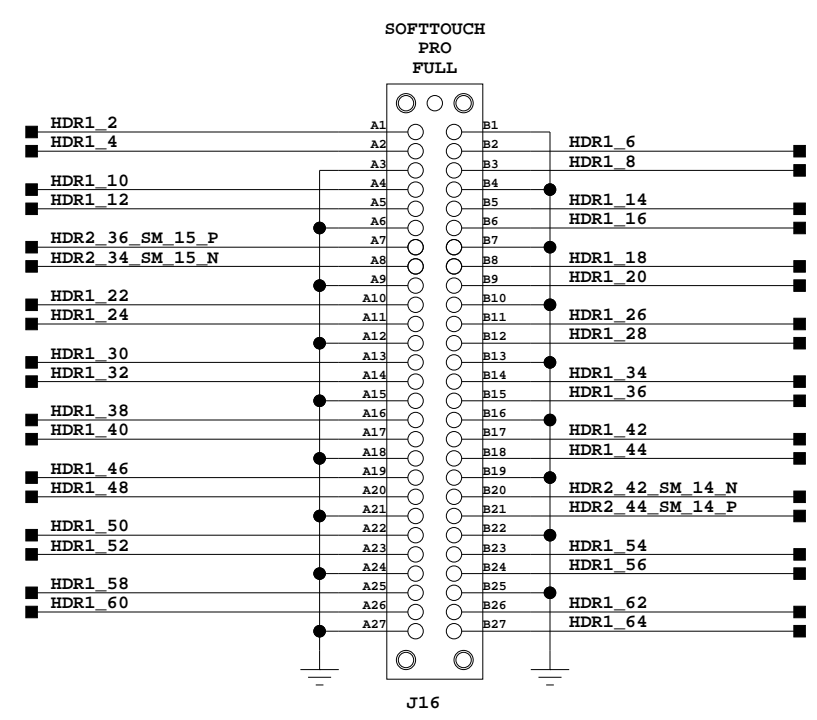
Title: GPIO Buttons, LEDs, Switches SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241		
Date: 1-22-2008_14:51	Ver: A	
Sheet Size: B	Rev: 02	
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# XGI Expansion Interface



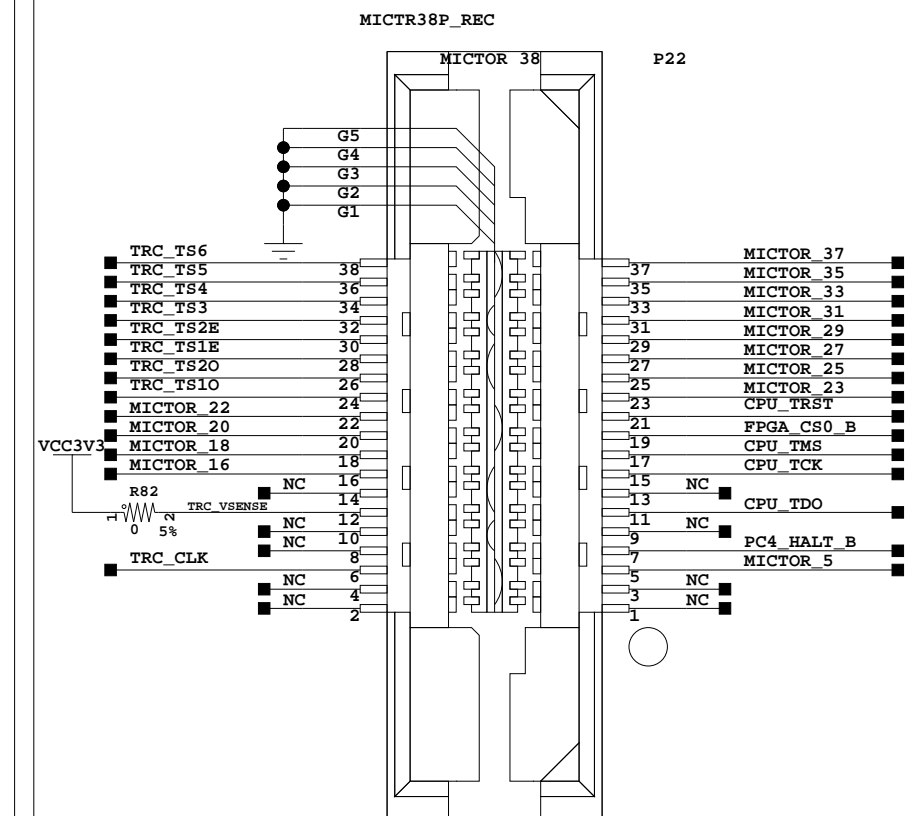
Bank 11/13 Expansion Connector Voltage  
 1-3 & 2-4 = 3.3V  
 3-5 & 4-6 = 2.5V

# SoftTouch Pro



Mark Pin 1  
 Pin 14 must be removed.

# Mictor



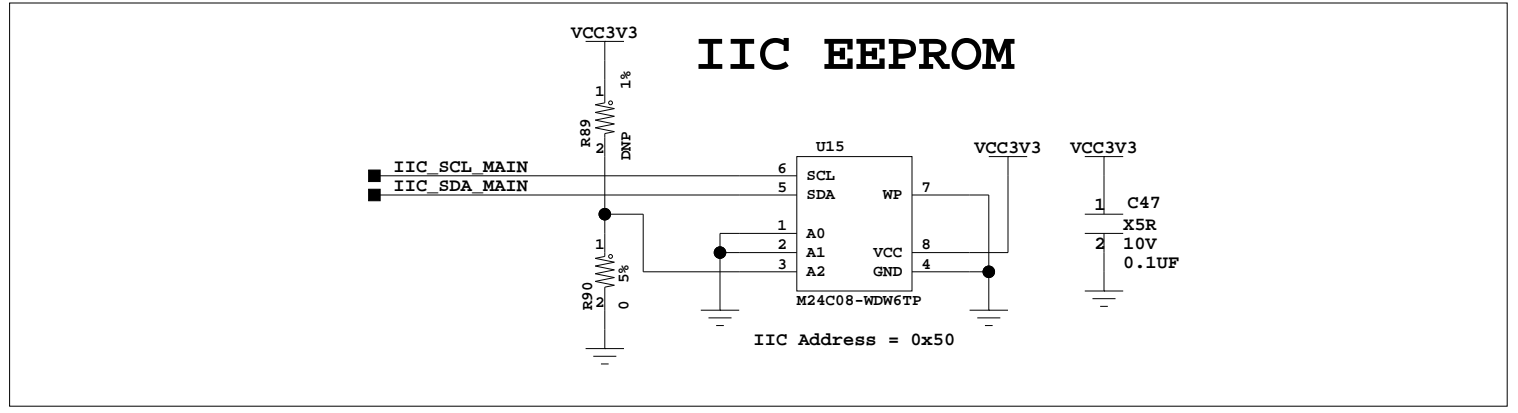
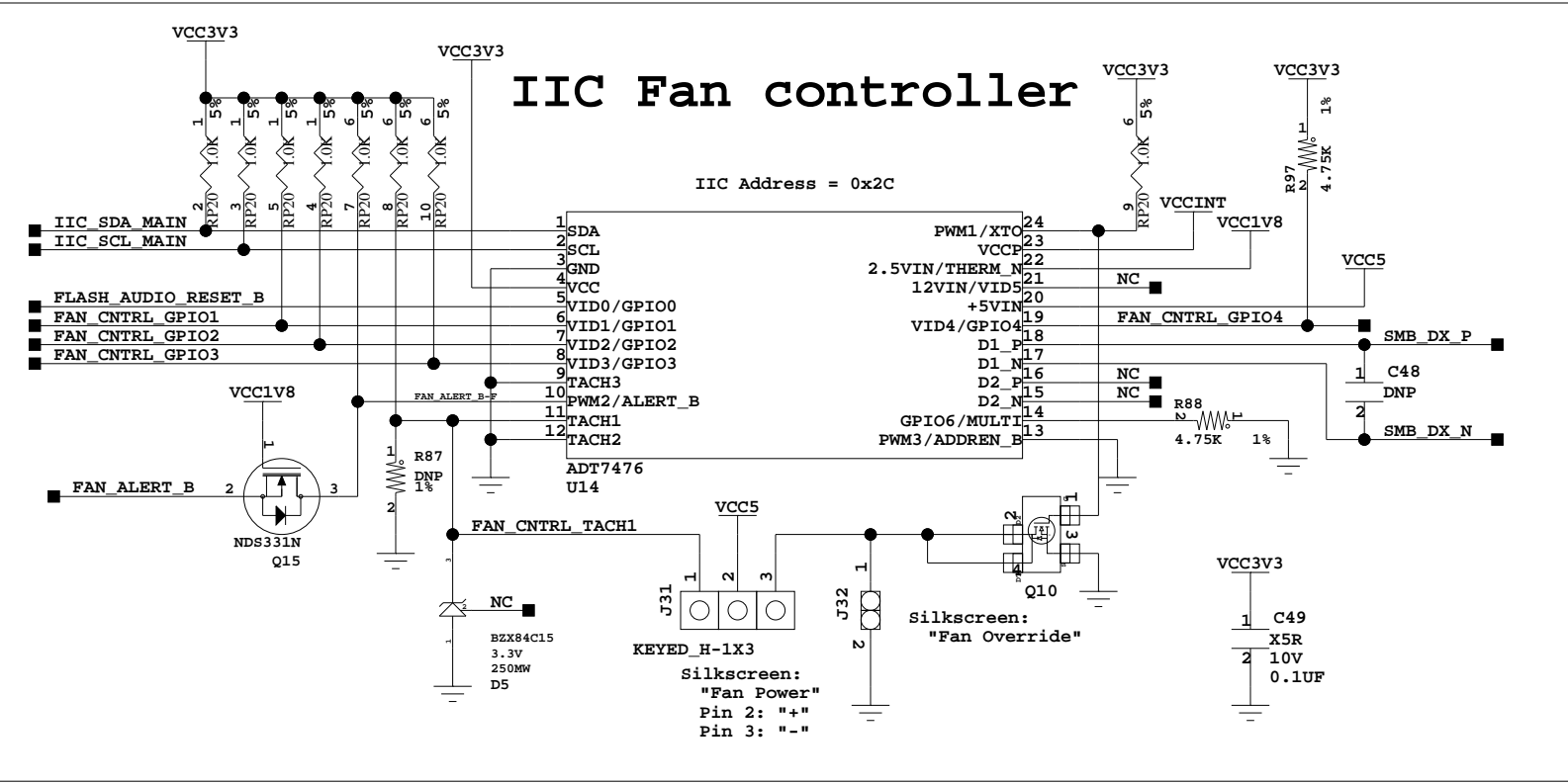
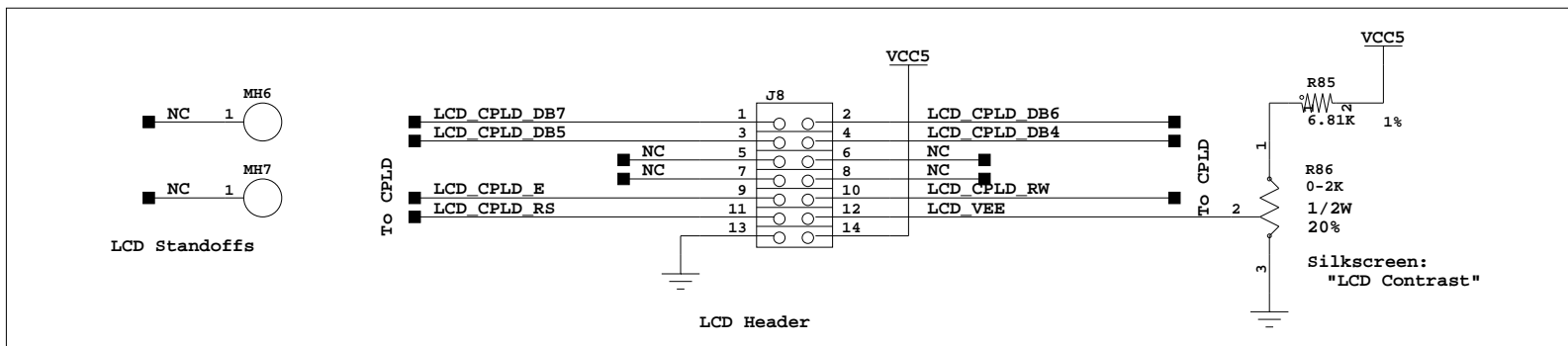
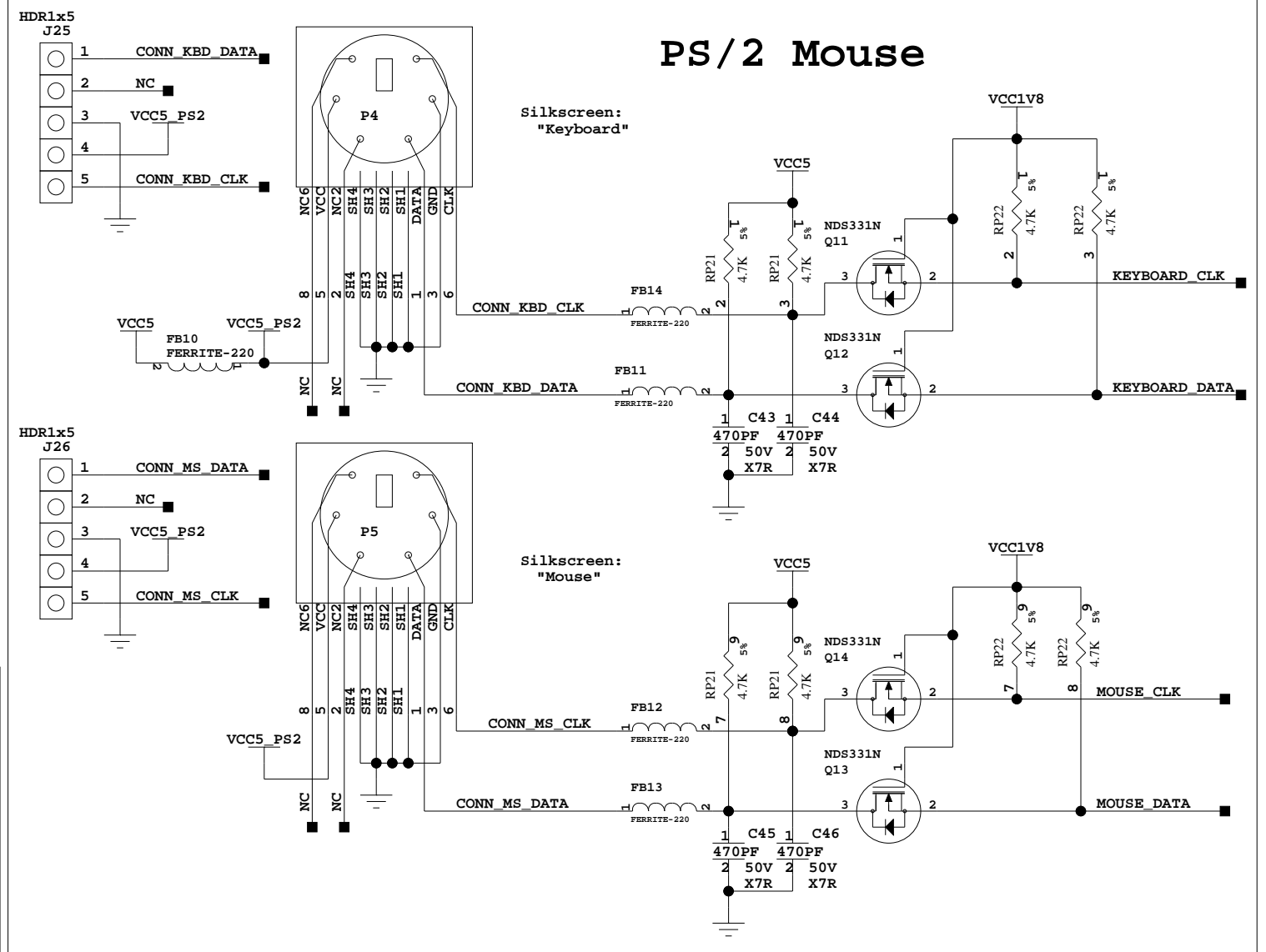
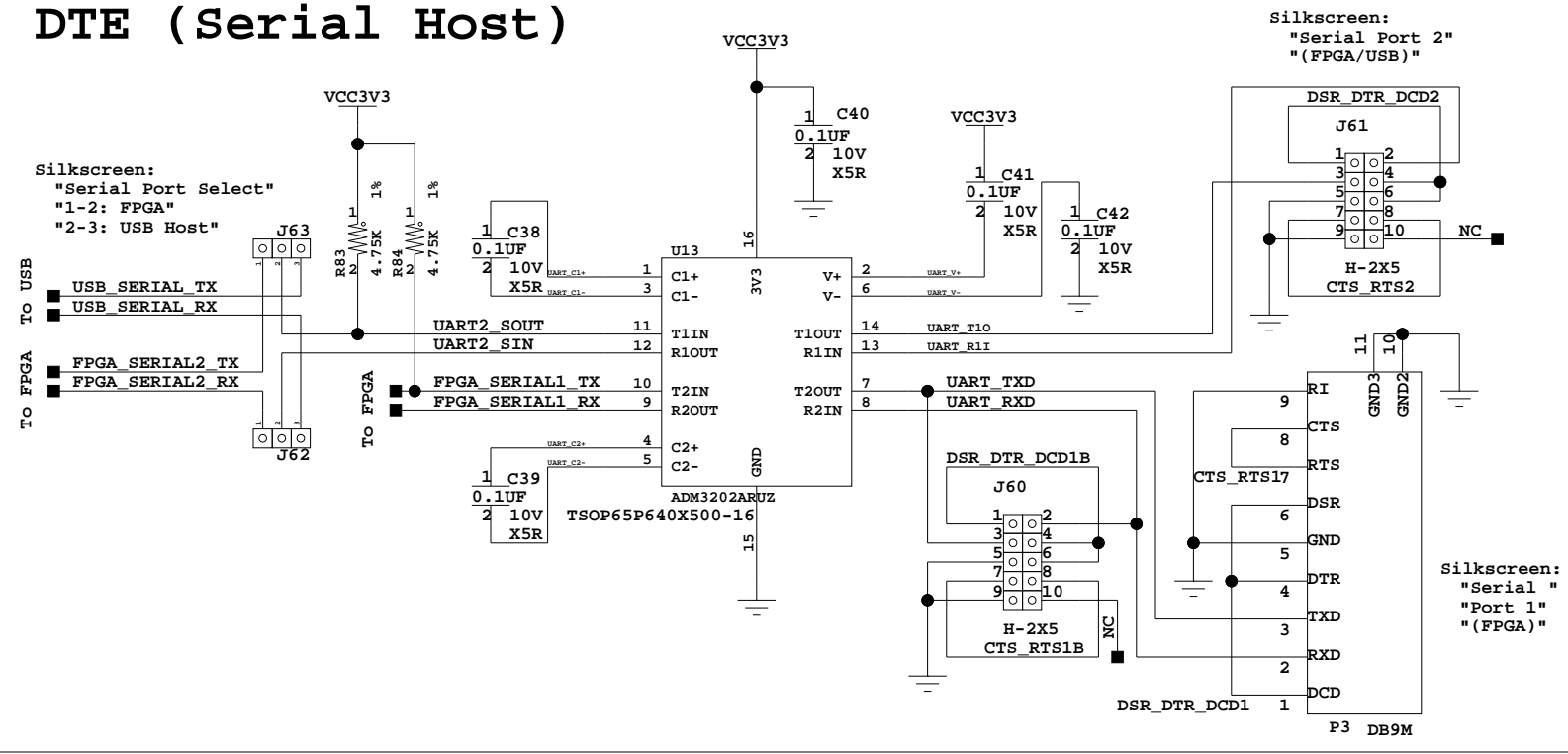
# XGI - Expansion Connector



Title: XGI - Expansion Headers  
 SCHEM, ROHS COMPLIANT  
 ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
 0381241

Date:	1-22-2008_14:51	Ver:	A
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# DTE (Serial Host)



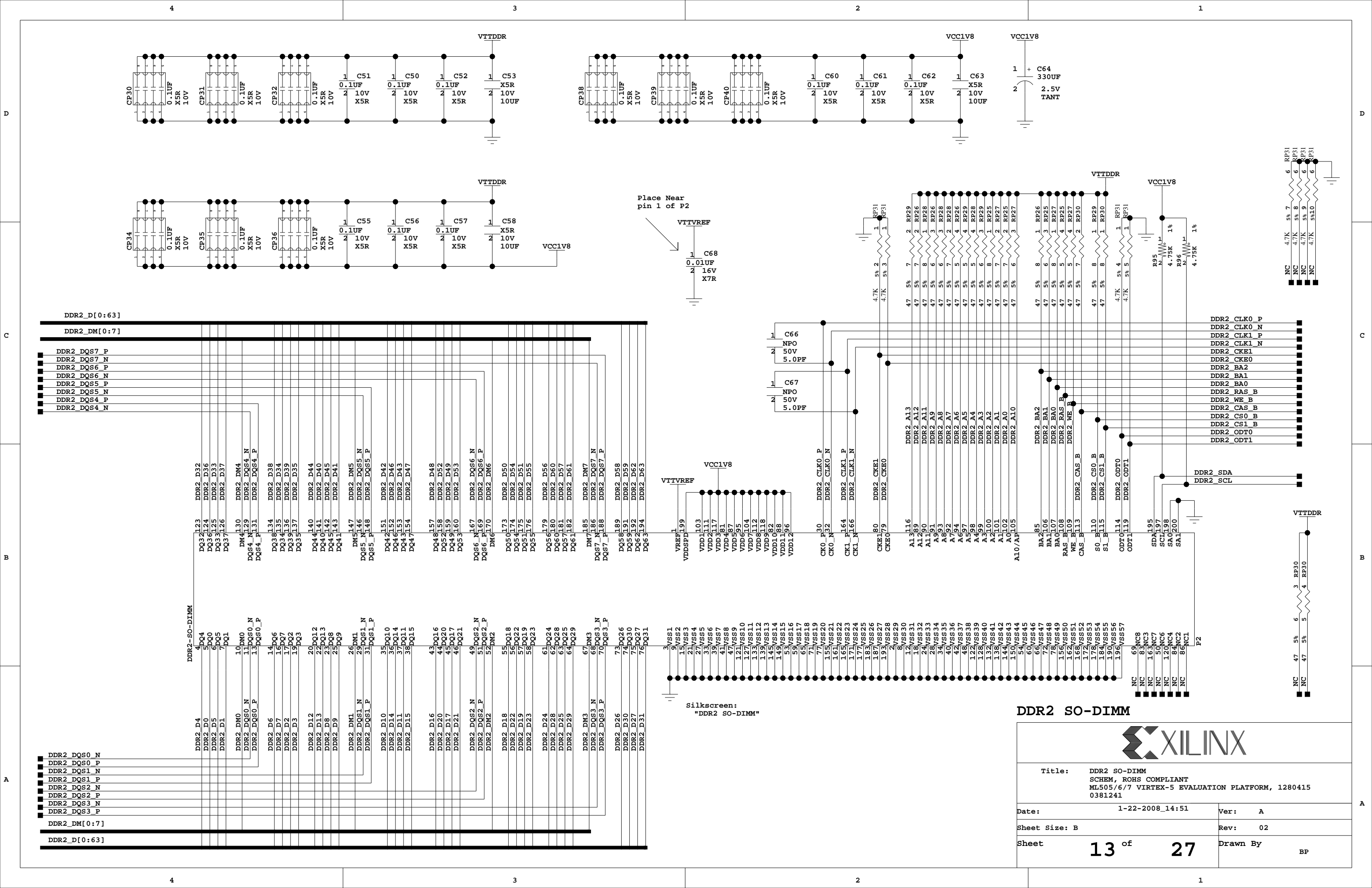
## Misc - LCD, PS2, UART, Fan Controller

**Title:** LCD, PS2, UART, IIC EEPROM, IIC Fan Controller SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241

**Date:** 1-22-2008\_14:55 **Ver:** A

**Sheet Size:** B **Rev:** 02

**Sheet** 12 **of** 27 **Drawn By** BP



### DDR2 SO-DIMM



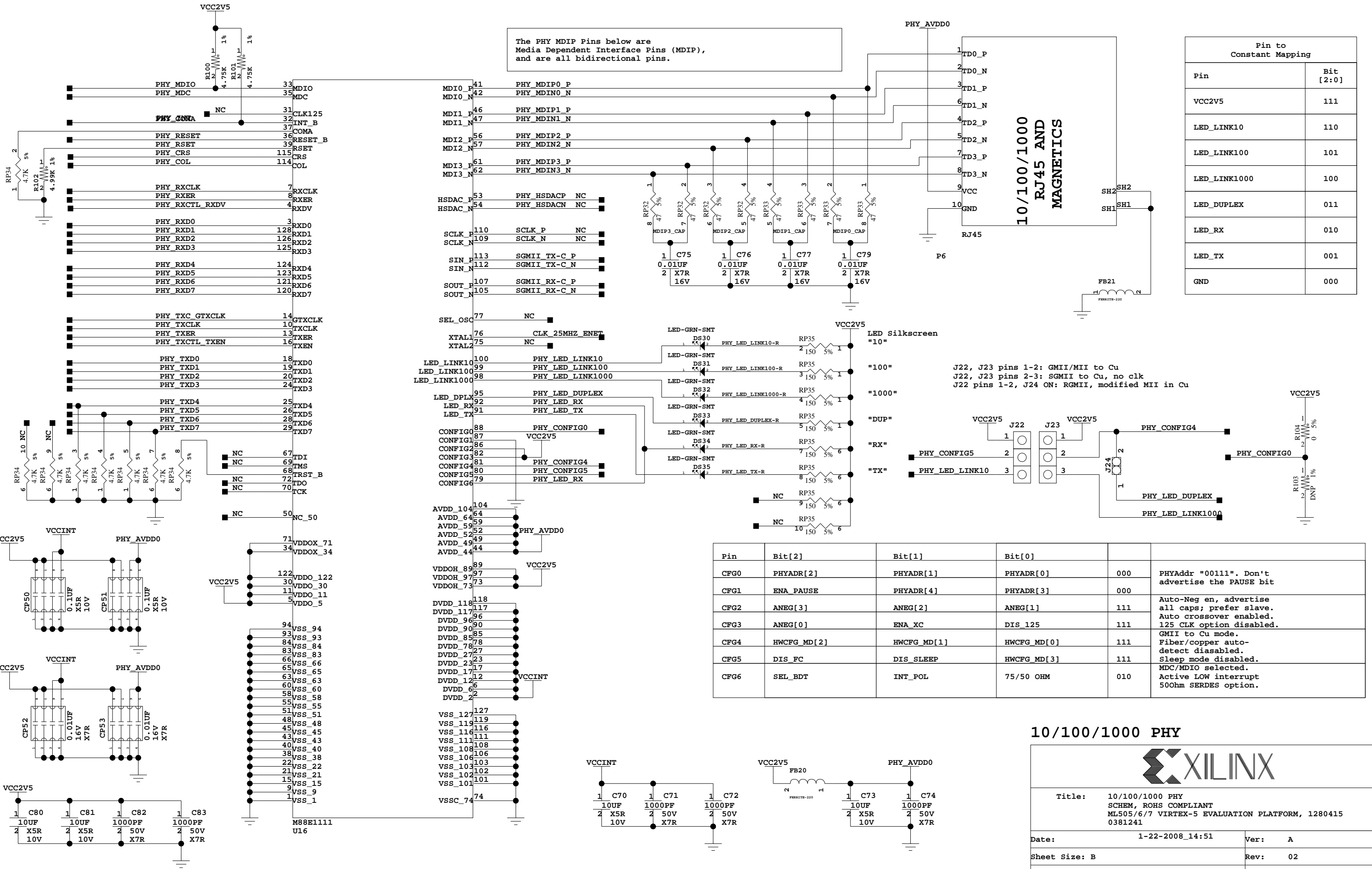
Title: DDR2 SO-DIMM  
 SCHEM, ROHS COMPLIANT  
 ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
 0381241

Date: 1-22-2008\_14:51 Ver: A

Sheet Size: B Rev: 02

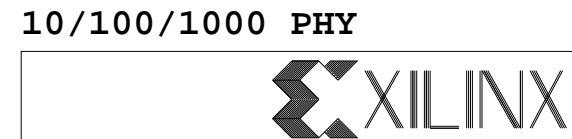
Sheet 13 of 27 Drawn By BP

The PHY MDIP Pins below are Media Dependent Interface Pins (MDIP), and are all bidirectional pins.



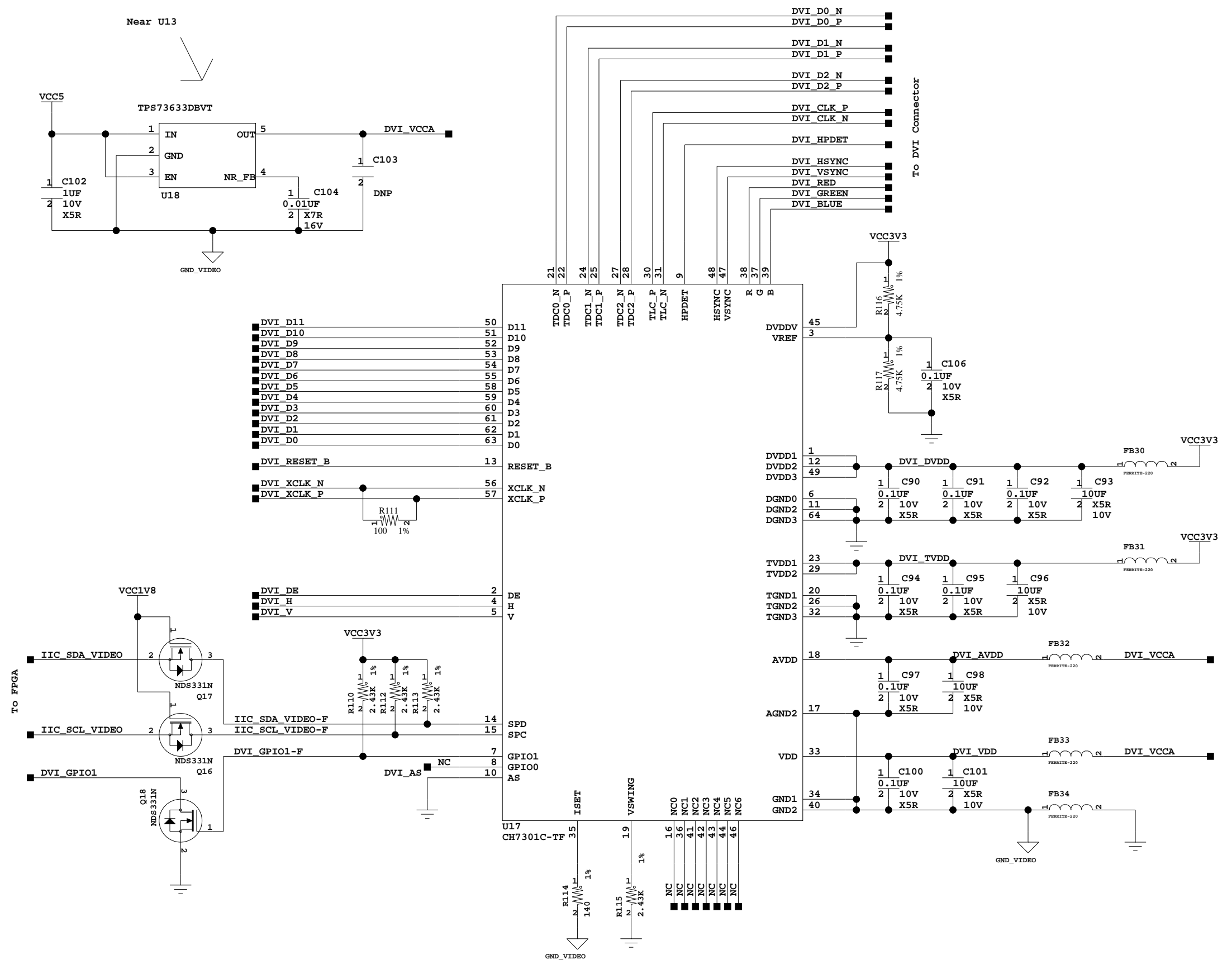
Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	000	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS 125	111	GMII to Cu mode. Fiber/copper auto-detect disabled. Sleep mode disabled.
CFG4	HWCFG MD[2]	HWCFG MD[1]	HWCFG MD[0]	111	MDC/MDIO selected. Active LOW interrupt 500hm SERDES option.
CFG5	DIS_FC	DIS_SLEEP	HWCFG MD[3]	111	
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	



Title: 10/100/1000 PHY SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241

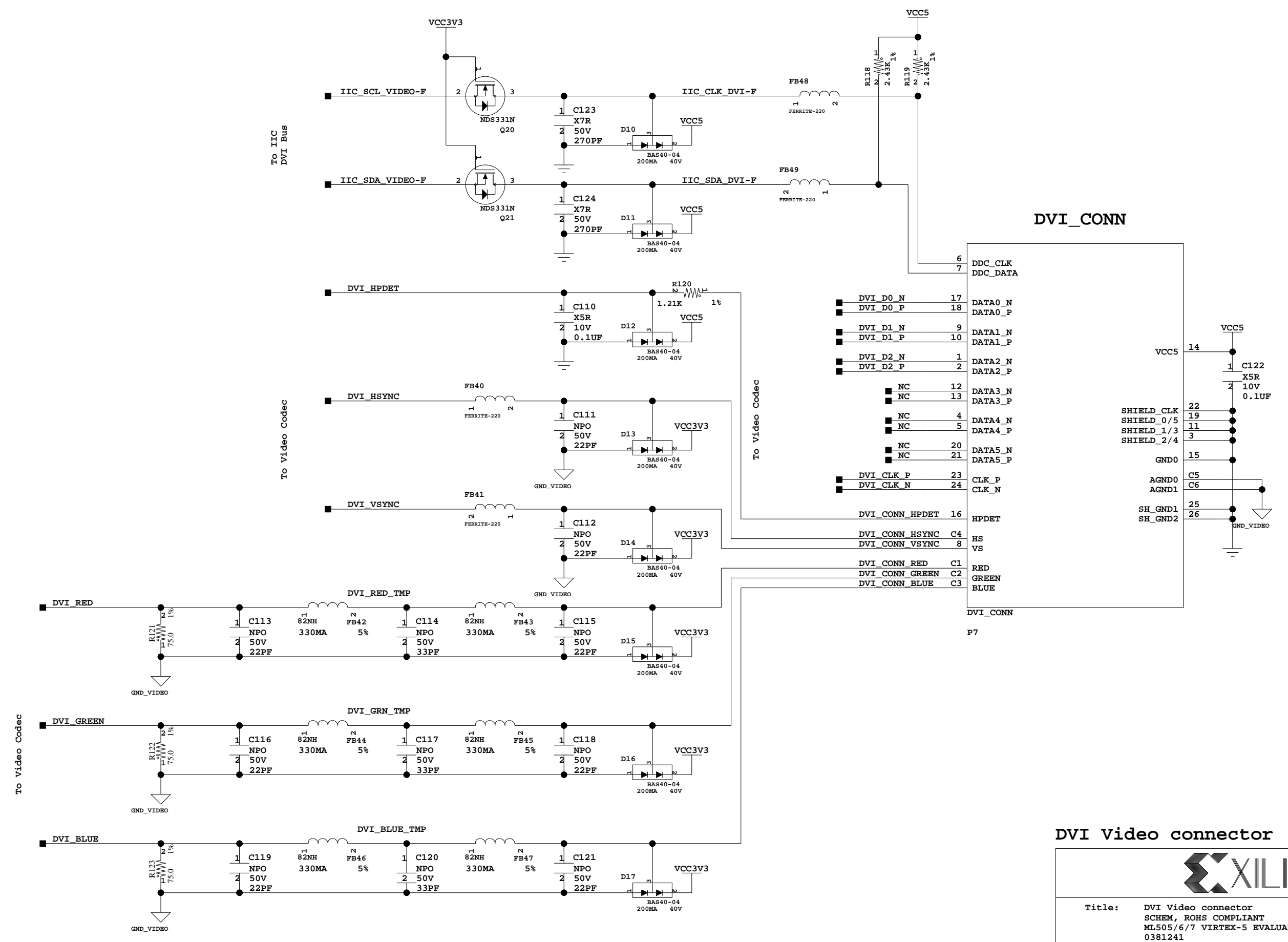
Date:	1-22-2008_14:51	Ver:	A
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IIC Address = 0x76

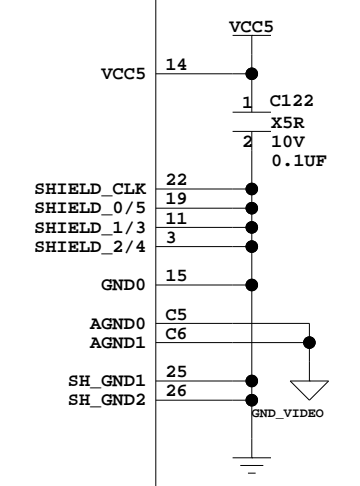
VGA Out Codec

Title: VGA Out Codec SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
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DVI\_CONN

6	DDC_CLK	
7	DDC_DATA	
17	DATA0_N	DVI D0 N
18	DATA0_P	DVI D0 P
9	DATA1_N	DVI D1 N
10	DATA1_P	DVI D1 P
1	DATA2_N	DVI D2 N
2	DATA2_P	DVI D2 P
12	DATA3_N	NC
13	DATA3_P	NC
4	DATA4_N	NC
5	DATA4_P	NC
20	DATA5_N	NC
21	DATA5_P	NC
23	CLK_P	DVI_CLK_P
24	CLK_N	DVI_CLK_N
16	HPDET	DVI_CONN_HPDET
C4	HS	DVI_CONN_HSYNC
8	VS	DVI_CONN_VSYNC
C1	RED	DVI_CONN_RED
C2	GREEN	DVI_CONN_GREEN
C3	BLUE	DVI_CONN_BLUE

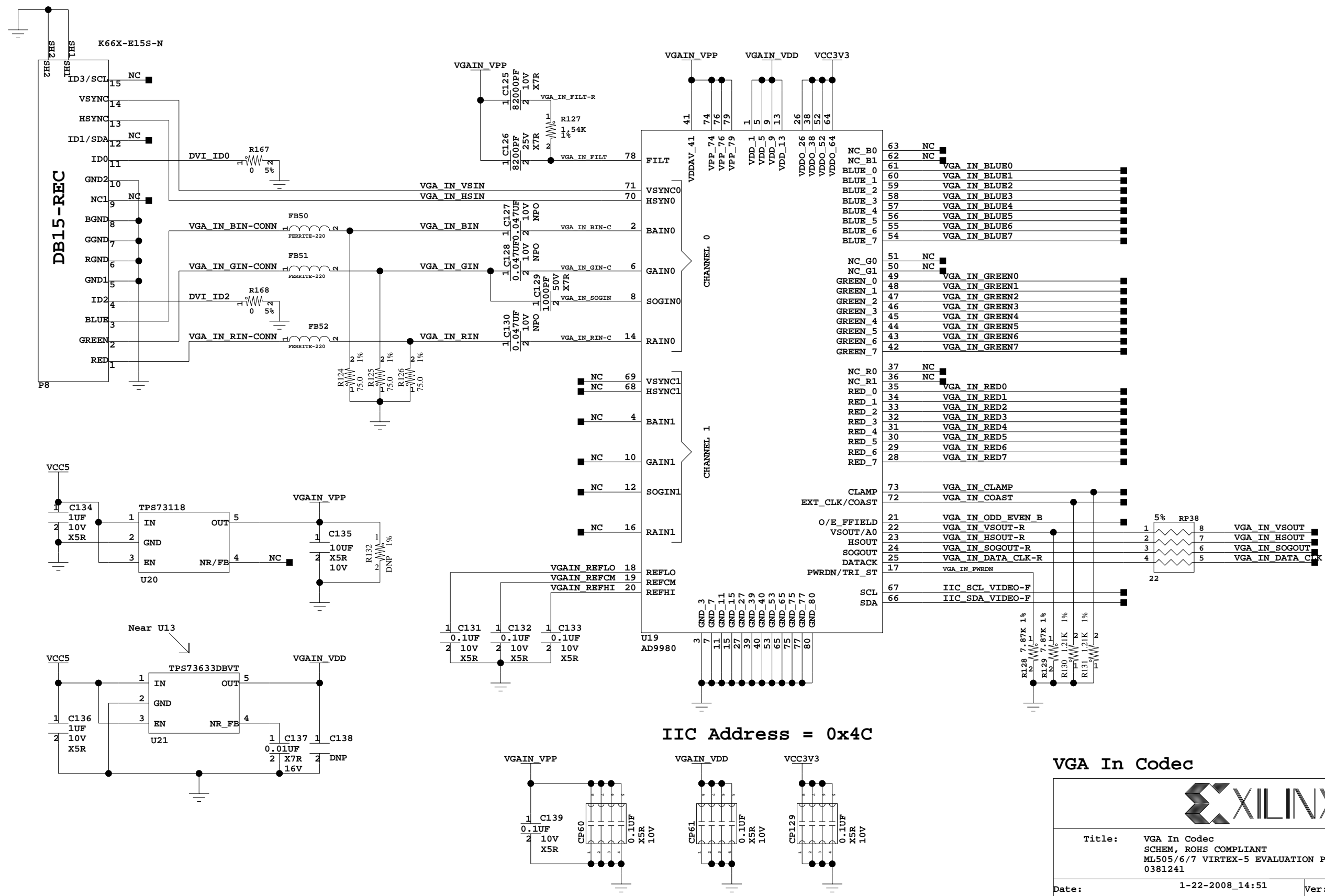


DVI Video connector




Title: DVI Video connector SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
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IIC Address = 0x4C

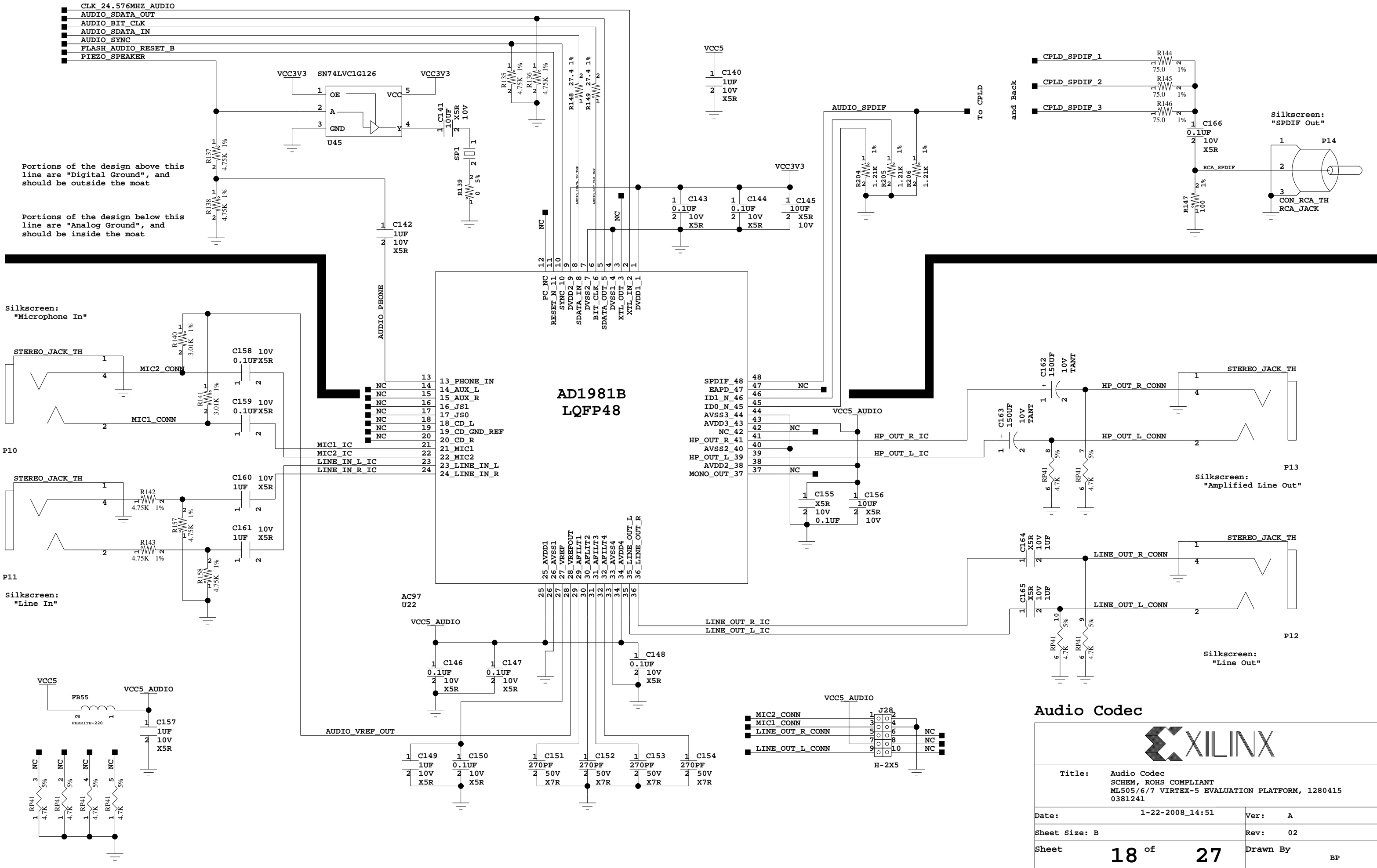
VGA In Codec

	
Title: VGA In Codec SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
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CLK 24.576MHZ AUDIO  
 AUDIO\_SDATA\_OUT  
 AUDIO\_BIT\_CLK  
 AUDIO\_SDATA\_IN  
 AUDIO\_SYNC  
 FLASH\_AUDIO\_RESET\_B  
 PIEZO\_SPEAKER

Portions of the design above this line are "Digital Ground", and should be outside the moat

Portions of the design below this line are "Analog Ground", and should be inside the moat



Audio Codec



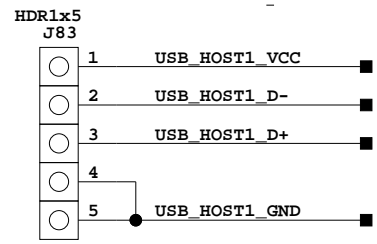
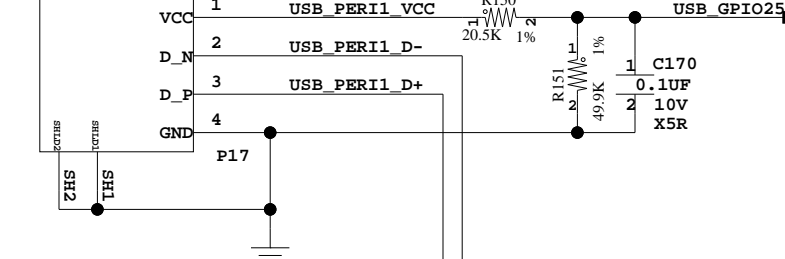
Title: Audio Codec  
 SCHEM, ROHS COMPLIANT  
 ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
 0381241

Date: 1-22-2008\_14:51 Ver: A

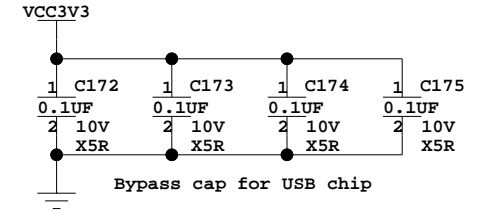
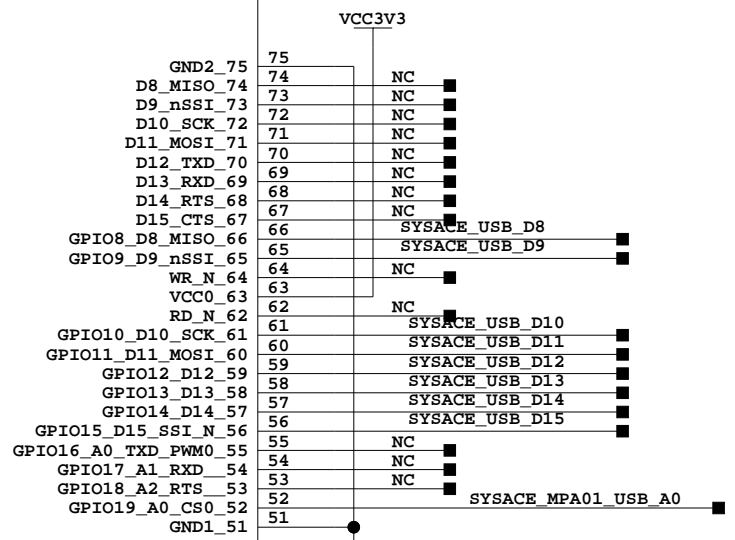
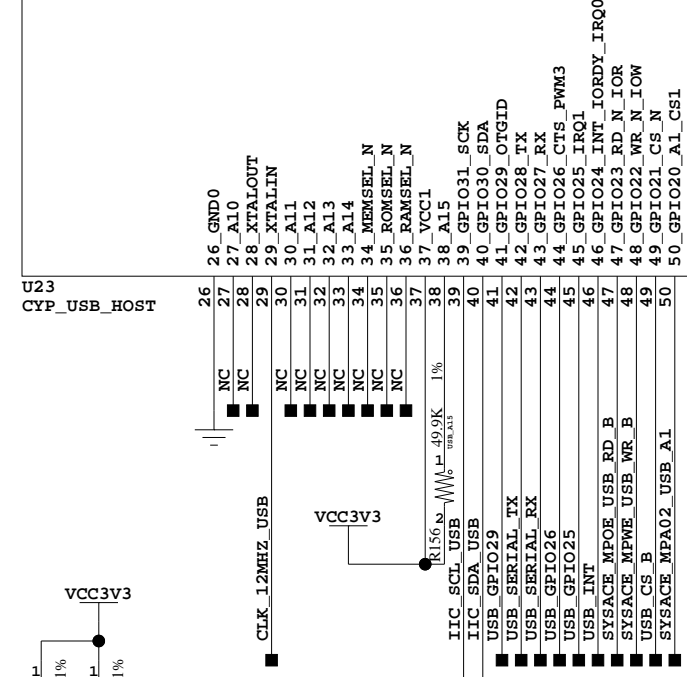
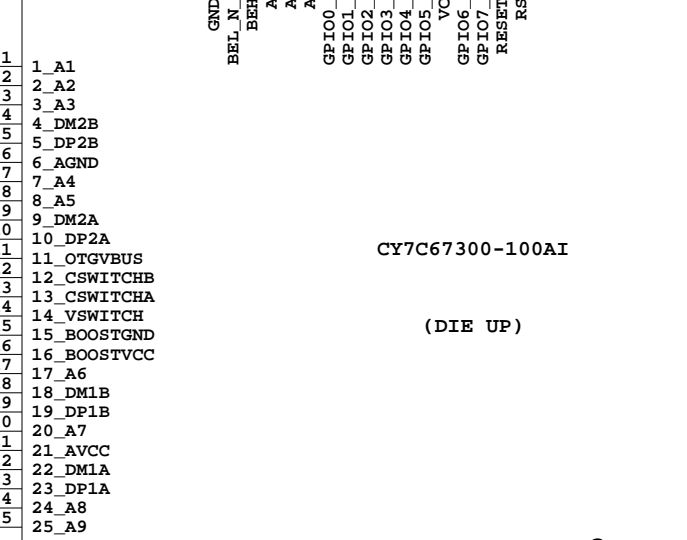
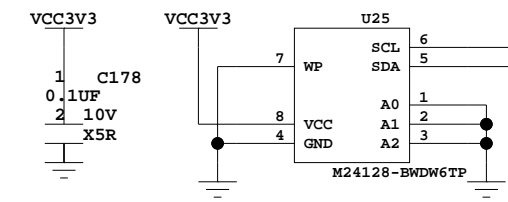
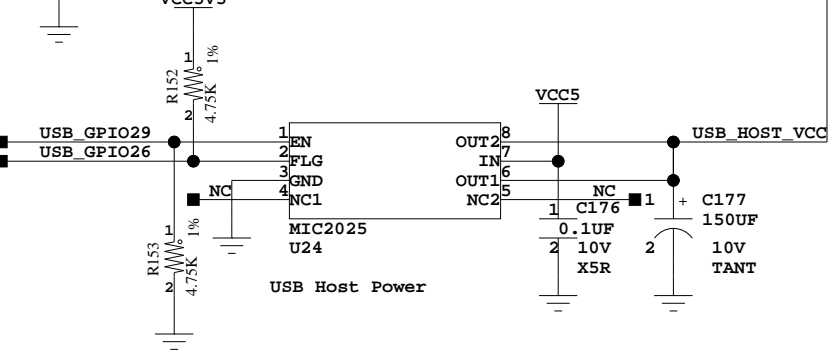
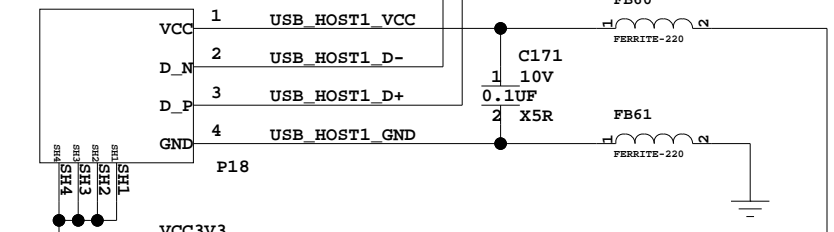
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Silkscreen:  
"USB Peripheral 1"  
USB\_B\_PERI\_SMT



Silkscreen:  
"USB Host"



### USB Controller



Title: USB Controller  
SCHEM, ROHS COMPLIANT  
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
0381241

Date: 1-22-2008\_14:51 Ver: A

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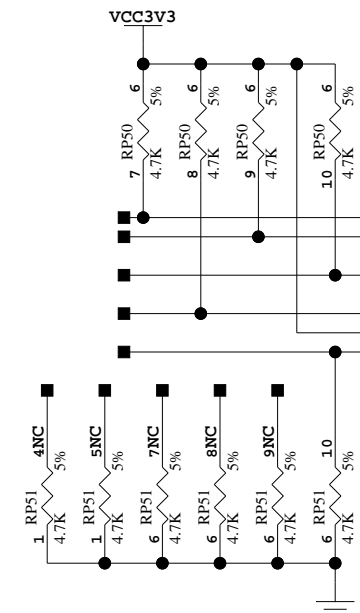
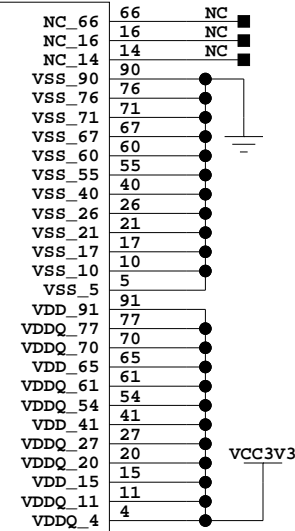
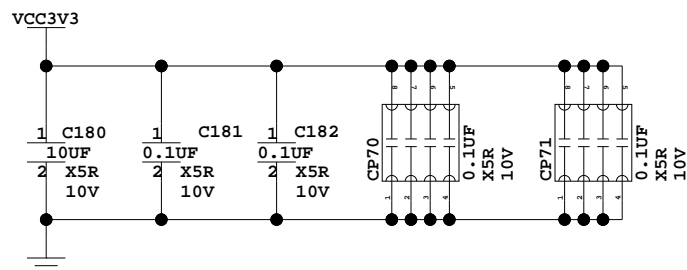
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The burst order mode of the SRAM is set to "Linear" by default

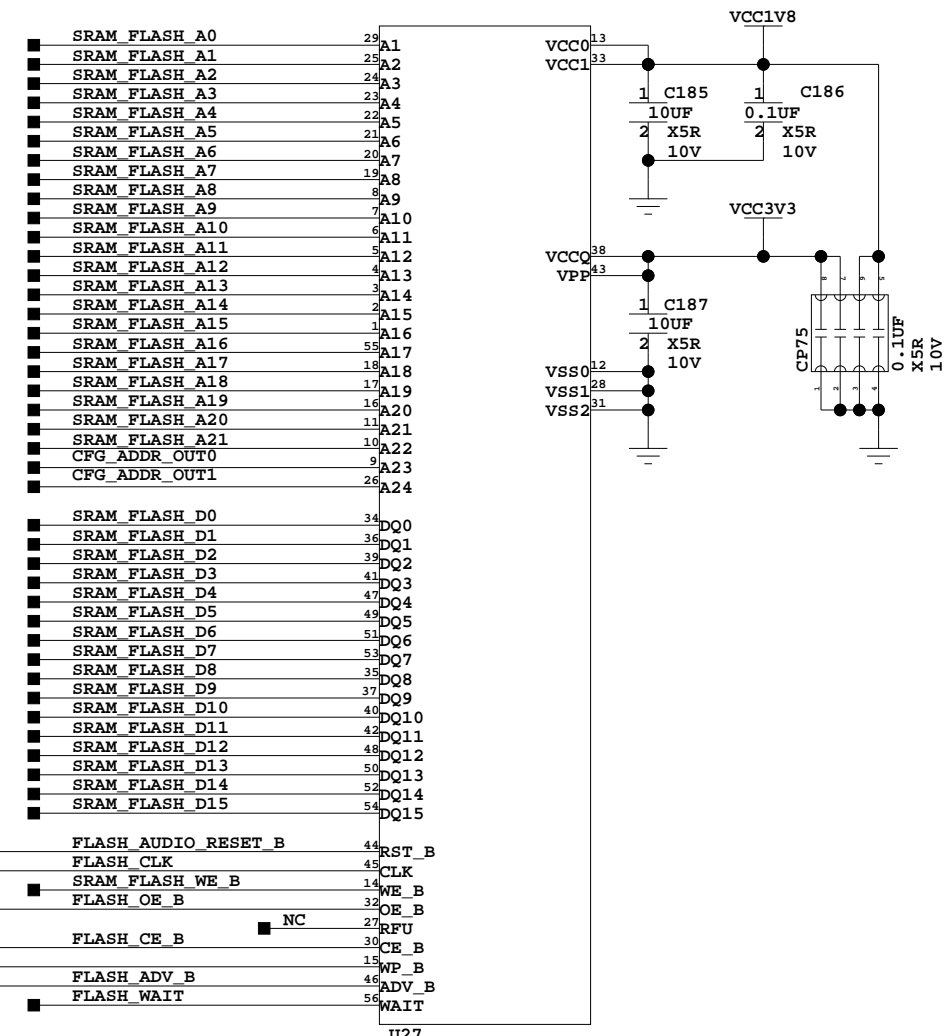
Silkscreen:  
"Synchronous SRAM"  
"9 MBit - 36 X 256K"



SRAM\_ZBT\_256KX36  
U26



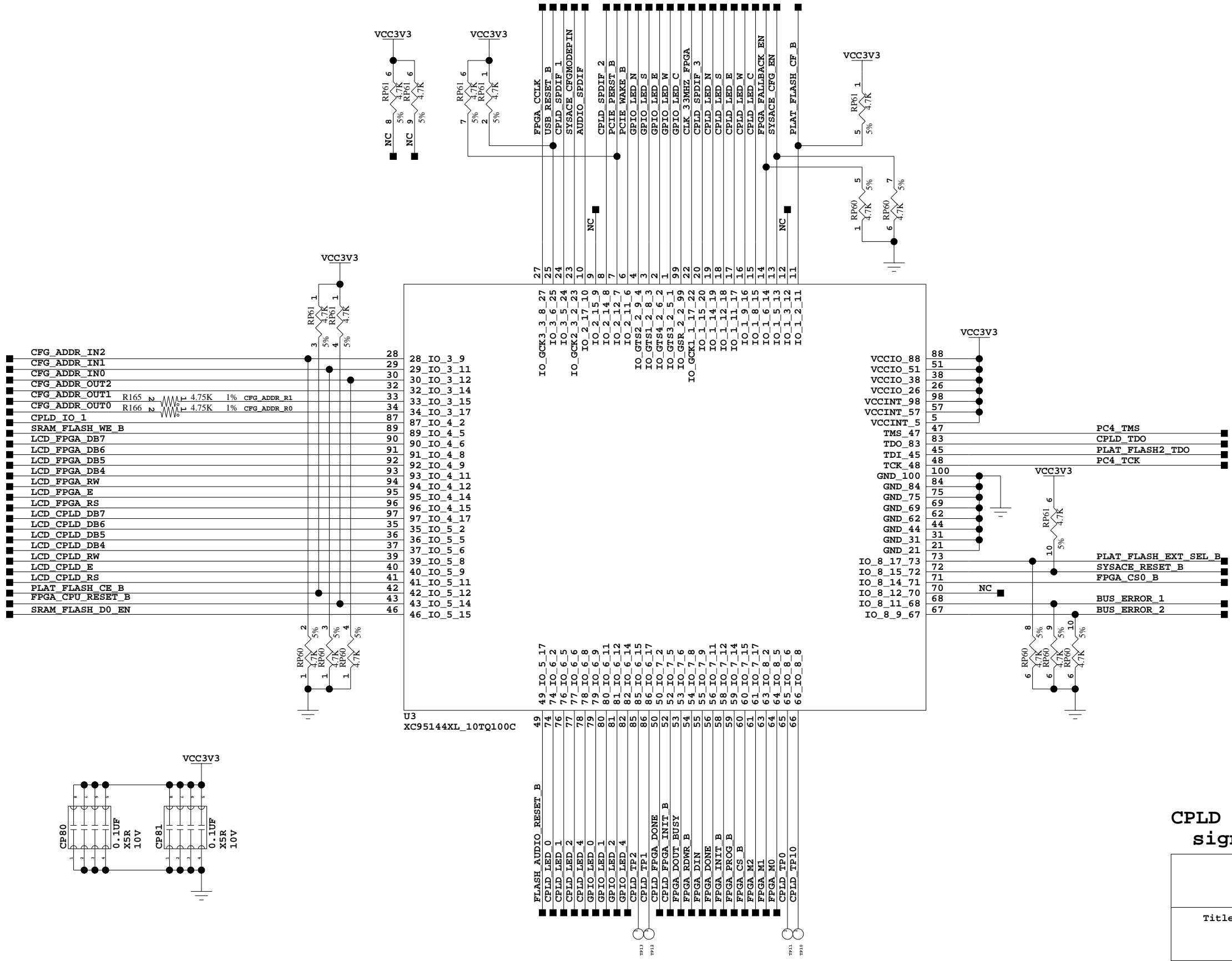
Silkscreen:  
"Strata FLASH"  
"256 MBit"



Memory:  
Synchronous SRAM,  
Strata FLASH



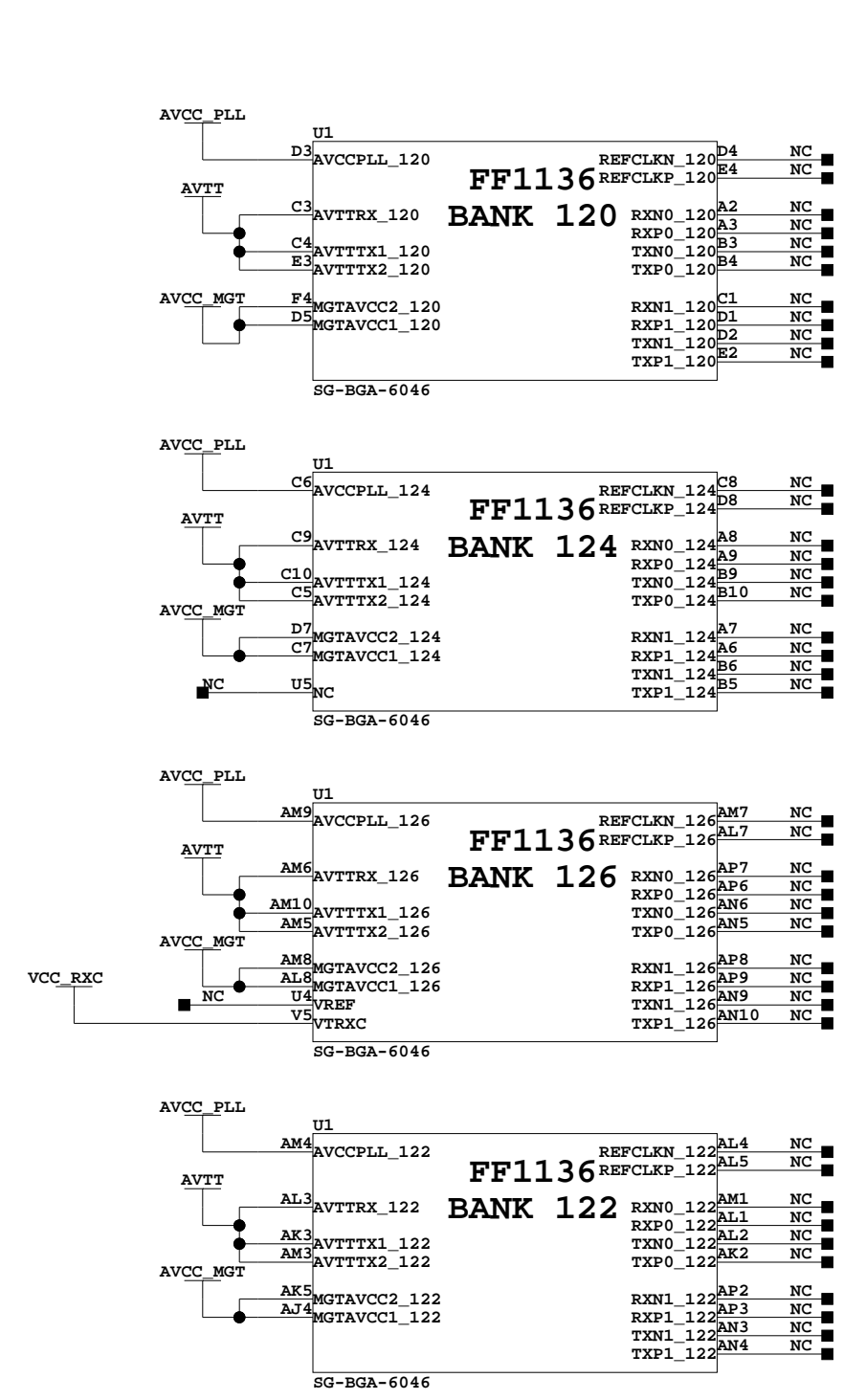
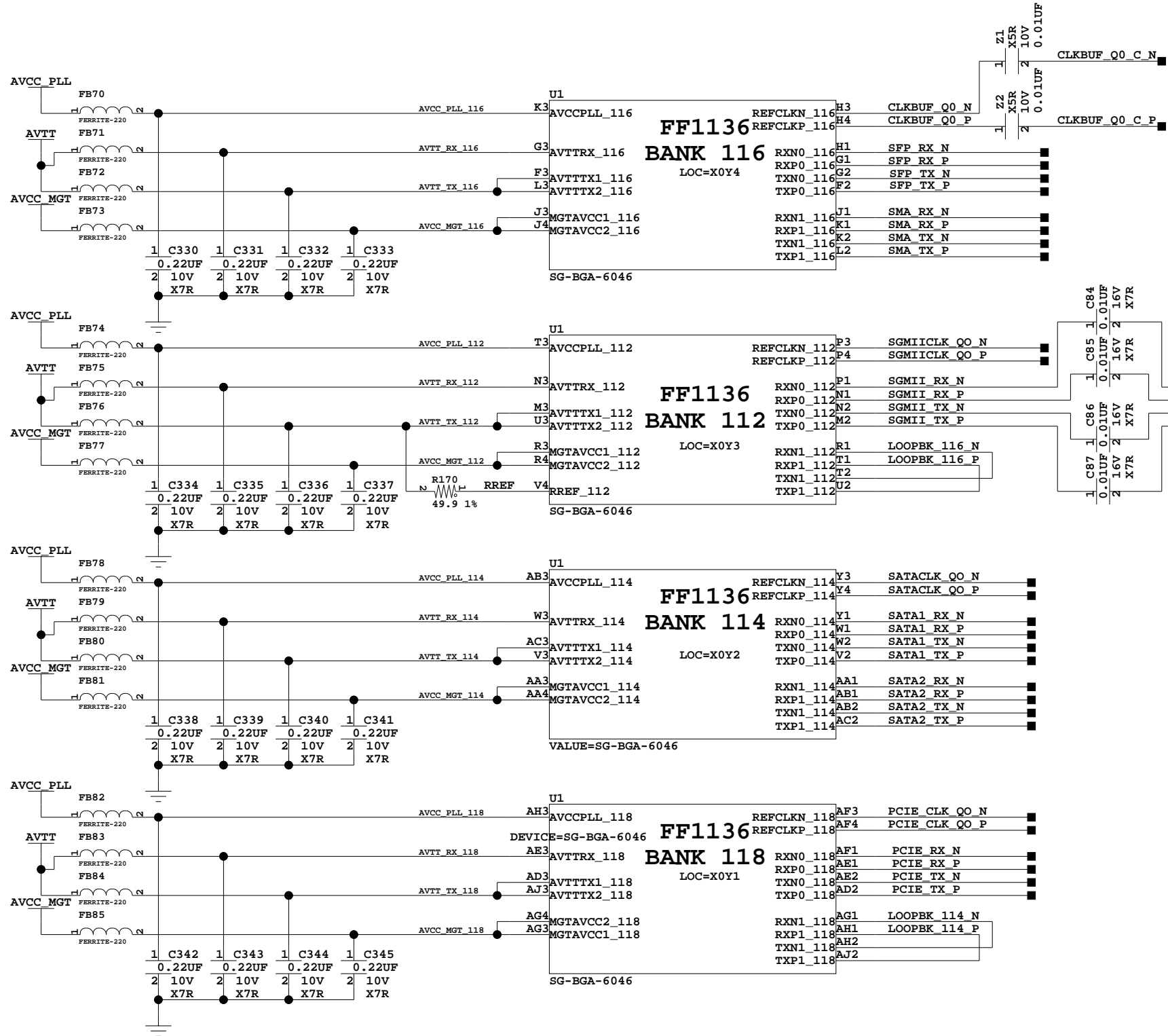
Title: Sync. SRAM, FLASH SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
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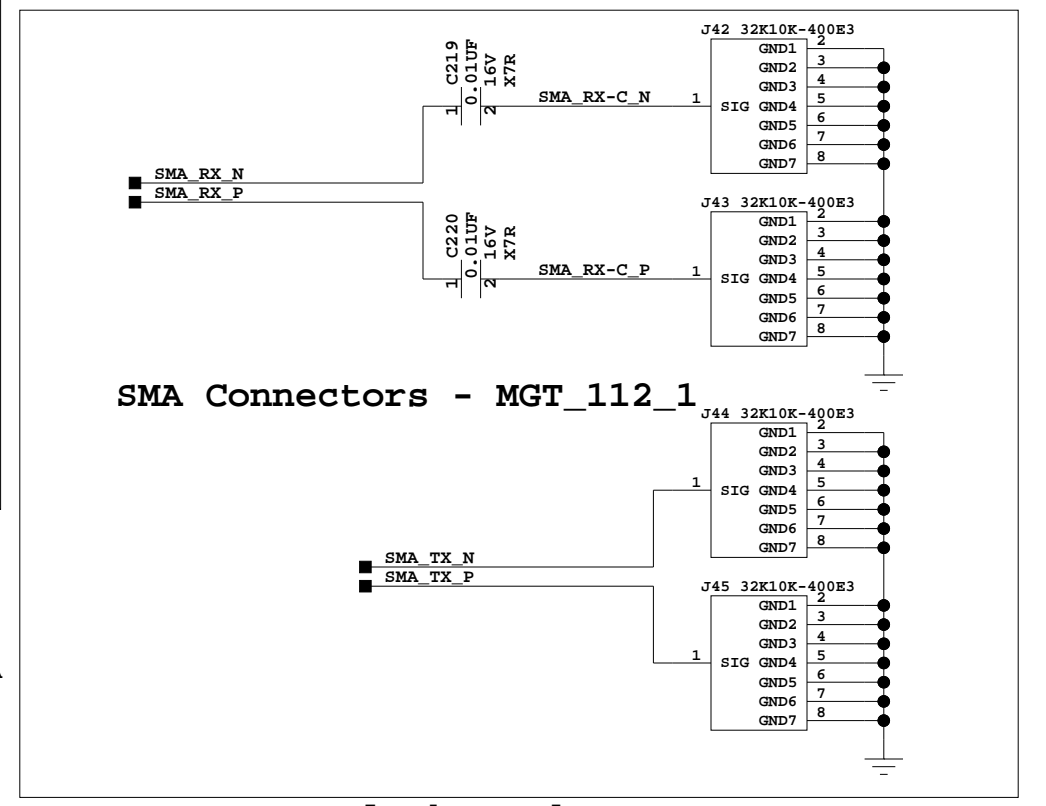
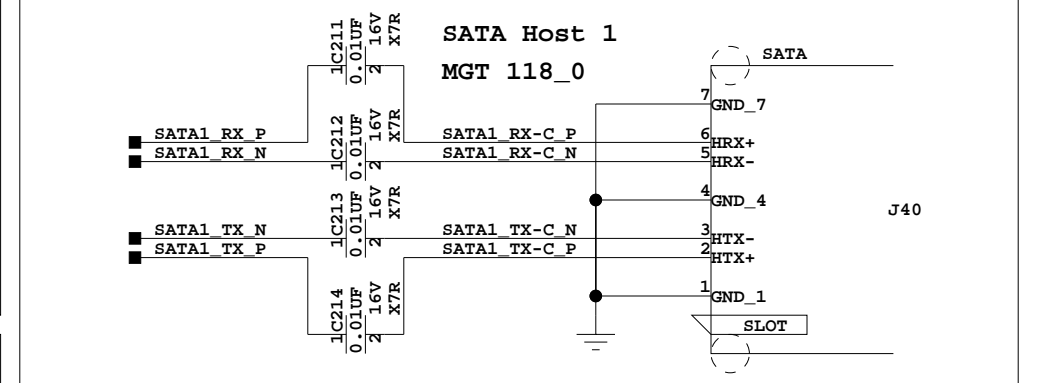
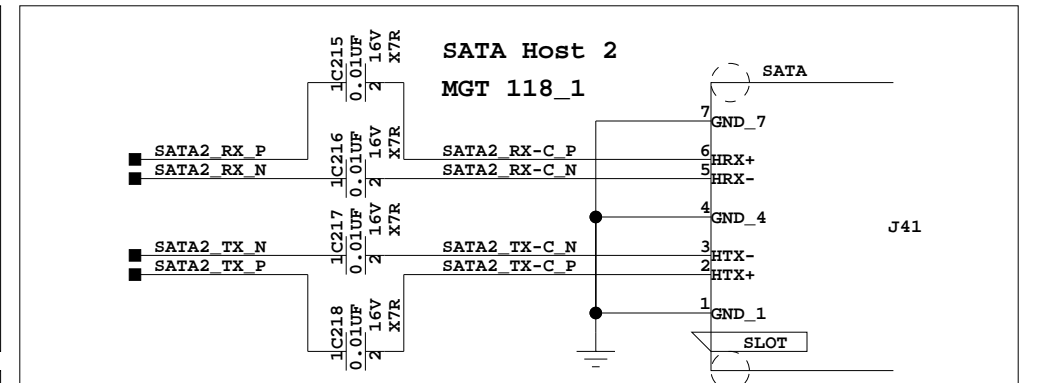
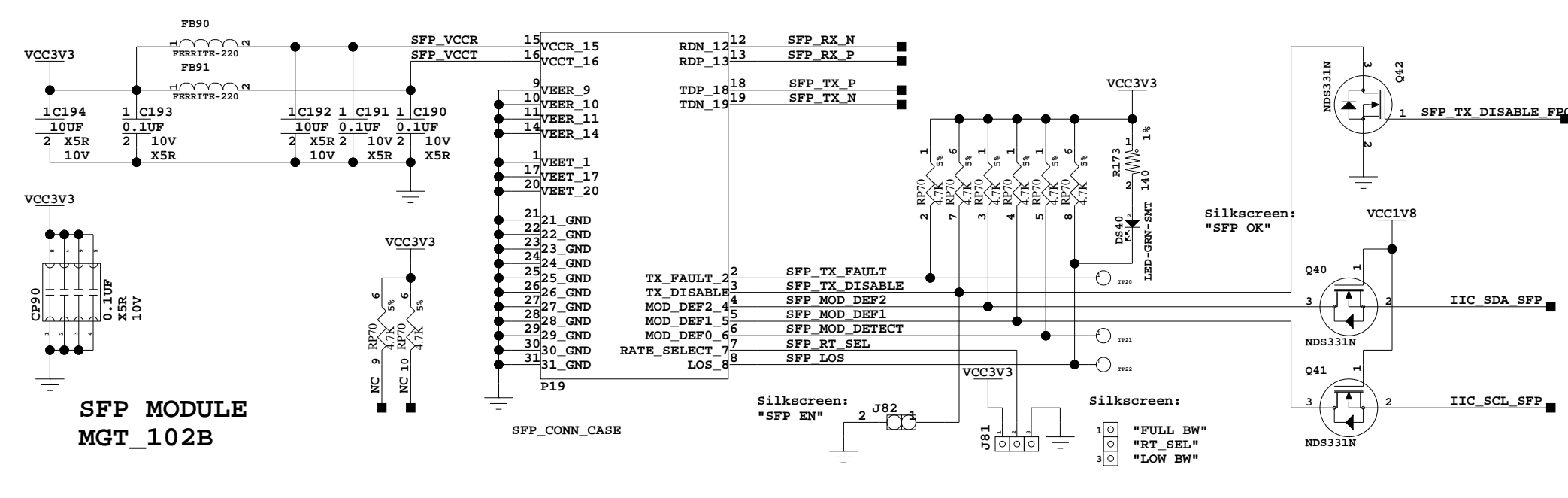
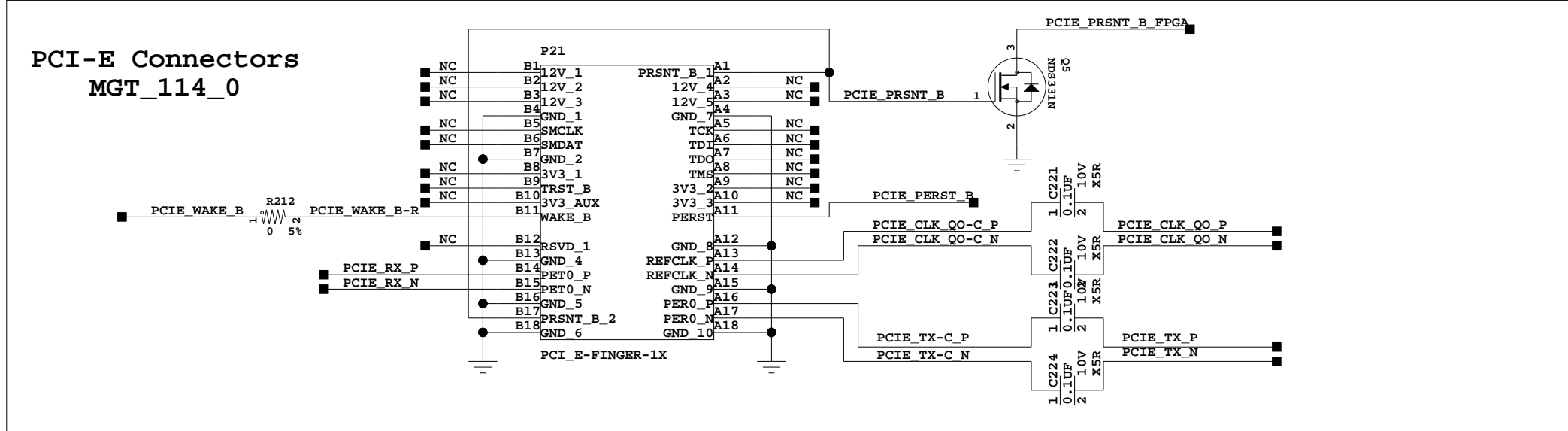
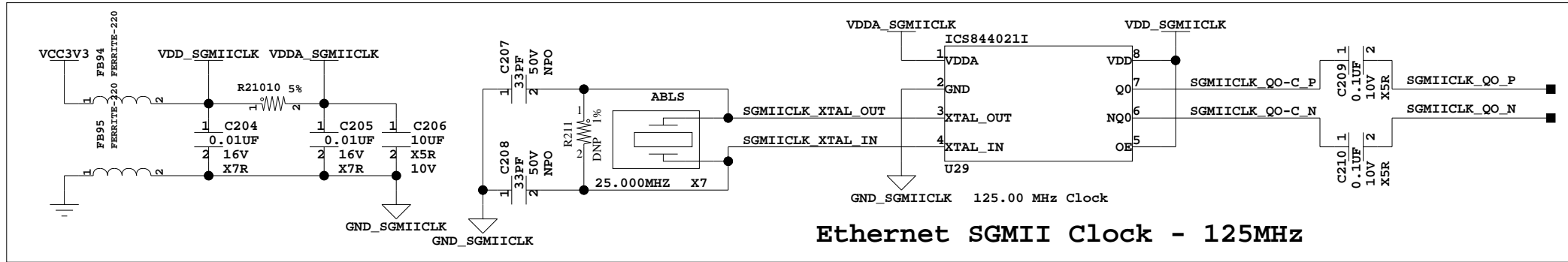
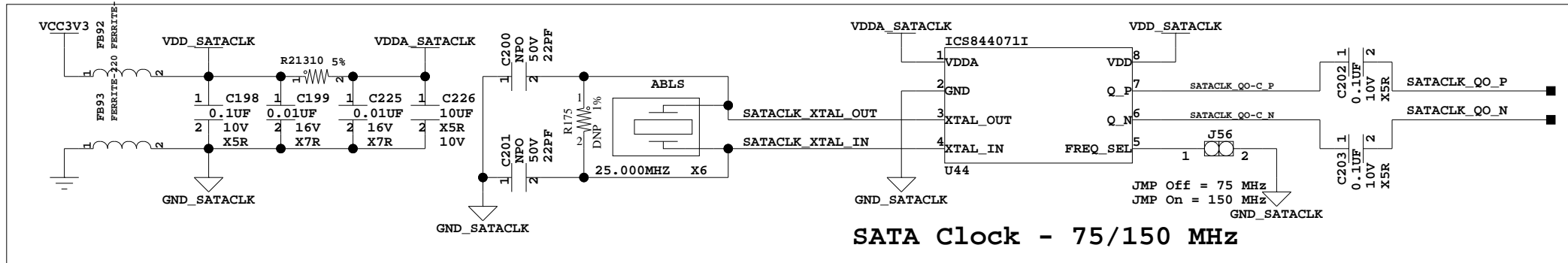
CPLD - Misc  
signal control



Title: CPLD - Misc signal control SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
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Title: MGT Banks SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
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**MGT Clocks and Connectors**



Title: MGT Connectors SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
Date: 1-22-2008_14:51	Ver: A
Sheet Size: B	Rev: 02
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### MGT PLL Regulator

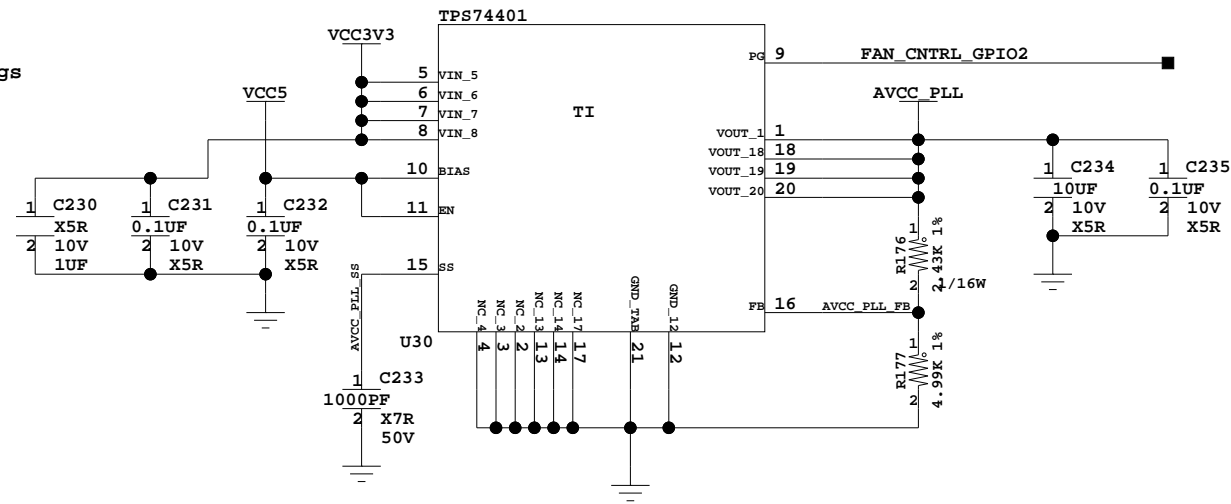
#### Voltage Output Settings

LXT & SXT (ML505/6)  
AVCC\_PLL = 1.2V @ 3A

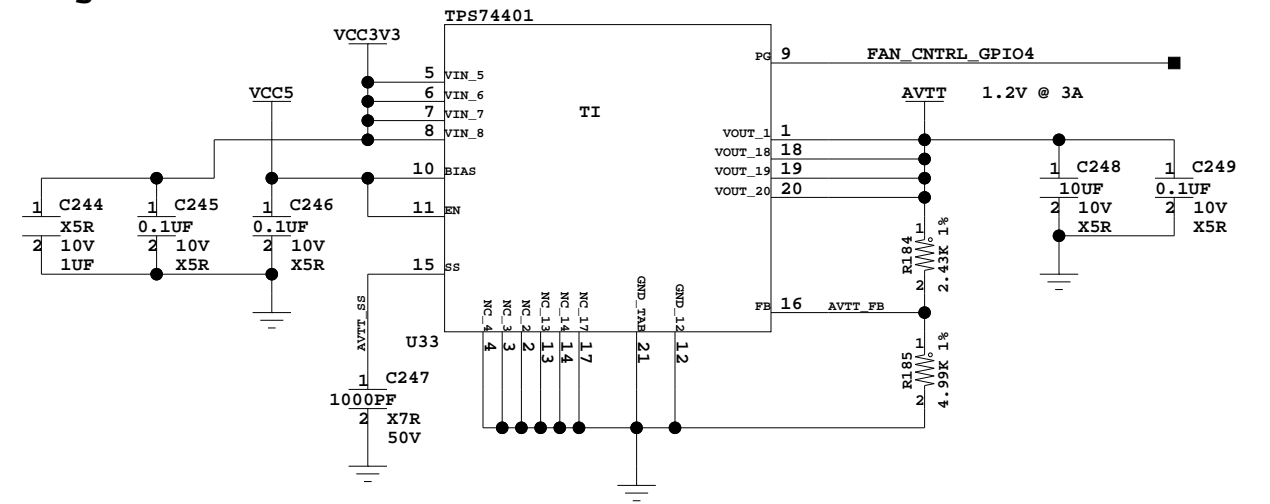
R176 = 2.43K 1%  
R177 = 4.99K 1%

FXT Only (ML507)  
AVCC\_PLL = 1.0V @ 3A

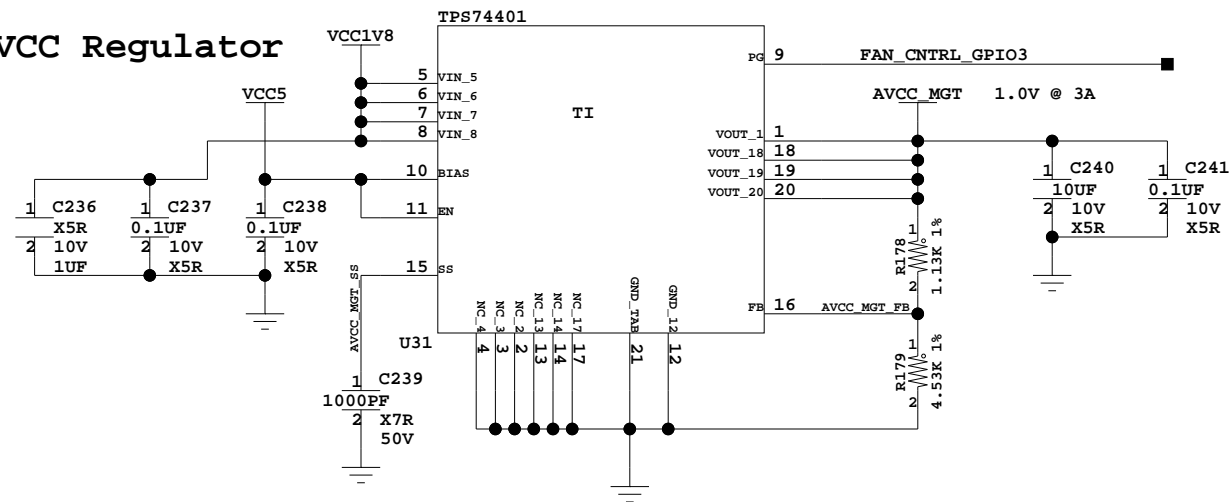
R176 = 1.13K 1%  
R177 = 4.53K 1%



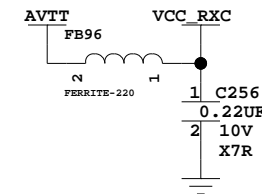
### MGT VTT Regulator



### MGT AVCC Regulator



### MGT RXC Regulator



### MGT Power Supplies

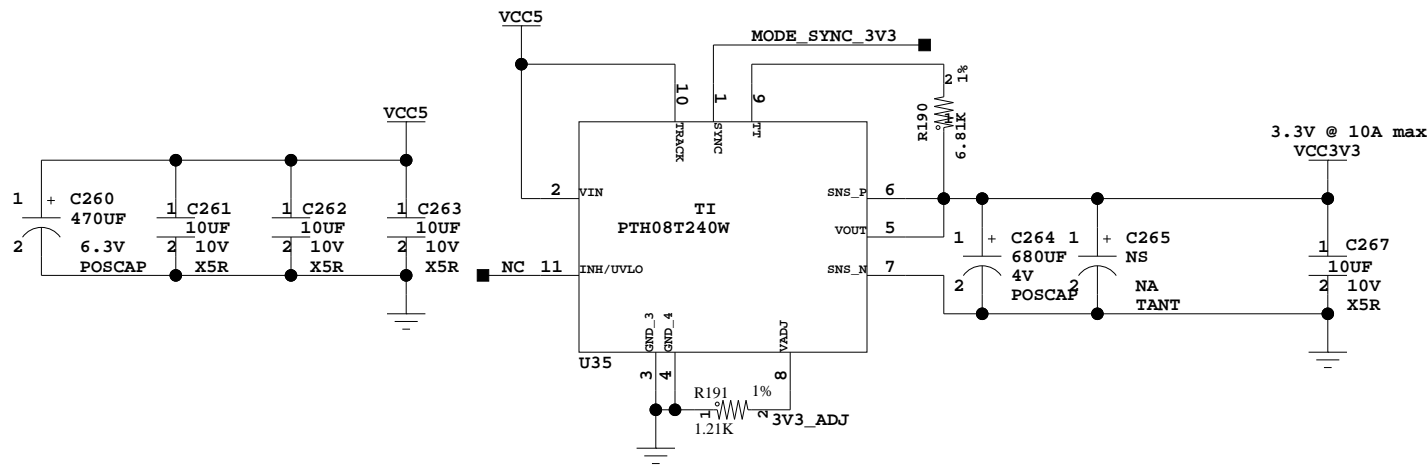


Title: MGT Power Supplies  
SCHEM, ROHS COMPLIANT  
ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415  
0381241

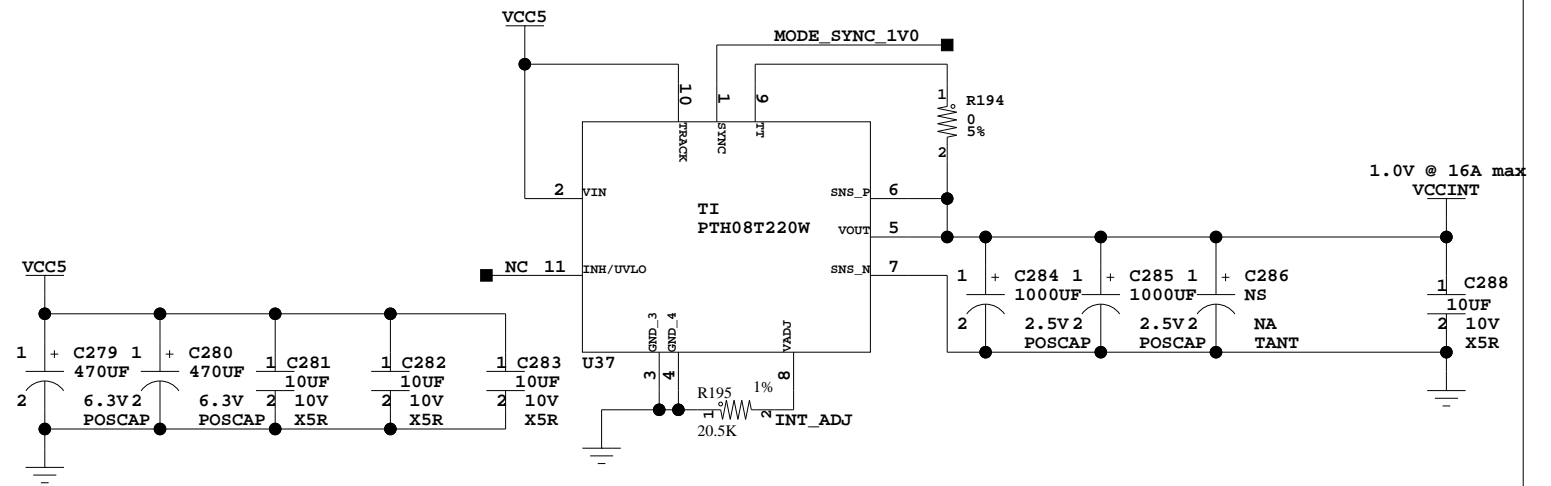
Date:	1-22-2008_14:51	Ver:	A
Sheet Size:	B	Rev:	02
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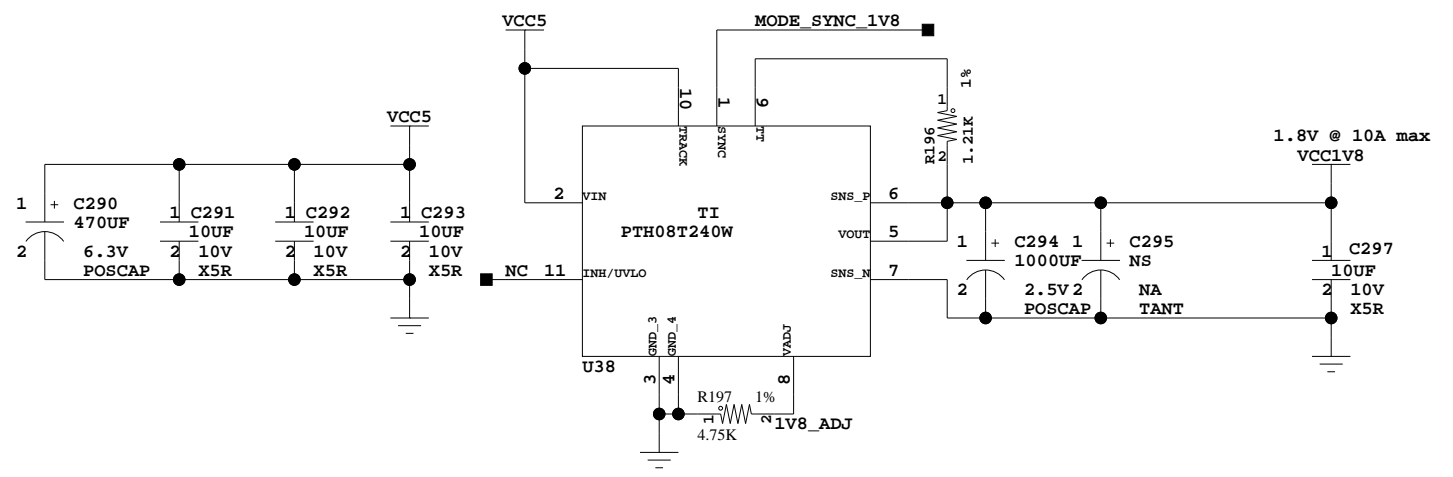
### 5v to 3.3V Regulator



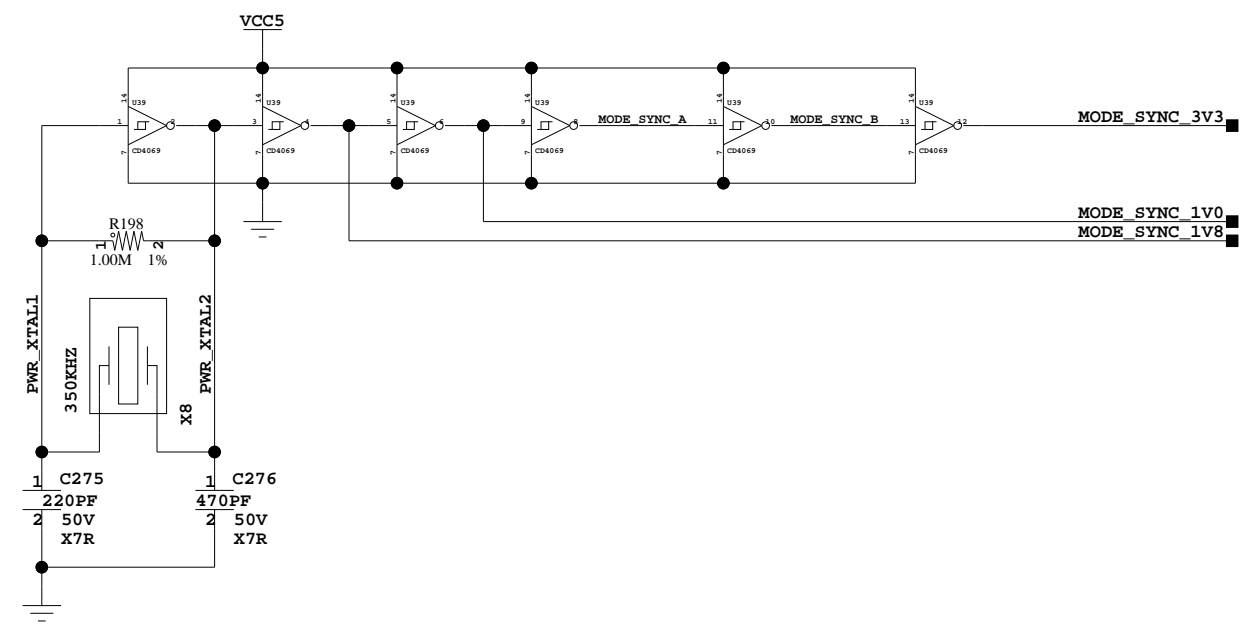
### 5v to 1.0V Regulator



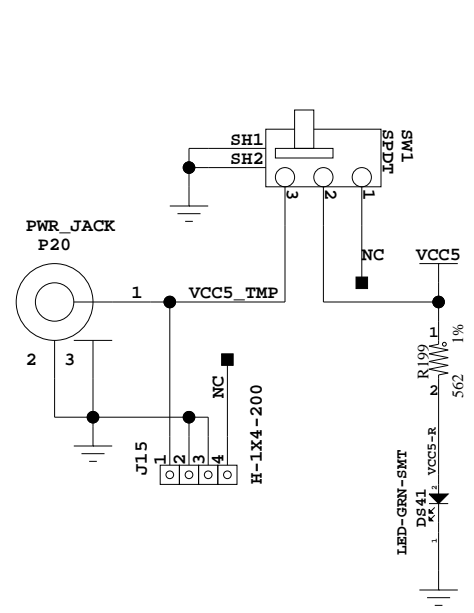
### 5v to 1.8V Regulator



### 5V Power Synchronizing Circuit



### 5V Power - Jack, Switch and LED

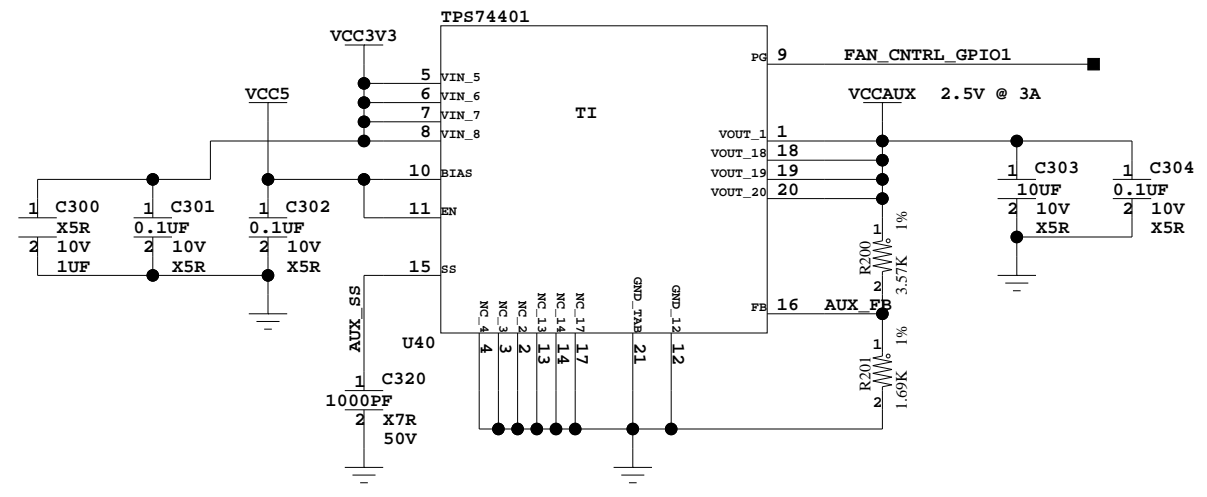


### 5V Power Supplies

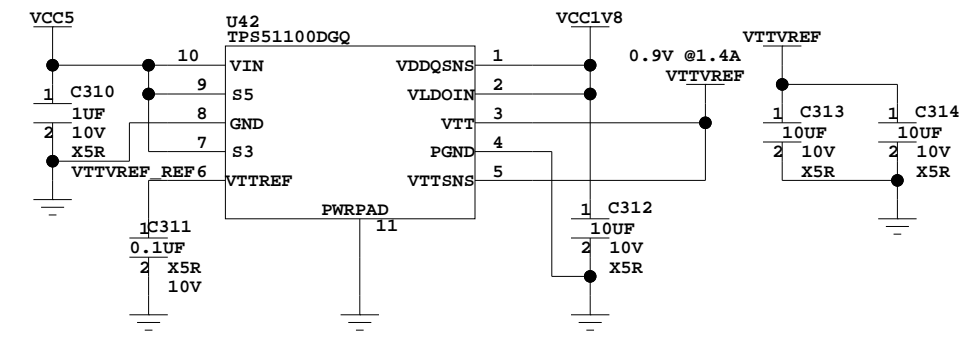


Title: Power Supplies SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
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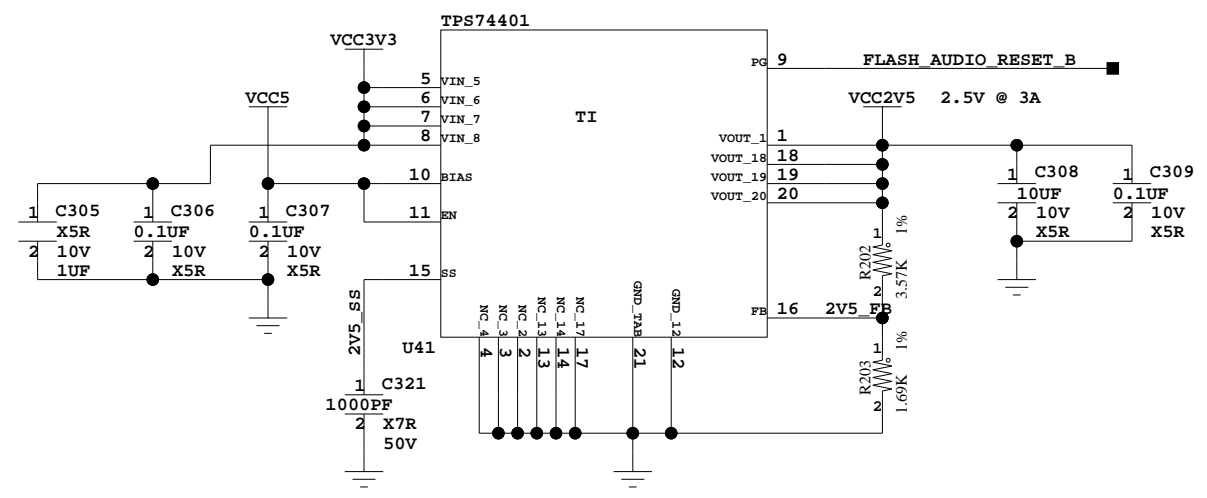
### 3.3v to 2.5V (VCC AUX) Regulator



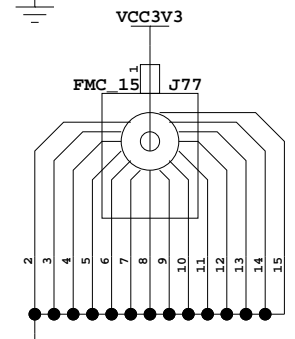
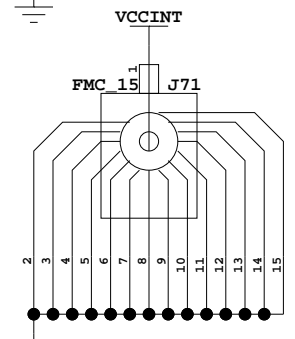
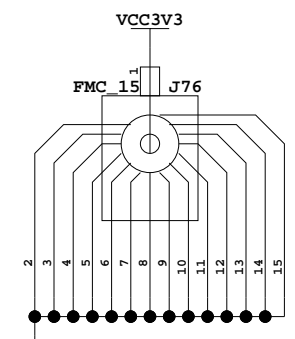
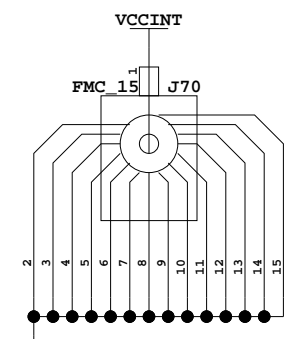
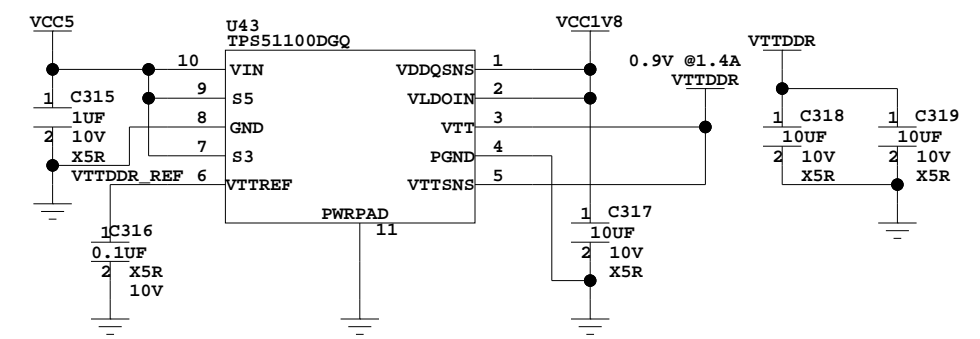
### 5V to 0.9V (DDR VTT VREF) Regulator



### 3.3v to 2.5V Regulator



### 5V to 0.9V (DDR2 VTT DDR) Regulator

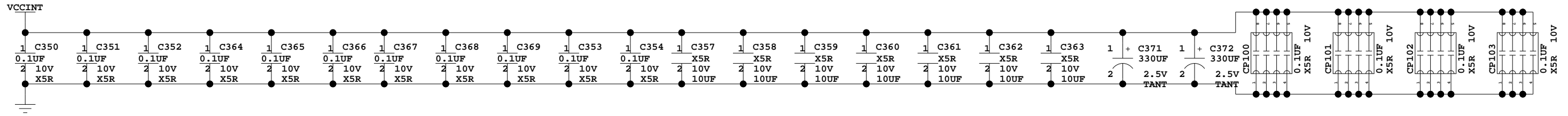


### 5V and 3.3V Power Supplies

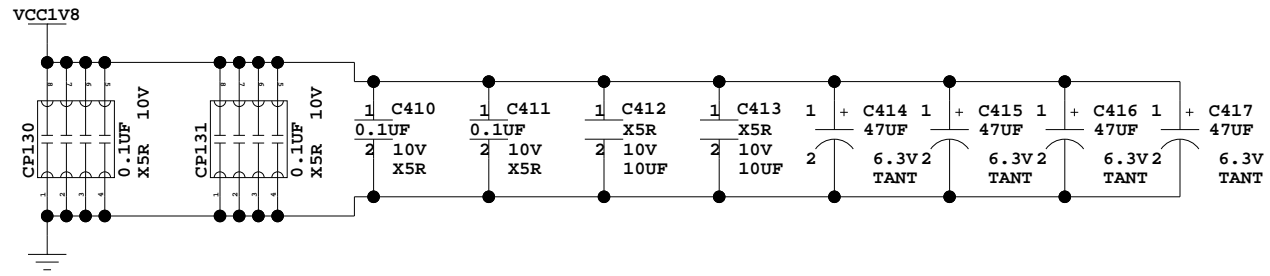
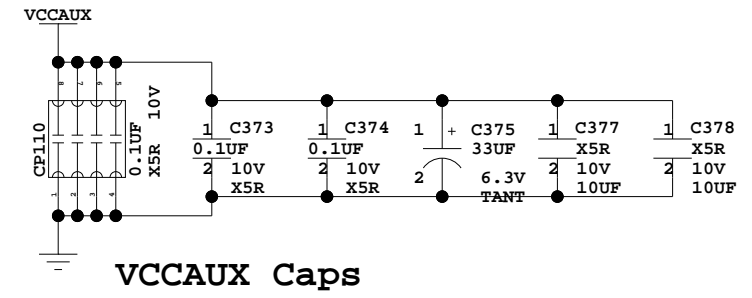
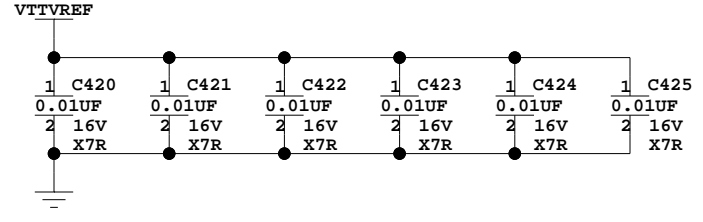
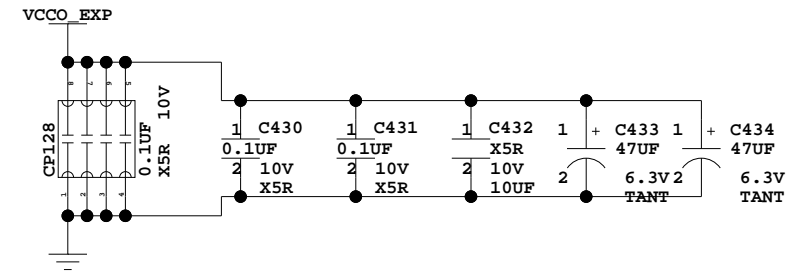
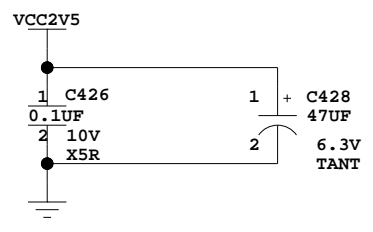
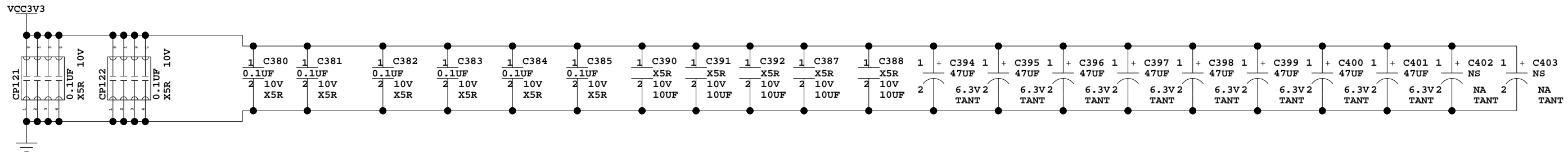


Title: Power Supplies SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
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## VCCINT Caps



## VCCO Caps



Title: FPGA Decoupling SCHEM, ROHS COMPLIANT ML505/6/7 VIRTEX-5 EVALUATION PLATFORM, 1280415 0381241	
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