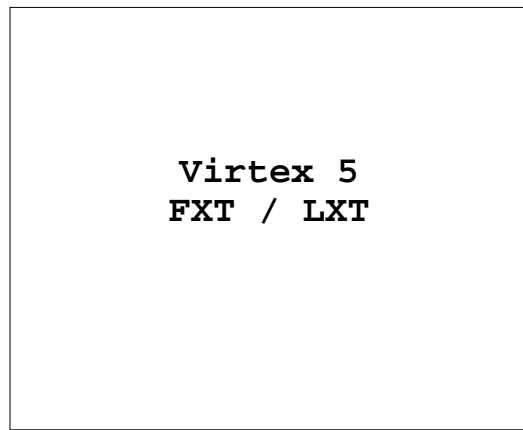


**Dual PCI Express Slots** **Dual 64 Bit DDR2 DIMMS** **Personality Modules**

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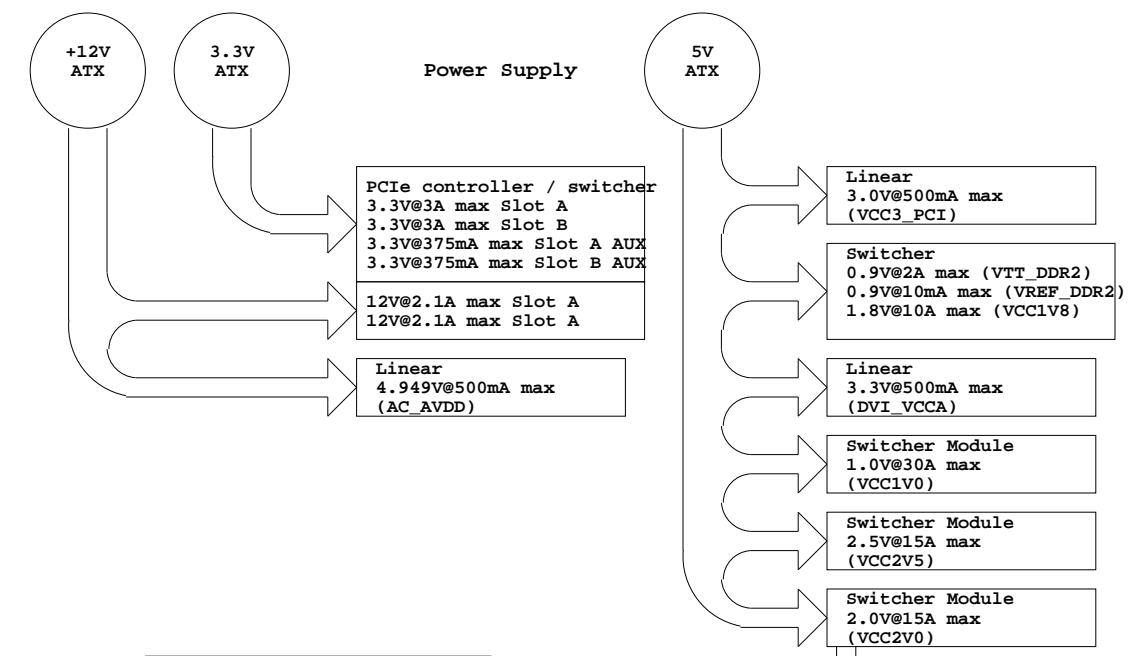
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USER Clock  
SMA Clock IN/OUT  
GTP CLK SMA INPUT  
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- MII/RGMII/SGMII  
10/100/1000 PHY  
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- SGMII  
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- 2 line  
Character LCD  
Header  
Page 62  
J13



**IIC Device Addresses**

DEVICE	REFDES	ADDR
LM87C1MT	u20	0x5C
RTC-8564JE	u22	0xA2
24LC64-I/SN	u21	0xA0
87705-1001	p9	0xA6
87705-1001	p48	0xA8
MIC2592B-2BTQ	U55	0x8E

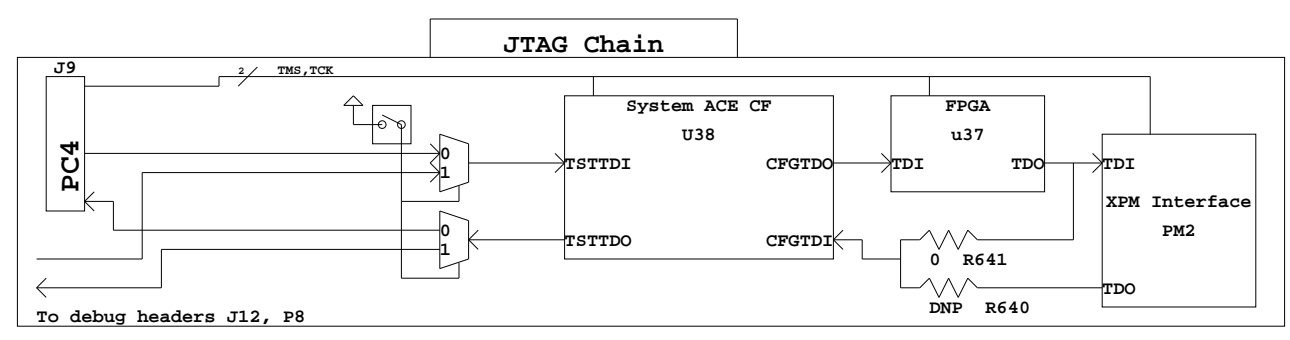
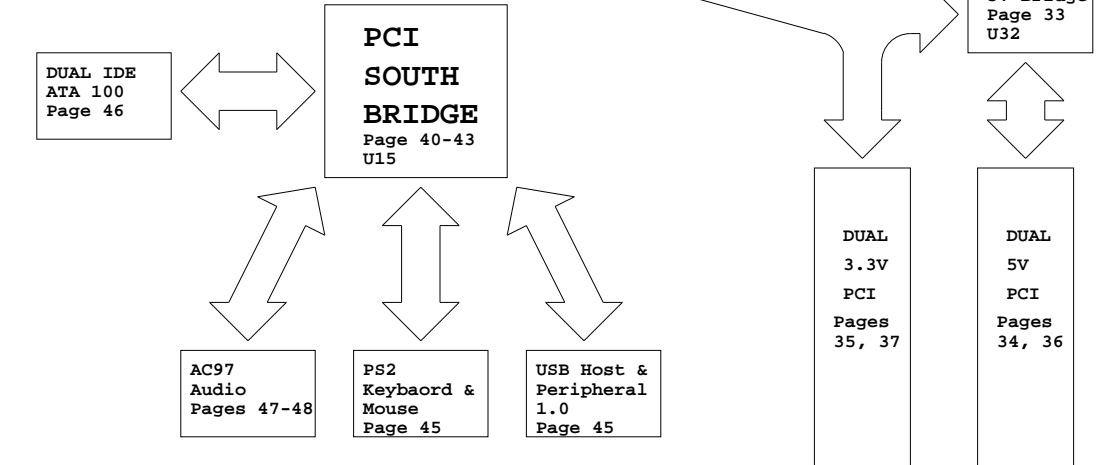
**XILINX PART NUMBERS**

SCHEMATICS	0381255
PCB ARTWORK	0532059
PCB FABRICATION	1280432

NOTE: PLEASE REVIEW THE ML510 BOM FOR ITEMS DESIGNATED AS "DNP".

DNP ITEMS ARE NOT POPULATED ON THE PCB.

THE ML510 BOM CONTAINS THE MOST ACCURATE INFORMATION ABOUT DNP DISCRETES AND COMPONENTS



**XILINX**

SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432


Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOrm  
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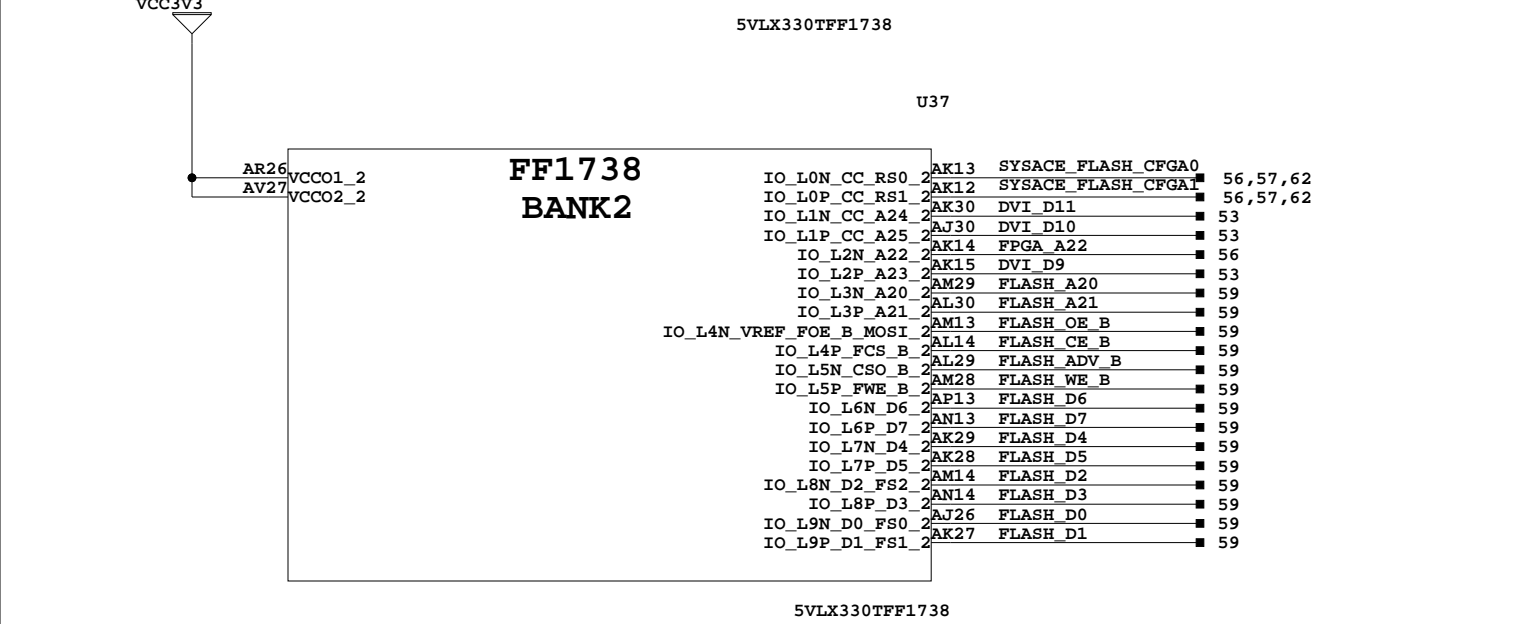
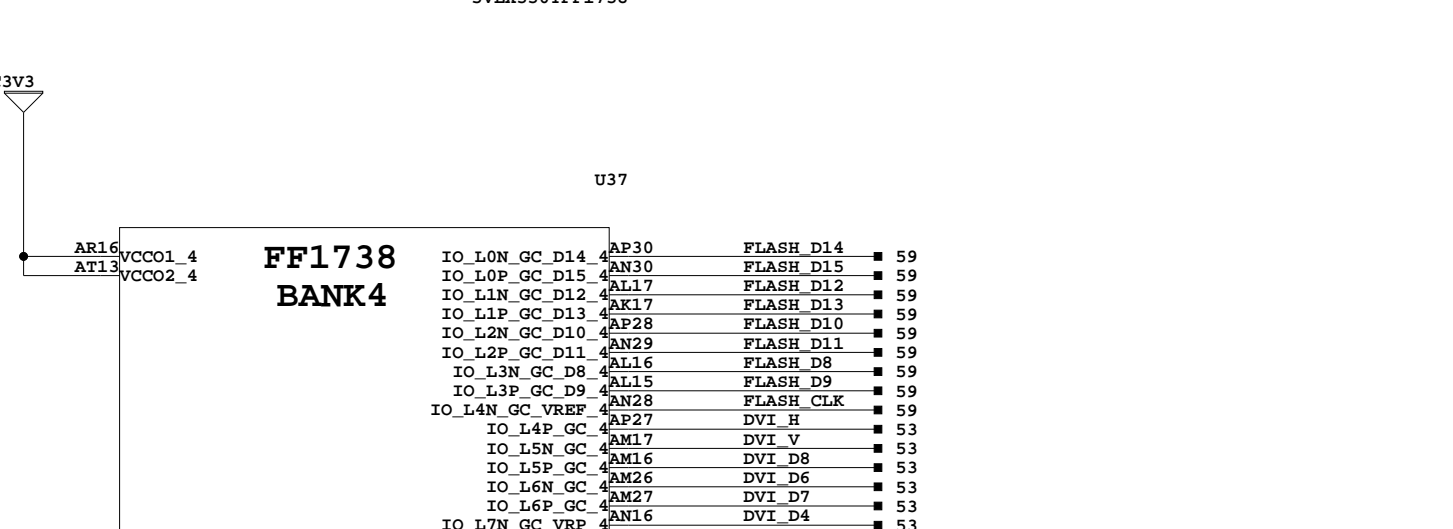
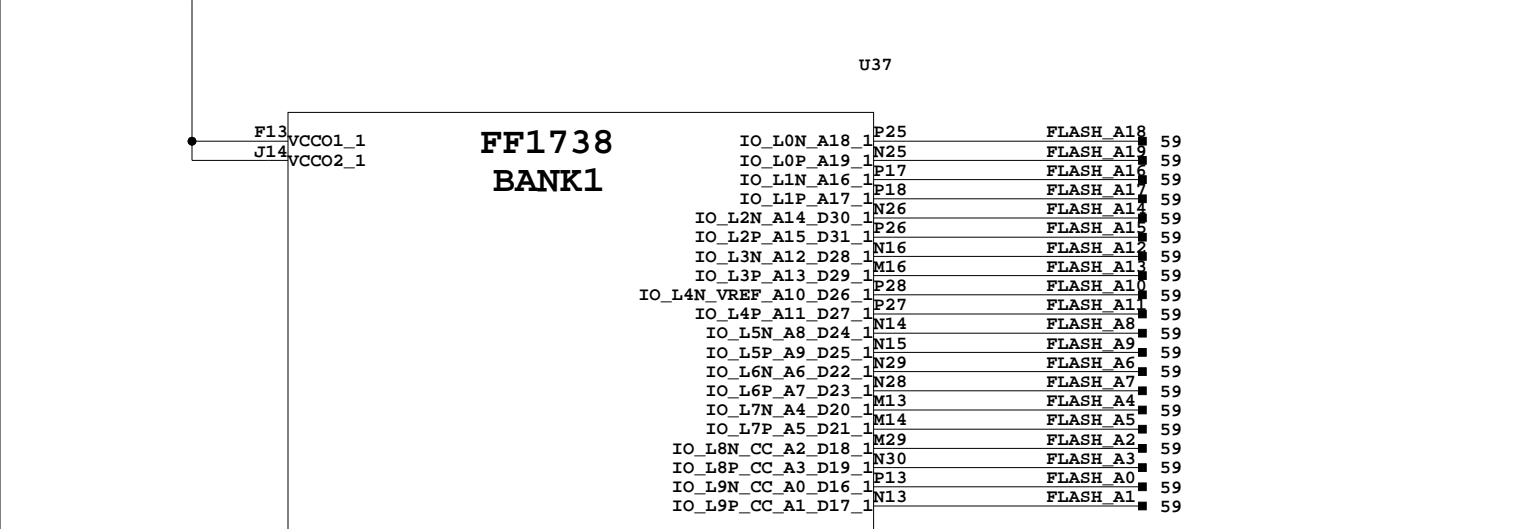
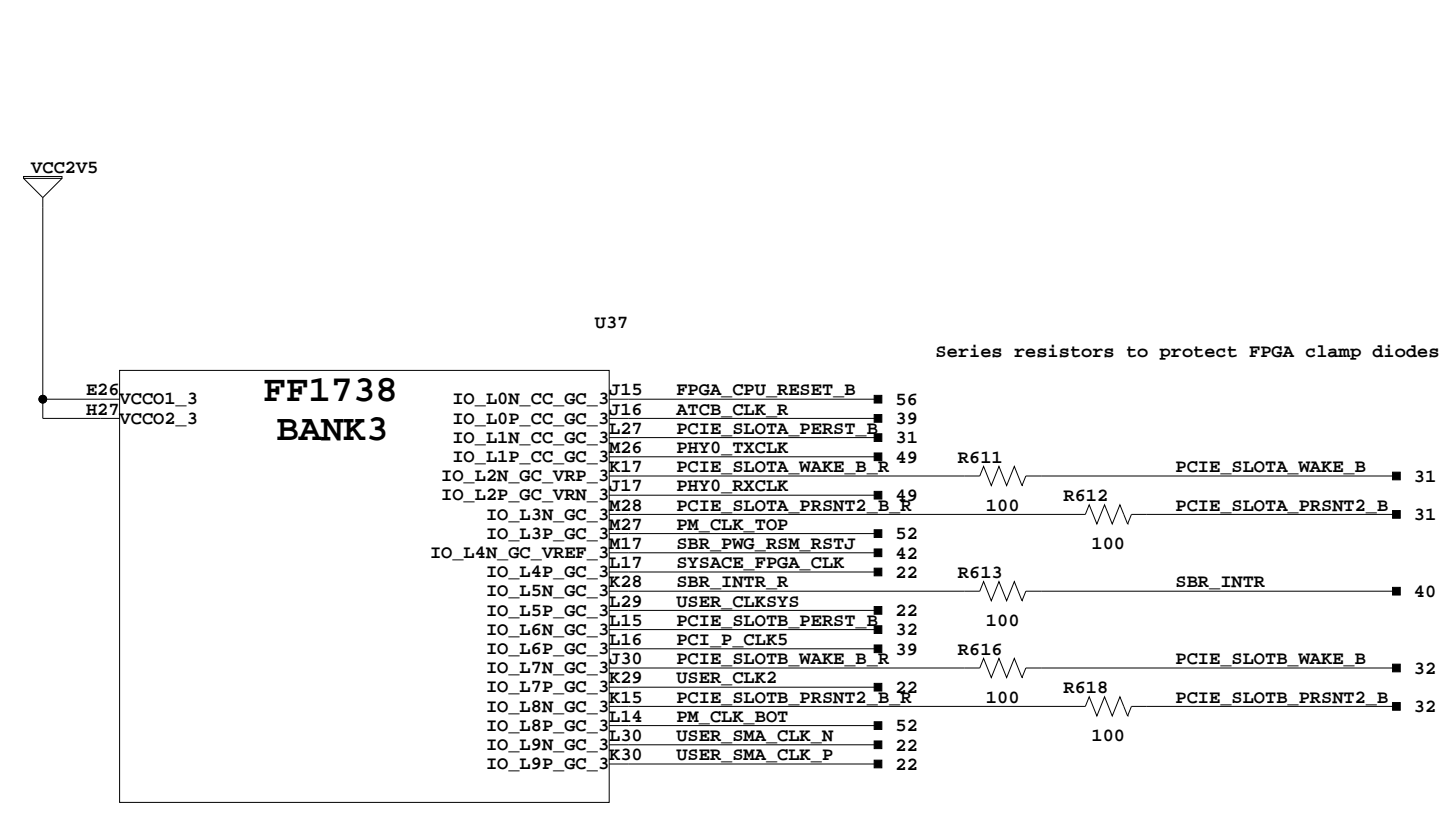
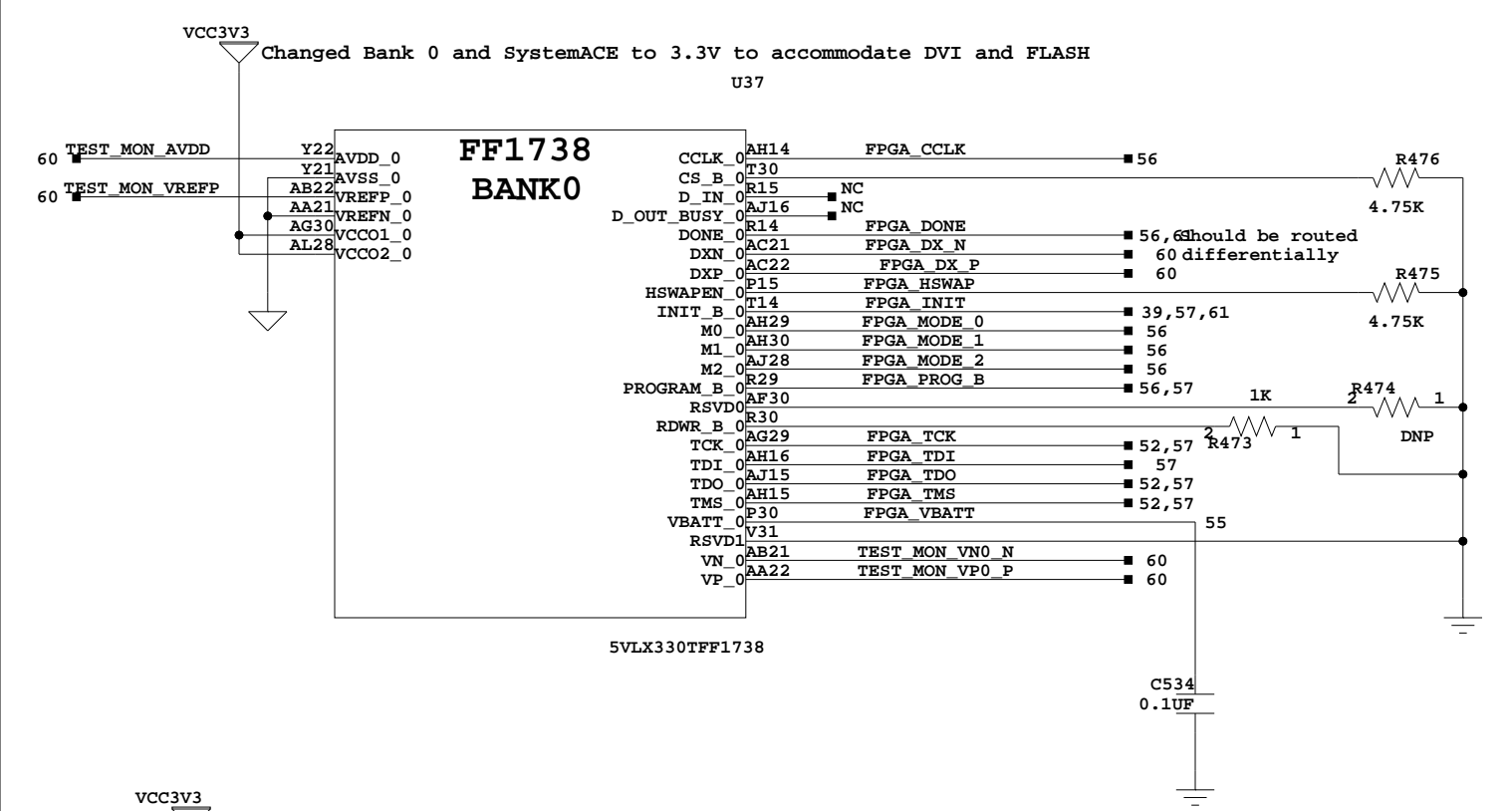
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9	FPGA - BANK 21,23
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		ART P/N	0532059
		FAB P/N	1280432
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FPGA - BANK 0, 1, 2, 3, 4

SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOM

FPGA - BANK 0, 1, 2, 3, 4 - CONFIG, MISC, FLASH, CLOCKS, DVI

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VCC2V5

U37

B25 VCCO1\_5  
C22 VCCO2\_5  
F23 VCCO3\_5

**FF1738**  
**BANK5**

IO_L0N_5	M24	PM_IO_1_N	52
IO_L0P_5	L24	PM_IO_0_P	52
IO_L10N_CC_5	K19	PM_IO_21_N	52
IO_L10P_CC_5	K18	PM_IO_20_P	52
IO_L11N_CC_5	L26	PM_IO_23_N	52
IO_L11P_CC_5	K27	PM_IO_22_P	52
IO_L12N_VRN_5	P20	VRP_BANK5	52
IO_L12P_VRN_5	N20	VRN_BANK5	52
IO_L13N_5	F27	PM_IO_25_N	52
IO_L13P_5	G27	PM_IO_24_P	52
IO_L14N_VREF_5	N19	PM_IO_27_N	52
IO_L14P_5	M19	PM_IO_26_P	52
IO_L15N_5	H28	PM_IO_29_N	52
IO_L15P_5	G28	PM_IO_28_P	52
IO_L16N_5	N18	PM_IO_31_N	52
IO_L16P_5	M18	PM_IO_30_P	52
IO_L17N_5	F29	PM_IO_33_N	52
IO_L17P_5	G29	PM_IO_32_P	52
IO_L18N_5	L19	PM_IO_35_N	52
IO_L18P_5	L20	PM_IO_34_P	52
IO_L19N_5	H30	PM_IO_37_N	52
IO_L19P_5	H29	PM_IO_36_P	52
IO_L1N_5	E17	PM_IO_3_N	52
IO_L1P_5	E18	PM_IO_2_P	52
IO_L2N_5	L25	PM_IO_5_N	52
IO_L2P_5	K24	PM_IO_4_P	52
IO_L3N_5	F17	PM_IO_7_N	52
IO_L3P_5	F16	PM_IO_6_P	52
IO_L4N_VREF_5	J25	PM_IO_9_N	52
IO_L4P_5	K25	PM_IO_8_P	52
IO_L5N_5	H16	PM_IO_11_N	52
IO_L5P_5	G16	PM_IO_10_P	52
IO_L6N_5	J26	PM_IO_13_N	52
IO_L6P_5	H26	PM_IO_12_P	52
IO_L7N_5	G17	PM_IO_15_N	52
IO_L7P_5	G18	PM_IO_14_P	52
IO_L8N_CC_5	J27	PM_IO_17_N	52
IO_L8P_CC_5	J28	PM_IO_16_P	52
IO_L9N_CC_5	H18	PM_IO_19_N	52
IO_L9P_CC_5	J18	PM_IO_18_P	52

5VLX330TFF1738

49.9

49.9

VCC2V5

VCC2V5

U37

AT23 VCCO1\_6  
AW24 VCCO2\_6  
AY21 VCCO3\_6

**FF1738**  
**BANK6**

IO_L0N_6	AR28	CPU_TDO_TMP	58
IO_L0P_6	AR29	CPU_HALT_B	58
IO_L10N_CC_6	AM18	TRC_BS1_BR1	58
IO_L10P_CC_6	AN18	TRC_BS2_BR2	58
IO_L11N_CC_6	AP26	ATD_0	58
IO_L11P_CC_6	AN26	TRC_BS0_BR0	58
IO_L12N_VRN_6	AP18	VRP_BANK6	58
IO_L12P_VRN_6	AR18	VRN_BANK6	58
IO_L13N_6	AP25	ATD_2	58
IO_L13P_6	AN25	ATD_1	58
IO_L14N_VREF_6	AR19	SBR_IDE_RST_B	46
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IO_L15N_6	AN24	IIC_THERM_B	42,55
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IO_L19P_6	AR14	CPU_TMS	50
IO_L1N_6	AT14	CPU_TCK	58
IO_L2N_6	AT30	CPU_TRST_B	58
IO_L2P_6	AR30	CPU_TDI	58
IO_L3N_6	AR15	TRC_ES4	58
IO_L3P_6	AT15	TRC_ES2	58
IO_L4N_VREF_6	AU29	SBR_NMI_R	58
IO_L4P_6	AT29	TRC_TS0	58
IO_L5N_6	AT16	TRC_TS2	58
IO_L5P_6	AT17	TRC_TS1	58
IO_L6N_6	AT27	TRC_TS4	58
IO_L6P_6	AU28	TRC_TS3	58
IO_L7N_6	AR17	TRC_TS6	58
IO_L7P_6	AP17	TRC_TS5	58
IO_L8N_CC_6	AR27	TRC_CLK_R	39
IO_L8P_CC_6	AT26	TRC_ES3	58
IO_L9N_CC_6	AN19	TRC_ES0	58
IO_L9P_CC_6	AN20	TRC_ES1	58

5VLX330TFF1738

49.9

49.9

VCC2V5

Series resistor to protect  
FPGA clamp diode

R619

100

SBR\_NMI 40

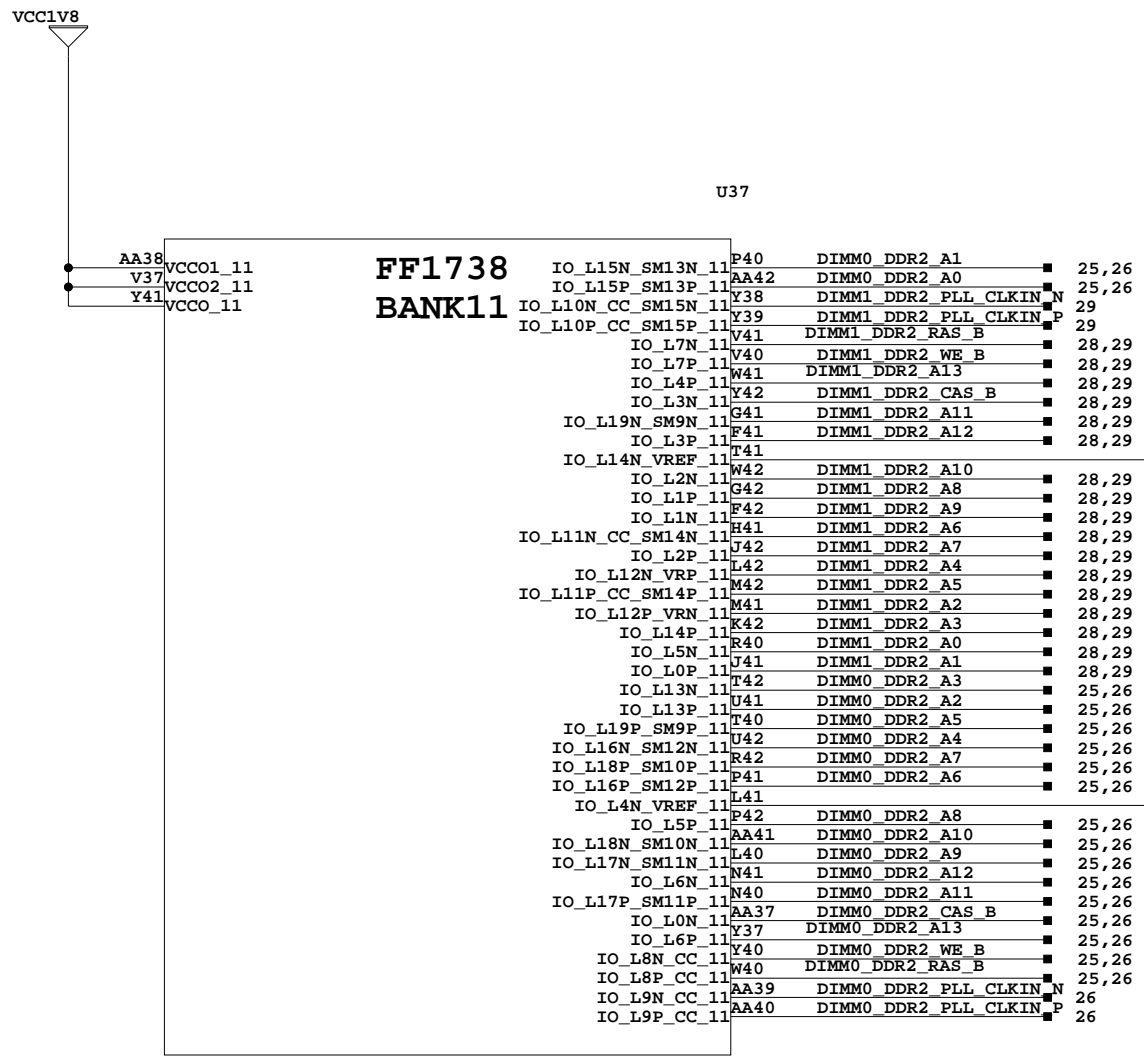
### FPGA - BANK 5,6



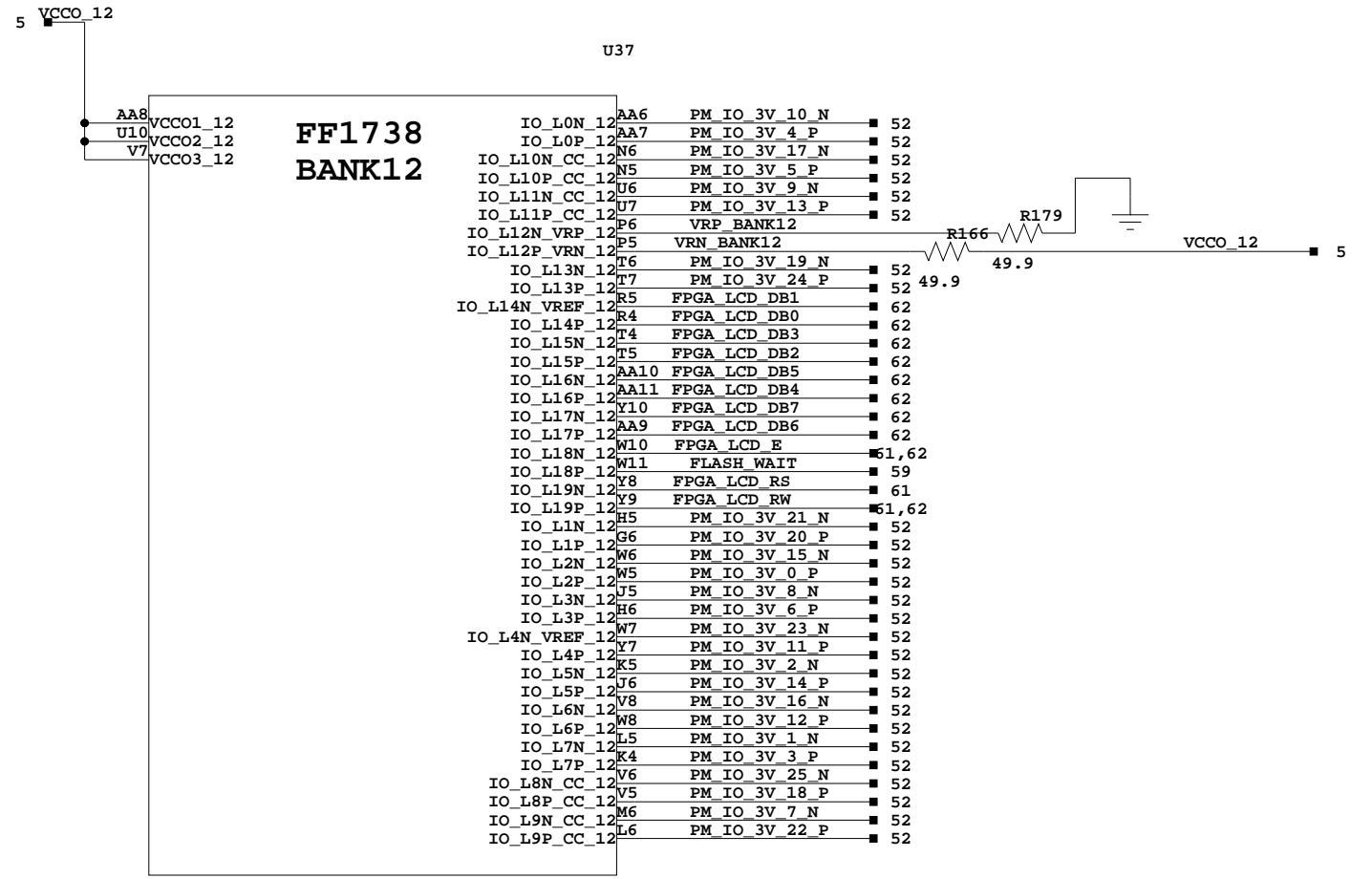
SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
FPGA - BANK 5,6 - PM, DEBUG

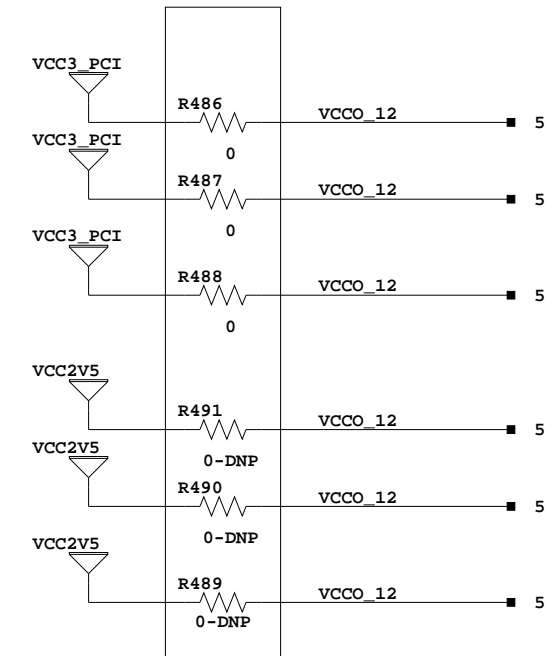
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5VLX330TFF1738



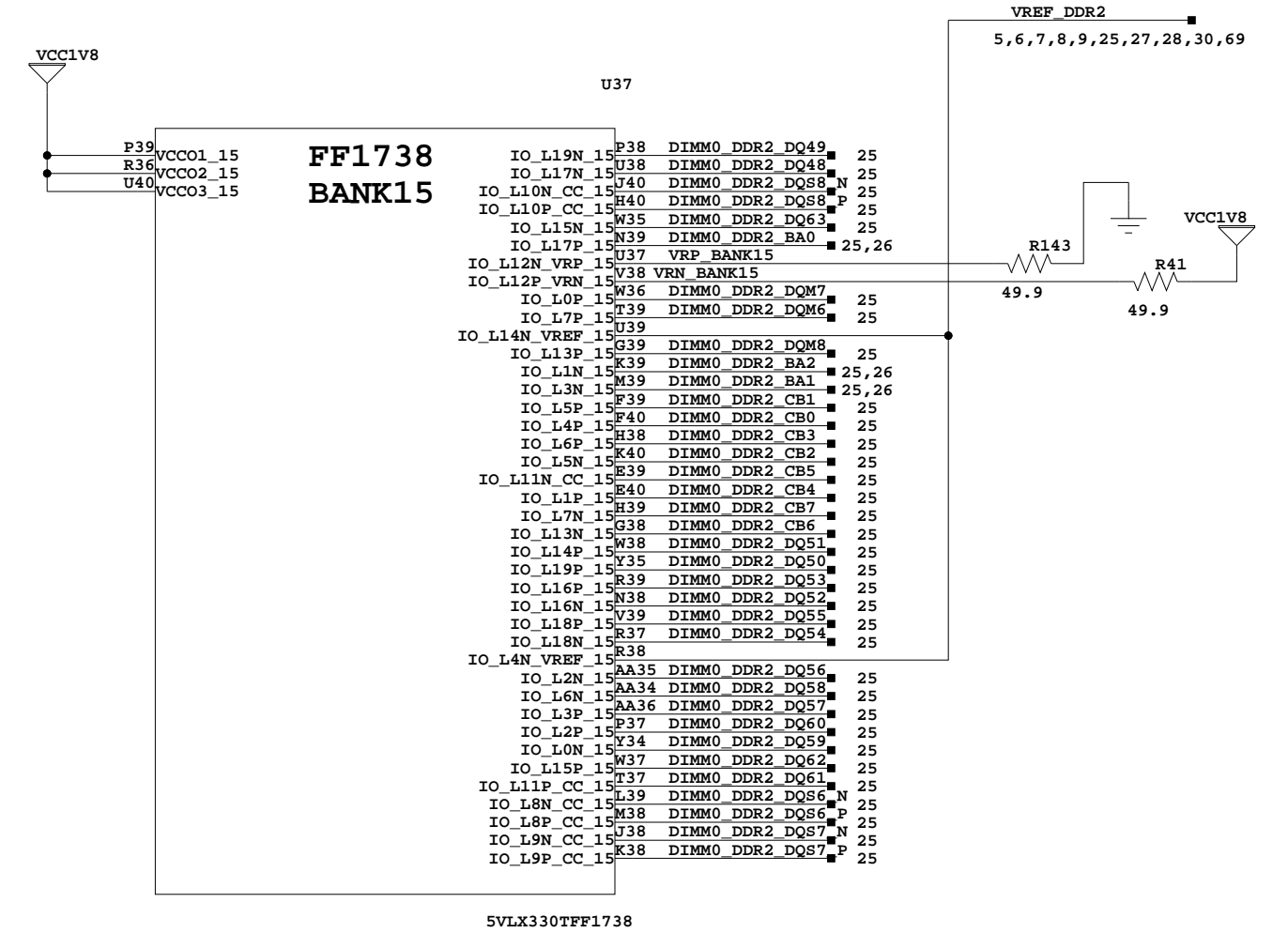
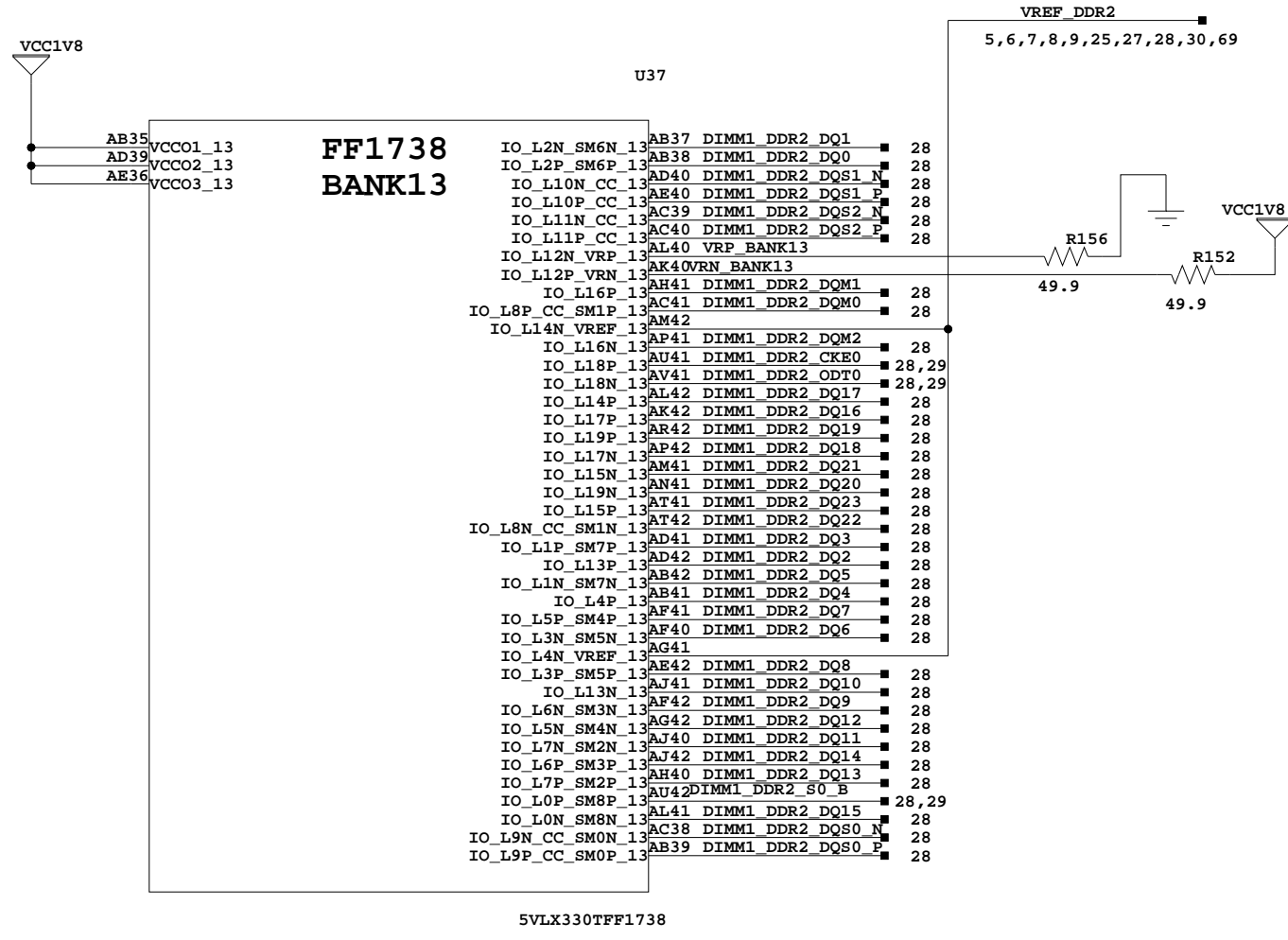
### FPGA - BANK 11,12



SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 FPGA - BANK 11,12 DDR2, PM, LCD

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**FPGA - BANK 13,15**

	SCH P/N	0381255
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	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM		
FPGA - BANK 13,15 - DDR2		
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VCC1V8

AG40  
AH37  
AK41

VCCO1\_17  
VCCO2\_17  
VCCO3\_17

**FF1738**  
**BANK17**

IO_L0N_17	AC34	DIMM1_DDR2_DQ25	28
IO_L2P_17	AB36	DIMM1_DDR2_DQ24	28
IO_L10N_CC_17	AU39	DIMM1_DDR2_DQ84_N	28
IO_L10P_CC_17	AV40	DIMM1_DDR2_DQ84_P	28
IO_L11N_CC_17	AR39	DIMM1_DDR2_DQ85_N	28
IO_L11P_CC_17	AT39	DIMM1_DDR2_DQ85_P	28
IO_L12N_VRN_17	AH39	VRN_BANK17	28
IO_L12P_VRN_17	AG39	VRN_BANK17	28
IO_L7N_17	AG37	DIMM1_DDR2_DQ4	28
IO_L4P_17	AC36	DIMM1_DDR2_DQ3	28
IO_L14N_VREF_17	AK37		28
IO_L18N_17	AN40	DIMM1_DDR2_DQ5	28
IO_L5P_17	AE39	DIMM1_DDR2_CKE1	28,29
IO_L8P_CC_17	AF37	DIMM1_DDR2_ODT1	28,29
IO_L6P_17	AP40	DIMM1_DDR2_DQ41	28
IO_L18P_17	AM38	DIMM1_DDR2_DQ40	28
IO_L17N_17	AP38	DIMM1_DDR2_DQ43	28
IO_L17N_17	AM37	DIMM1_DDR2_DQ42	28
IO_L19N_17	AK38	DIMM1_DDR2_DQ45	28
IO_L16P_17	AL39	DIMM1_DDR2_DQ44	28
IO_L5N_17	AN39	DIMM1_DDR2_DQ47	28
IO_L17P_17	AN38	DIMM1_DDR2_DQ46	28
IO_L0P_17	AE38	DIMM1_DDR2_DQ27	28
IO_L2N_17	AD36	DIMM1_DDR2_DQ26	28
IO_L3P_17	AC35	DIMM1_DDR2_DQ29	28
IO_L13P_17	AB34	DIMM1_DDR2_DQ28	28
IO_L3N_17	AD37	DIMM1_DDR2_DQ31	28
IO_L1P_17	AD35	DIMM1_DDR2_DQ30	28
IO_L4N_VREF_17	AD38		28
IO_L8N_CC_17	AJ38	DIMM1_DDR2_DQ32	28
IO_L1N_17	AL37	DIMM1_DDR2_DQ34	28
IO_L15N_17	AH38	DIMM1_DDR2_DQ33	28
IO_L7P_17	AF39	DIMM1_DDR2_DQ36	28
IO_L6N_17	AM39	DIMM1_DDR2_DQ35	28
IO_L15P_17	AK39	DIMM1_DDR2_DQ38	28
IO_L13N_17	AG38	DIMM1_DDR2_DQ37	28
IO_L16N_17	AE37	DIMM1_DDR2_S1_B	28,29
IO_L14P_17	AJ37	DIMM1_DDR2_DQ39	28
IO_L9N_CC_17	AT40	DIMM1_DDR2_DQ83_N	28
IO_L9P_CC_17	AR40	DIMM1_DDR2_DQ83_P	28

5VLX330TFF1738

VREF\_DDR2  
5,6,8,9,25,27,28,30,69

R244  
49.9

R206  
49.9

VCC1V8

VCC2V5

AD9  
AE6  
AG10

VCCO1\_18  
VCCO2\_18  
VCCO3\_18

**FF1738**  
**BANK18**

IO_L0N_18	AK7	PM_IO_39_N	52
IO_L0P_18	AJ7	PM_IO_38_P	52
IO_L10N_CC_18	AC6	PM_IO_59_N	52
IO_L10P_CC_18	AC5	PM_IO_58_P	52
IO_L11N_CC_18	AF6	PM_IO_61_N	52
IO_L11P_CC_18	AF5	PM_IO_60_P	52
IO_L12N_VRN_18	AD7	VRN_BANK18	52
IO_L12P_VRN_18	AD6	VRN_BANK18	52
IO_L13N_18	AG7	PM_IO_63_N	52
IO_L13P_18	AG6	PM_IO_62_P	52
IO_L14N_VREF_18	AD5	PM_IO_65_N	52
IO_L14P_18	AE5	PM_IO_64_P	52
IO_L15N_18	AF7	PM_IO_66_P	52
IO_L15P_18	AE8	PM_IO_69_P	52
IO_L16N_18	AE8	PM_IO_68_P	52
IO_L16P_18	AD8	PM_IO_68_P	52
IO_L17N_18	AF10	PM_IO_71_N	52
IO_L17P_18	AF9	PM_IO_70_P	52
IO_L18N_18	AE10	PM_IO_73_N	52
IO_L18P_18	AE9	PM_IO_72_P	52
IO_L19N_18	AF12	PM_IO_75_N	52
IO_L19P_18	AF11	PM_IO_74_P	52
IO_L1N_18	AC10	PM_IO_41_P	52
IO_L1P_18	AB11	PM_IO_40_P	52
IO_L2N_18	AK5	PM_IO_43_N	52
IO_L2P_18	AL5	PM_IO_42_P	52
IO_L3N_18	AB8	PM_IO_45_N	52
IO_L3P_18	AB9	PM_IO_44_P	52
IO_L4N_VREF_18	AJ5	PM_IO_47_N	52
IO_L4P_18	AJ6	PM_IO_46_P	52
IO_L5N_18	AC9	PM_IO_49_N	52
IO_L5P_18	AC8	PM_IO_48_P	52
IO_L6N_18	AH5	PM_IO_51_N	52
IO_L6P_18	AH6	PM_IO_50_P	52
IO_L7N_18	AD11	PM_IO_53_N	52
IO_L7P_18	AD10	PM_IO_52_P	52
IO_L8N_CC_18	AH4	PM_IO_55_N	52
IO_L8P_CC_18	AG4	PM_IO_54_P	52
IO_L9N_CC_18	AB6	PM_IO_57_N	52
IO_L9P_CC_18	AB7	PM_IO_56_P	52

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R199  
49.9

R198  
49.9

VCC2V5

### FPGA - BANK 17,18



SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
FPGA - BANK 17,18 - DDR2, PM

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VCC1V8

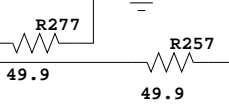
G40 VCC01\_19  
K41 VCC02\_19  
L38 VCC03\_19

### FF1738 BANK19

IO_L8P_CC_19	G36	DIMMO_DDR2_DQ25	25
IO_L18P_19	F37	DIMMO_DDR2_DQ24	25
IO_L10N_CC_19	F36	DIMMO_DDR2_DQS4_N	25
IO_L10P_CC_19	R35	DIMMO_DDR2_DQS4_P	25
IO_L11N_CC_19	V36	DIMMO_DDR2_DQS5_N	25
IO_L11P_CC_19	U36	DIMMO_DDR2_DQS5_P	25
IO_L12N_VRP_19	G37	VRP_BANK19	25
IO_L12P_VRN_19	H36	VRN_BANK19	25
IO_L0N_19	M36	DIMMO_DDR2_DQM4	25
IO_L13P_19	F36	DIMMO_DDR2_DQM3	25
IO_L14N_VREF_19	E37		25
IO_L0P_19	V35	DIMMO_DDR2_DQM5	25
IO_L2P_19	L37	DIMMO_DDR2_CKE1	25,26
IO_L2N_19	K35	DIMMO_DDR2_ODT1	25,26
IO_L5N_19	W32	DIMMO_DDR2_DQ41	25
IO_L14P_19	V33	DIMMO_DDR2_DQ40	25
IO_L19N_19	AA32	DIMMO_DDR2_DQ43	25
IO_L16P_19	Y32	DIMMO_DDR2_DQ42	25
IO_L16N_19	T35	DIMMO_DDR2_DQ45	25
IO_L19P_19	R34	DIMMO_DDR2_DQ44	25
IO_L17N_19	W33	DIMMO_DDR2_DQ47	25
IO_L17P_19	Y33	DIMMO_DDR2_DQ46	25
IO_L13N_19	K37	DIMMO_DDR2_DQ27	25
IO_L4P_19	J36	DIMMO_DDR2_DQ26	25
IO_L8N_CC_19	E38	DIMMO_DDR2_DQ29	25
IO_L15N_19	D37	DIMMO_DDR2_DQ28	25
IO_L5P_19	J37	DIMMO_DDR2_DQ31	25
IO_L7N_19	H35	DIMMO_DDR2_DQ30	25
IO_L4N_VREF_19	L35		25
IO_L7P_19	N35	DIMMO_DDR2_DQ32	25
IO_L6N_19	V34	DIMMO_DDR2_DQ34	25
IO_L15P_19	P36	DIMMO_DDR2_DQ33	25
IO_L1P_19	J35	DIMMO_DDR2_DQ36	25
IO_L3P_19	U34	DIMMO_DDR2_DQ35	25
IO_L3N_19	N36	DIMMO_DDR2_DQ38	25
IO_L1N_19	L36	DIMMO_DDR2_DQ37	25
IO_L18N_19	M37	DIMMO_DDR2_S1_B	25
IO_L6P_19	P35	DIMMO_DDR2_DQ39	25,26
IO_L9N_CC_19	U33	DIMMO_DDR2_DQS3_N	25
IO_L9P_CC_19	T34	DIMMO_DDR2_DQS3_P	25

5VLX330TFF1738

VREF\_DDR2  
5,6,7,9,25,27,28,30,69



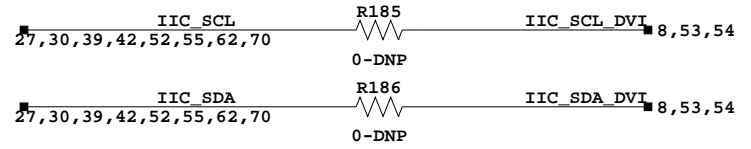
VCC3\_PCI

L8 VCC01\_20  
P9 VCC02\_20  
R6 VCC03\_20

### FF1738 BANK20

IO_L0N_20	N8	PCI_P_CBEL_B	33,35,37,40
IO_L0P_20	N9	PCI_P_CBEL_B	33,35,37,40
IO_L10N_CC_20	G8	PCI_P_SERR_B	33,35,37,38,40
IO_L10P_CC_20	G7	PCI_P_PERR_B	33,35,37,38
IO_L11N_CC_20	J9	PCI_P_CLK1_R	39
IO_L11P_CC_20	U8	PCI_P_CLK0_R	39
IO_L12N_VRP_20	H9	UART0_TXD	44
IO_L12P_VRN_20	H8	UART0_CTS_B	44
IO_L13N_20	F11	UART0_RXD	44
IO_L13P_20	F10	UART1_TXD	44
IO_L14N_VREF_20	J7	UART0_RTS_B	44
IO_L14P_20	J8	UART1_CTS_B	44
IO_L15N_20	V11	UART1_RXD	44
IO_L15P_20	U11	PCI_P_CLK4_R	39
IO_L16N_20	K9	UART1_RTS_B	44
IO_L16P_20	K8	FPGA_SDA	39
IO_L17N_20	L7	FPGA_SCL	39
IO_L17P_20	K7	FLASH_RESET_B	39
IO_L18N_20	M8	DVI_DE	59
IO_L18P_20	M7	IIC_SDA_DVI	53
IO_L19N_20	L9	IIC_SCL_DVI	8,53,54
IO_L19P_20	M9	PCI_P_CLK3_R	39
IO_L1N_20	E8	PCI_P_PAR	33,35,37,40
IO_L1P_20	E9	PCI_P_CBEO_B	33,35,37,40
IO_L2N_20	F8	PCI_P_IRDY_B	33,35,37,38,40
IO_L2P_20	F7	PCI_P_FRAME_B	33,35,37,38,40
IO_L3N_20	E7	PCI_P_REQ0_B	35,38
IO_L3P_20	D7	PCI_P_REQ2_B	38
IO_L4N_VREF_20	R8	PCI_P_REQ1_B	37,38
IO_L4P_20	R7	PCI_P_REQ4_B	33,38
IO_L5N_20	F6	PCI_P_REQ3_B	33,38
IO_L5P_20	F7	PCI_P_GNT1_B	38,40,43
IO_L6N_20	F9	PCI_P_GNT0_B	37,38
IO_L6P_20	F9	PCI_P_GNT3_B	35,38
IO_L7N_20	F5	PCI_P_GNT2_B	38,40
IO_L7P_20	E5	PCI_P_GNT4_B	33,38
IO_L8N_CC_20	V10	PCI_P_TRDY_B	33,35,37,38,40
IO_L8P_CC_20	V9	PCI_P_CLK5_R	39
IO_L9N_CC_20	F9	PCI_P_STOP_B	39
IO_L9P_CC_20	F9	PCI_P_DEVSEL_B	33,35,37,38,40

5VLX330TFF1738



## FPGA - BANK 19,20



SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

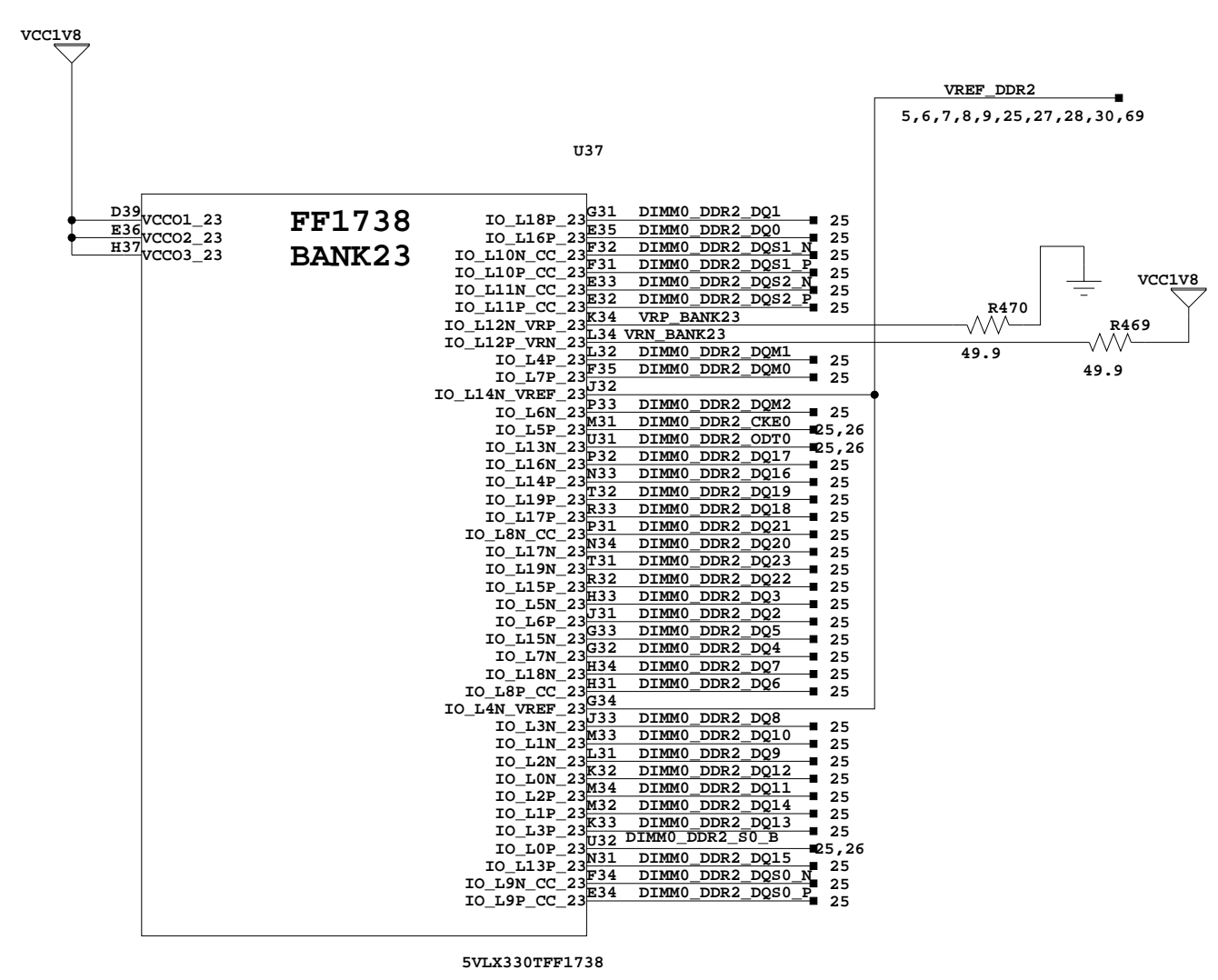
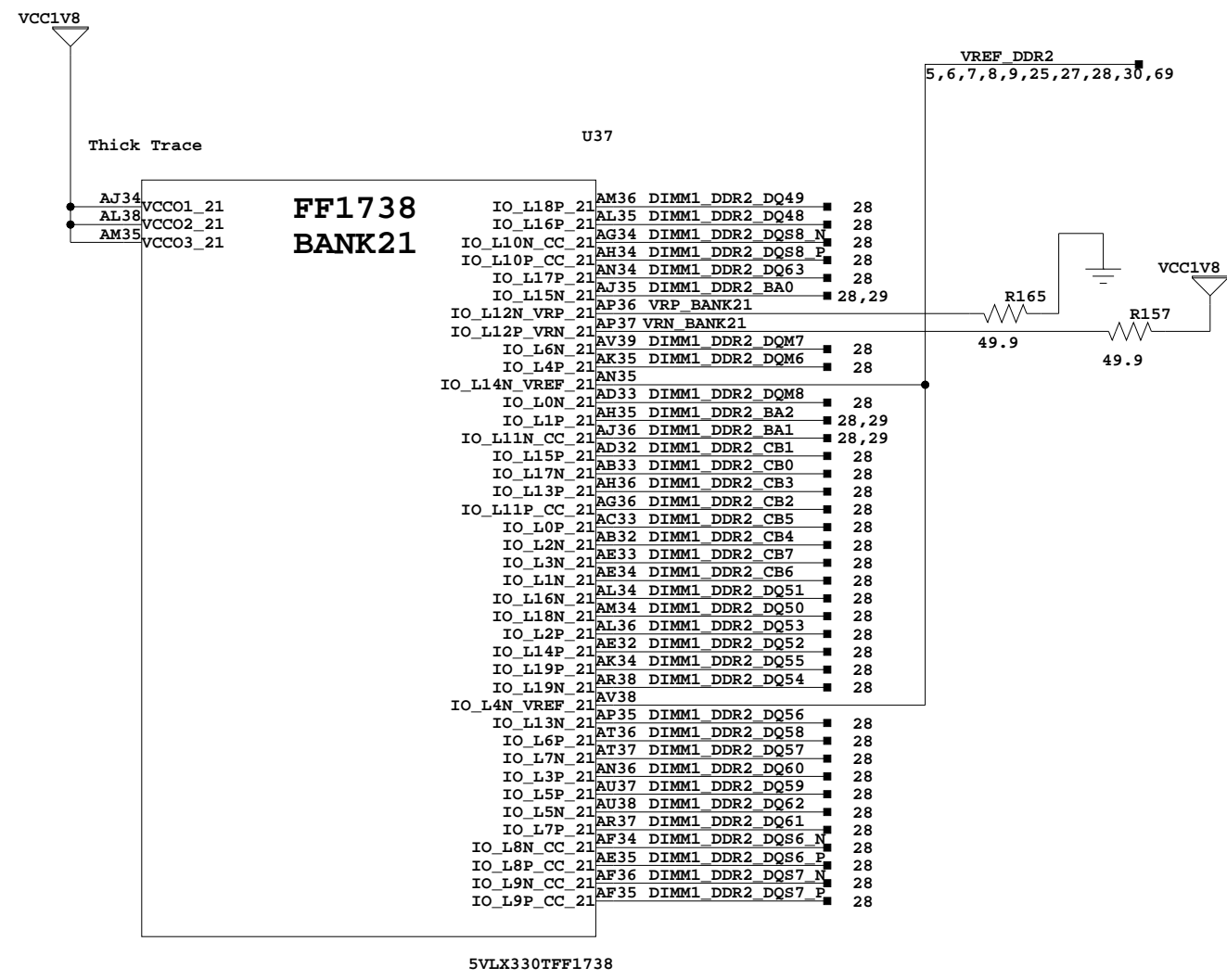
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
FPGA - BANK 19,20 DDR2, PCI, IIC, UART

Date: 8-1-2008\_15:03 Ver: C

Sheet Size: B Rev: 01

Sheet 8 of 70 Drawn By BF





### FPGA - BANK 21,23



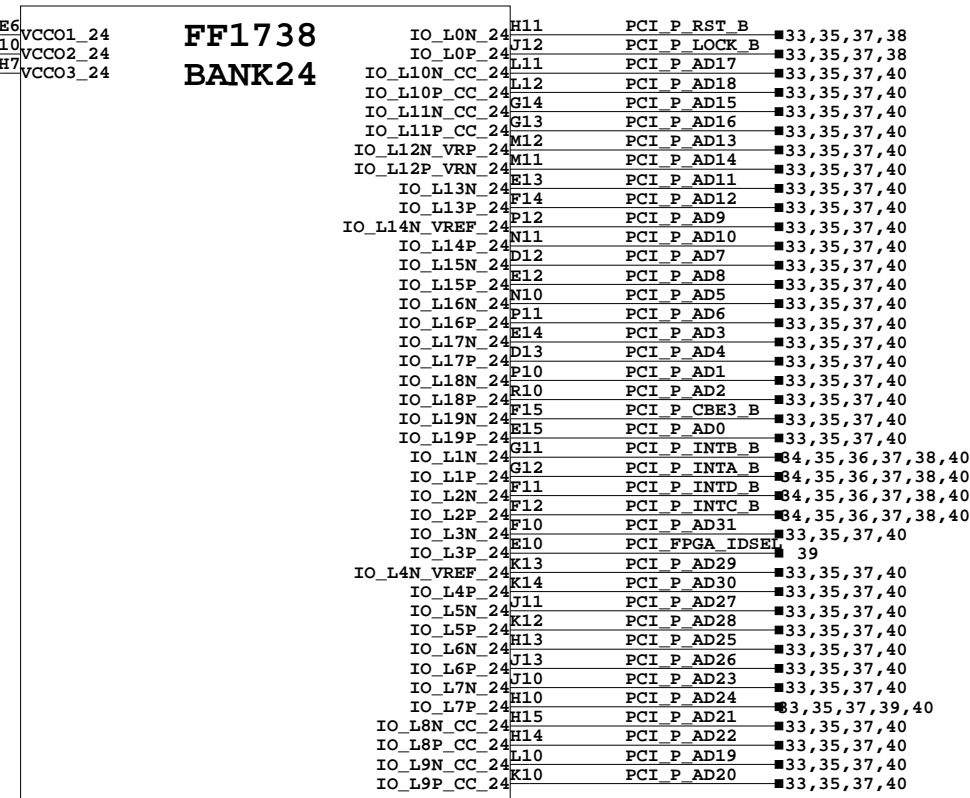
SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 FPGA - BANK 21,23 DDR2

Date:	8-1-2008_15:03	Ver:	C
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VCC3\_PCI

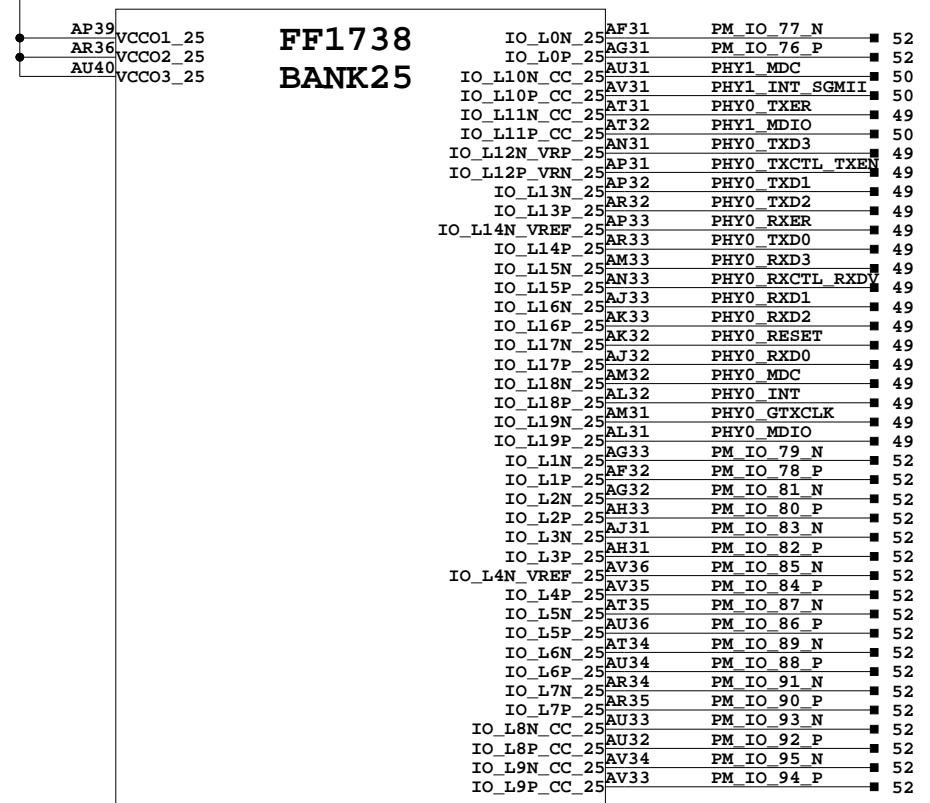
U37



5VLX330TFF1738

VCC2V5

U37



5VLX330TFF1738

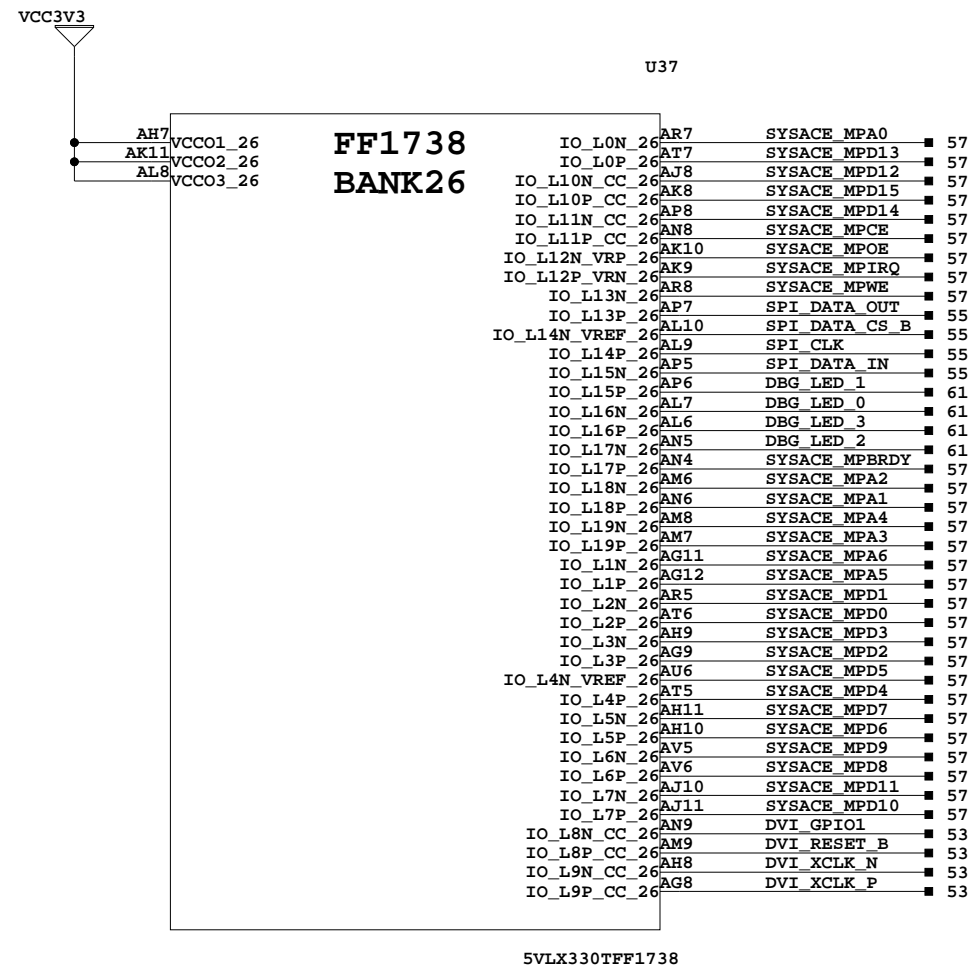
### FPGA - BANK 24,25



SCH P/N	0381255
ART P/N	0532059
FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTRM  
 FPGA - BANK 24,25 PCI, PERSONALITY MODULE, PHY

Date:	8-1-2008_15:03	Ver:	C
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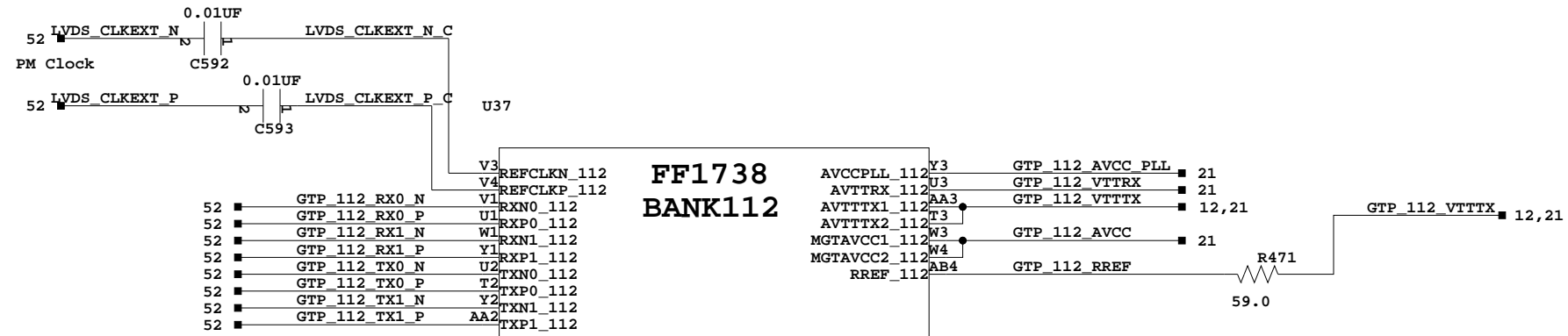
### FPGA - BANK 26



SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

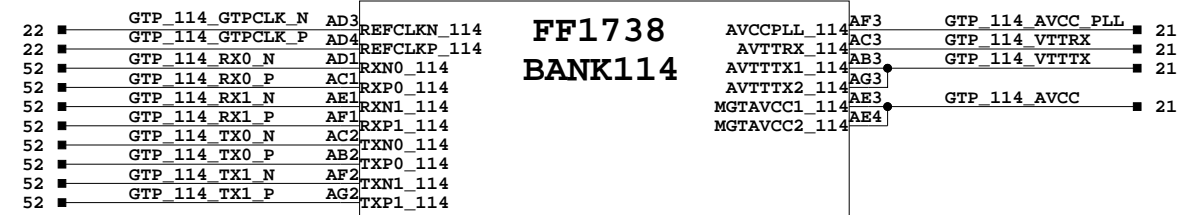
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 FPGA - BANK 26 SYSTEM ACE, DVI, SPI, LEDES

Date:	8-1-2008_15:03	Ver:	C
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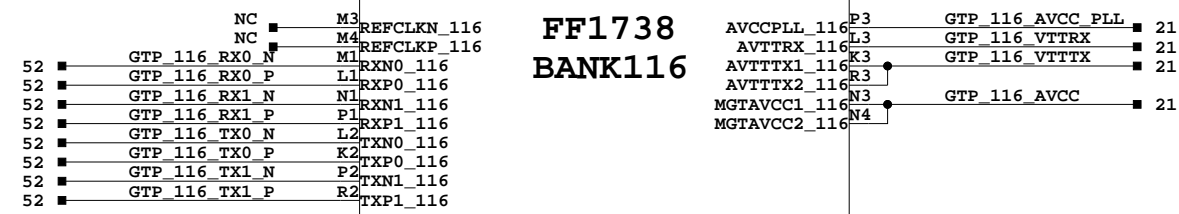
5VLX330TFF1738

U37



5VLX330TFF1738

U37



5VLX330TFF1738

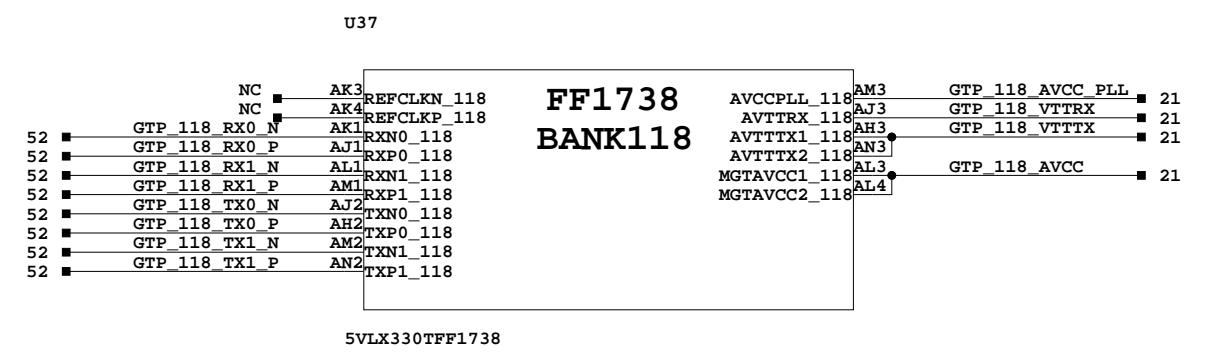
### FPGA - BANK 112, 114, 116



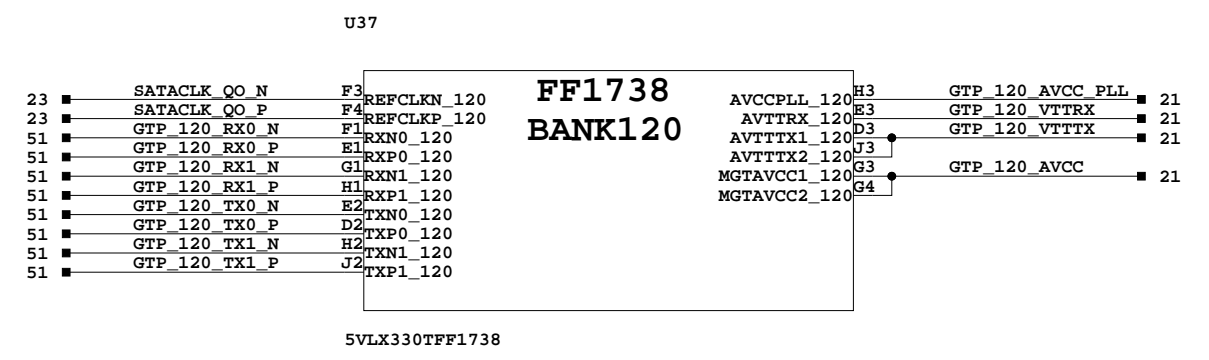
SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 FPGA-BANK 112, 114, 116 PERSONALITY MODULES

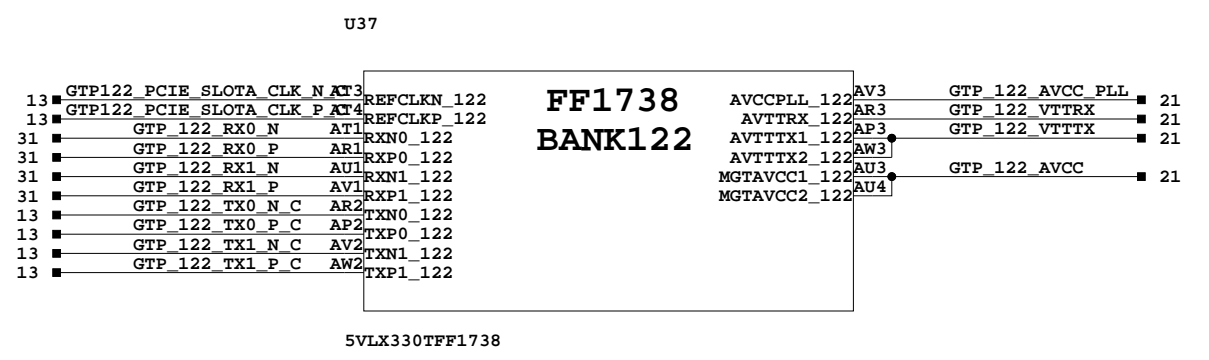
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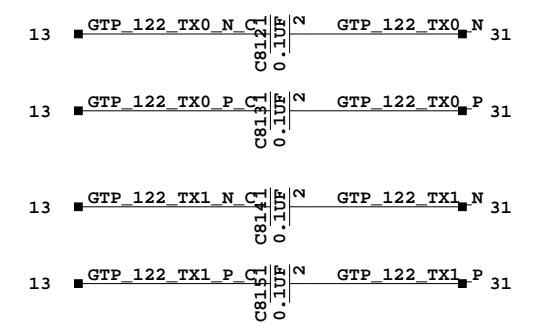
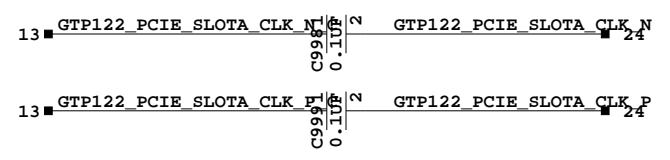
PM



SATA  
SATA Clock



PCIE Slot A

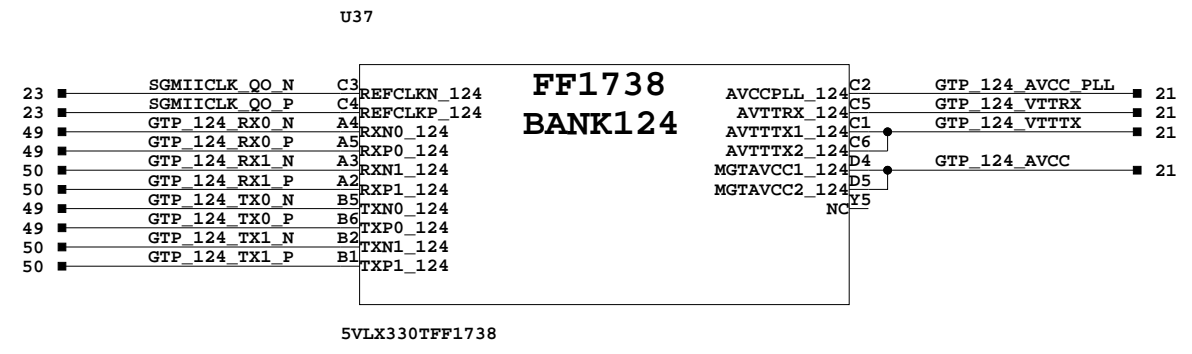


### FPGA - BANK 118,120,122

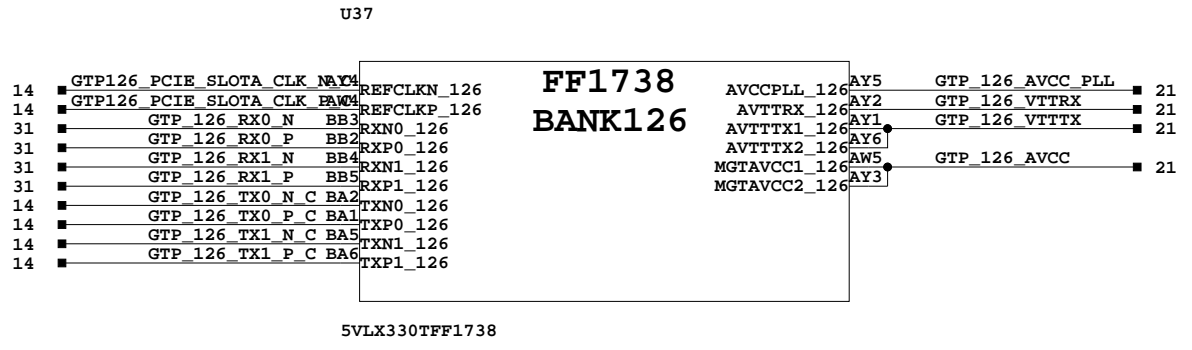


SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

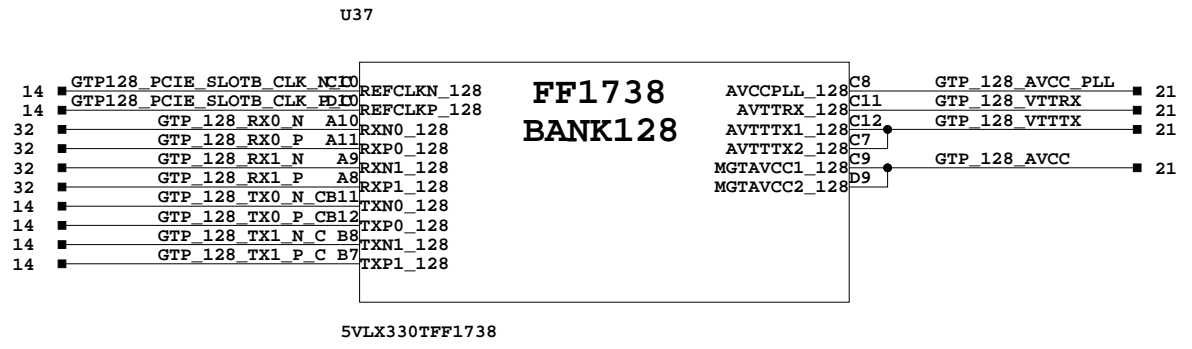
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM FPGA - BANK 118,120,122 PM, SATA, PCI-E		
Date: 8-1-2008_15:03	Ver: C	
Sheet Size: B	Rev: 01	
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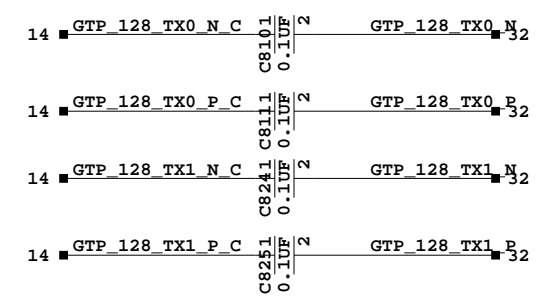
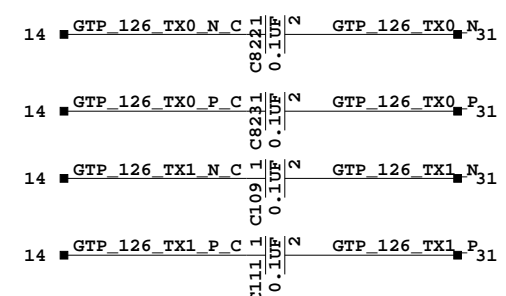
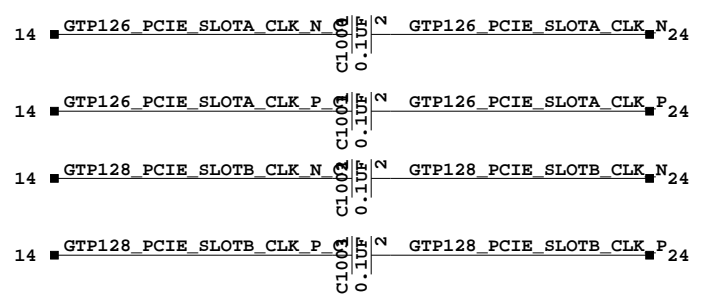
SGMII



PCie Slot A



PCie Slot B  
(FX130T / FX200T / LX330T only)

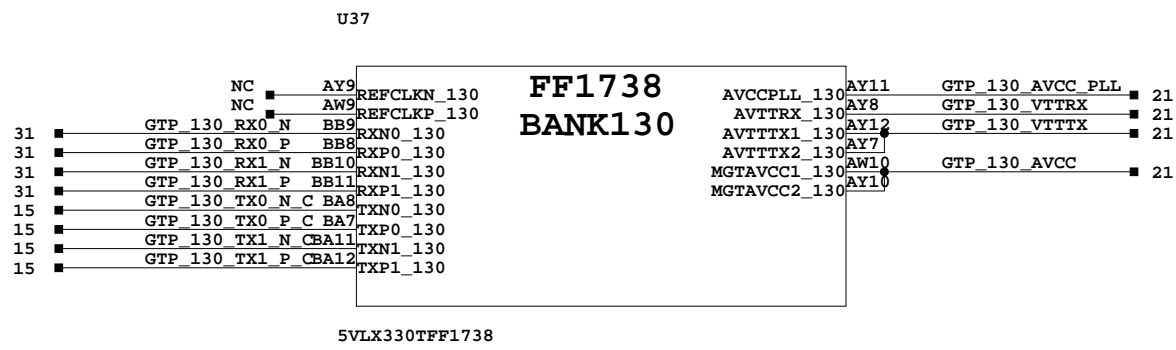


### FPGA - BANK 124,126,128

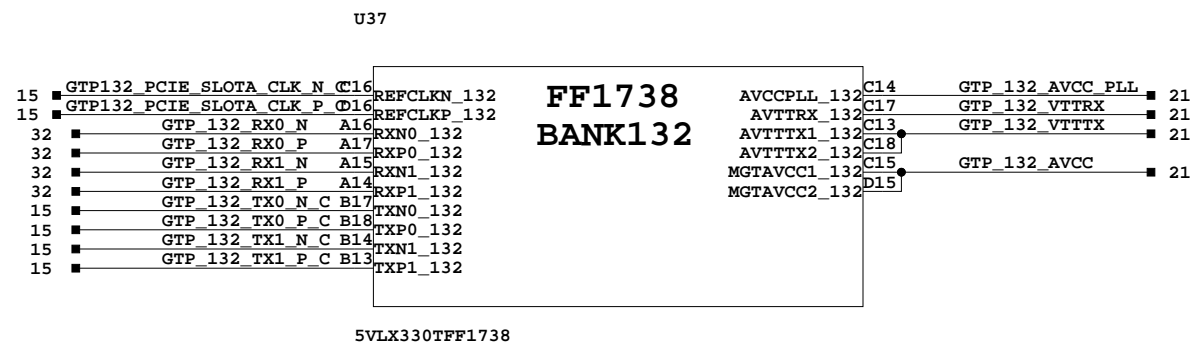


SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

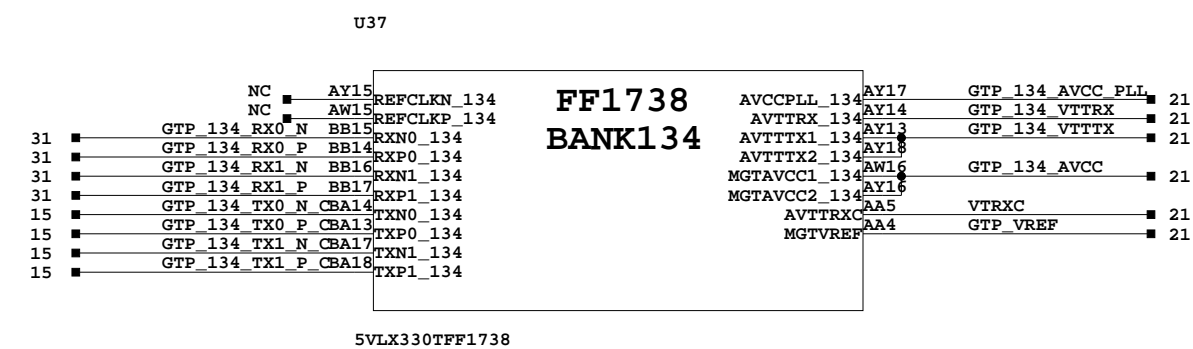
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTRM FPGA - BANK 124,126,128 SGMII, PCI-E		
Date: 8-1-2008_15:03	Ver: C	
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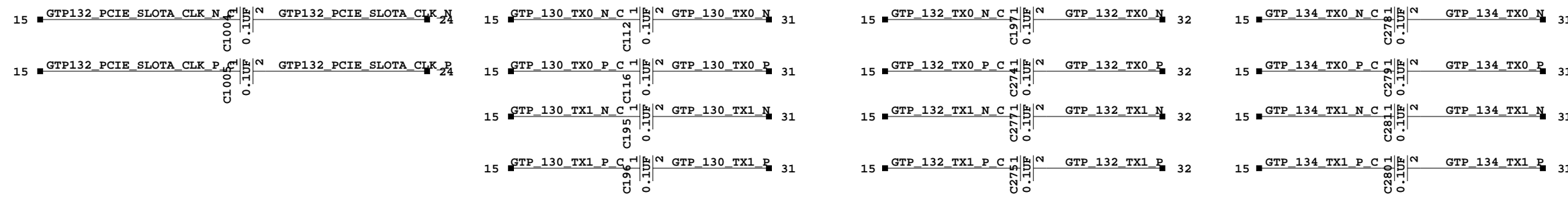
PCie Slot A  
(FX130T / FX200T / LX330T only)



PCie Slot B  
(FX200T / LX330T only)



PCie Slot A  
(FX200T / LX330T only)



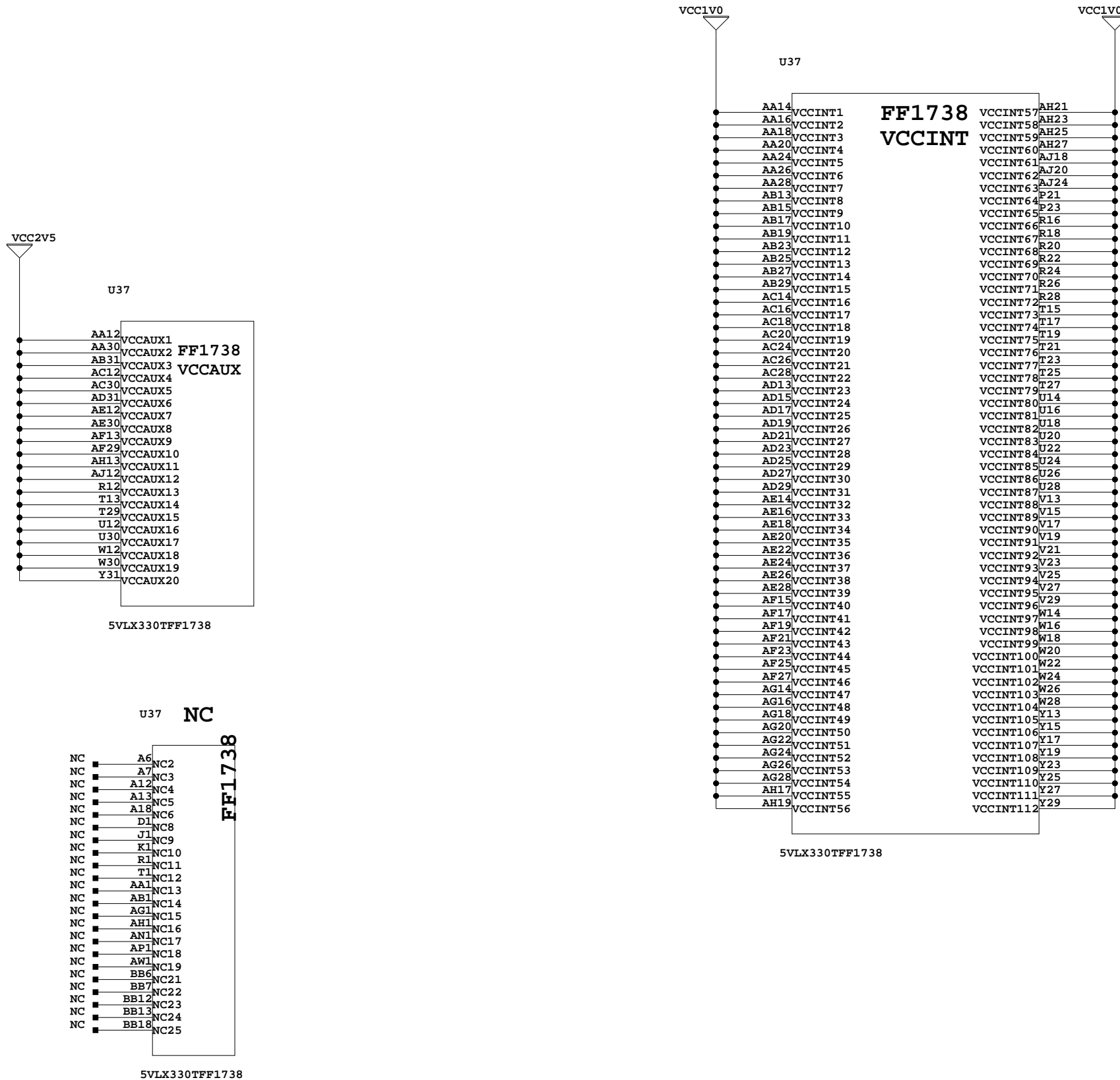
**FPGA - BANK 130,132,134**



SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
FPGA - BANK 130,132,134 PCI-E

Date:	8-1-2008_15:03	Ver:	C
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**FPGA - VCCAUX, VCCINT, NC**



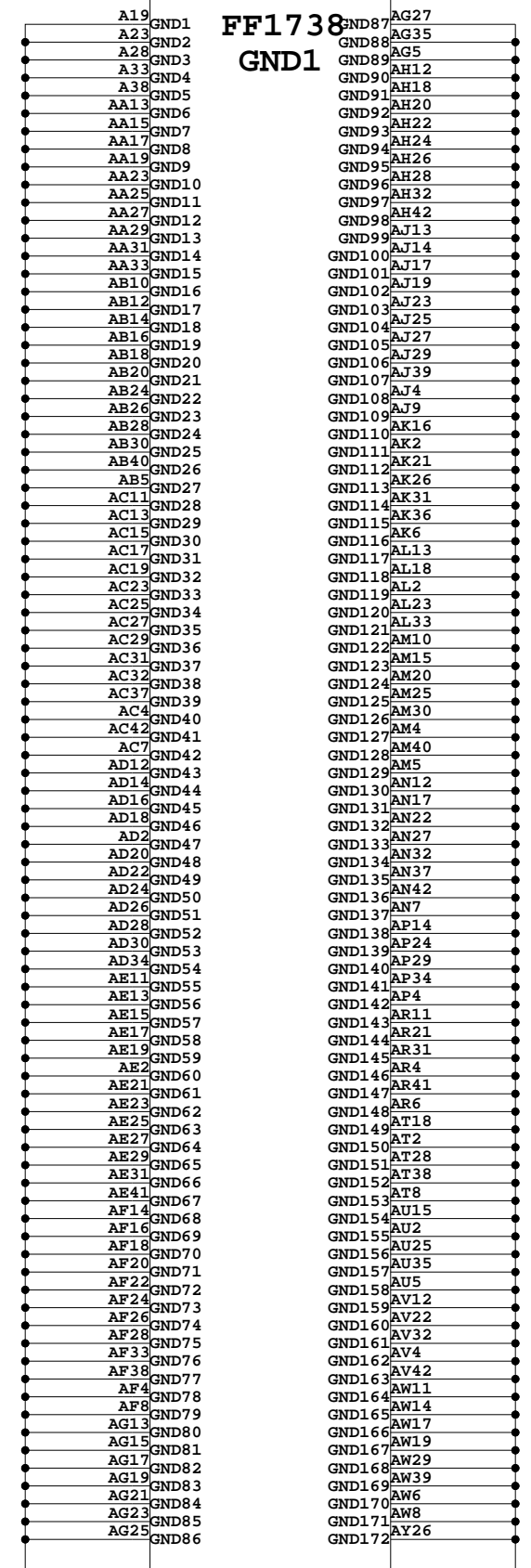
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 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 FPGA - VCCAUX, VCCINT, NC

Date:	8-1-2008_15:04	Ver:	C
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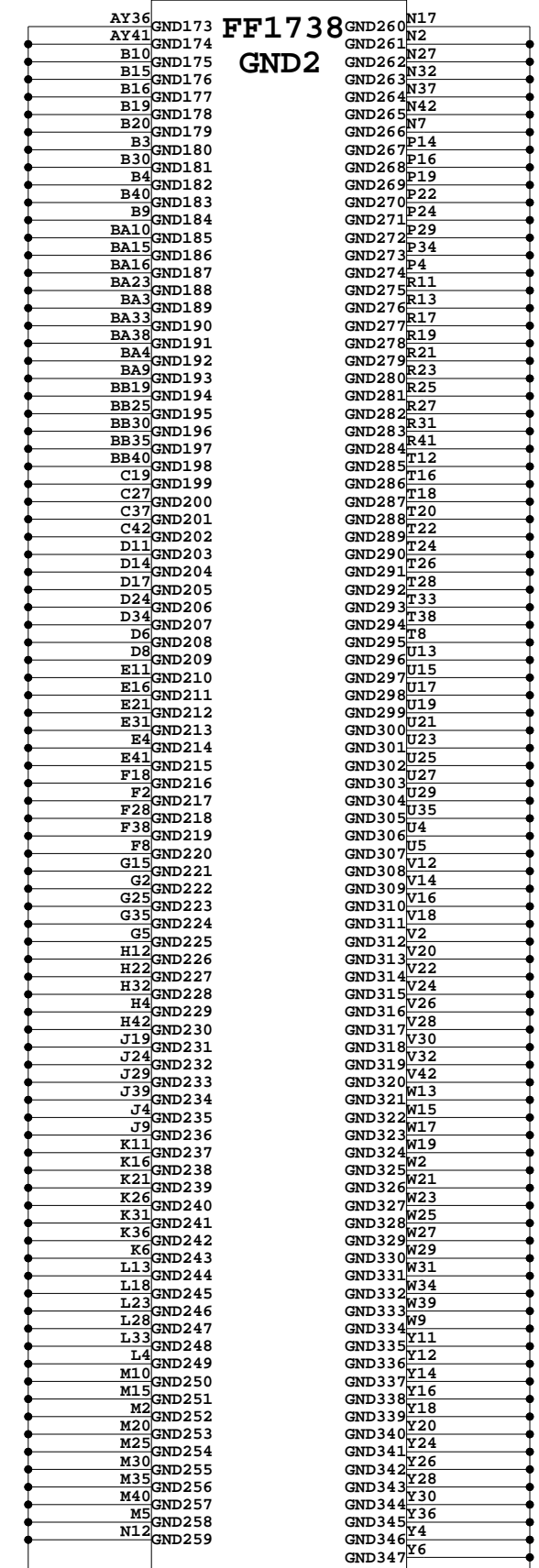


U37



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U37



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### FPGA - GND



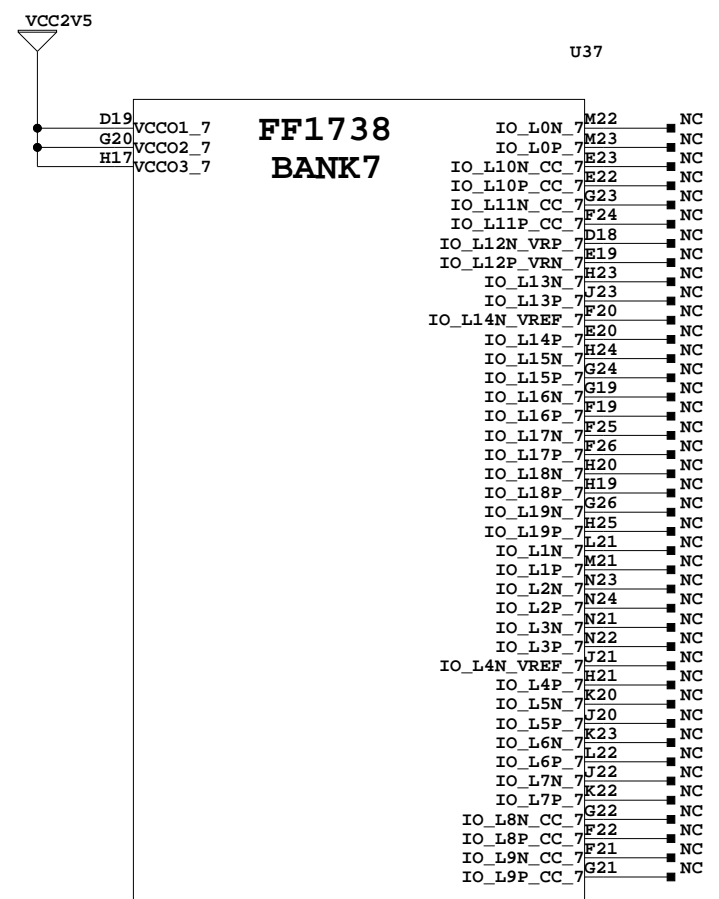
SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 FPGA GROUND PINS

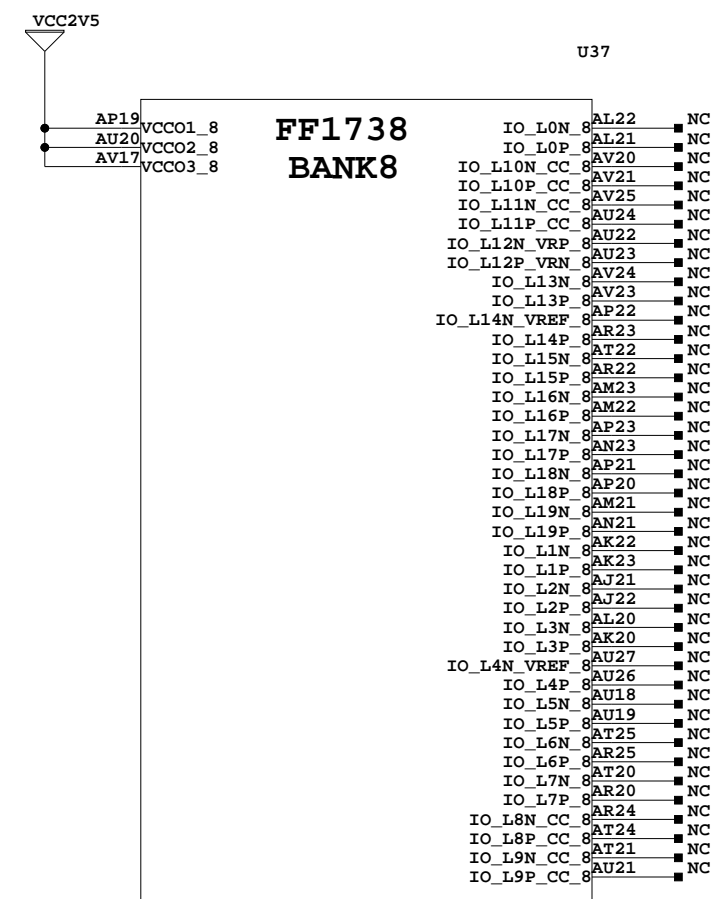
Date: 7-10-2008\_10:19 Ver: C

Sheet Size: B Rev: 01

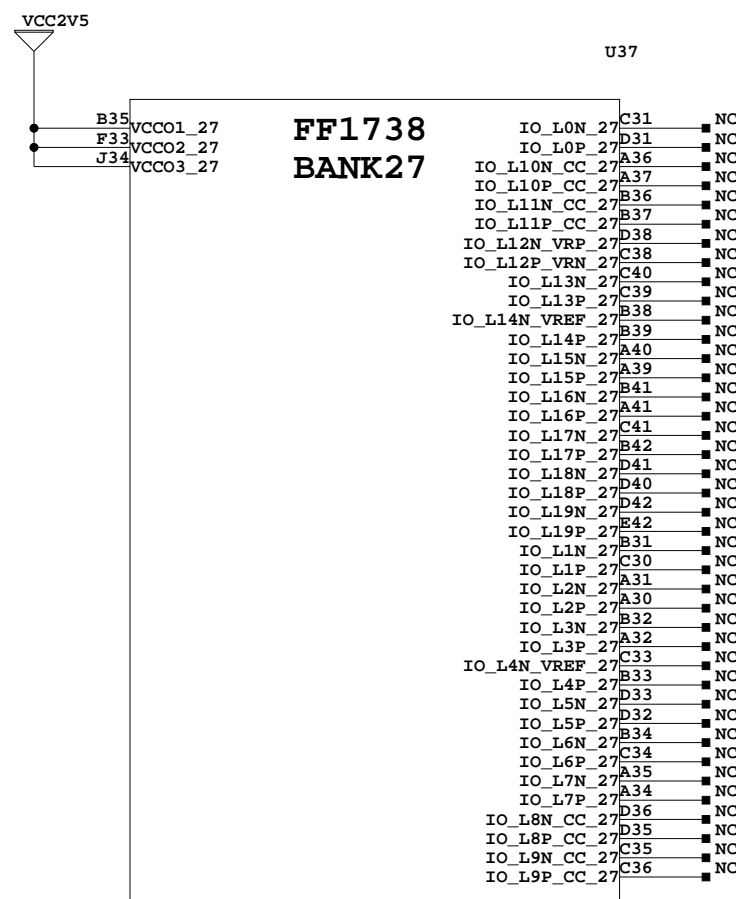
Sheet 17 of 70 Drawn By BF



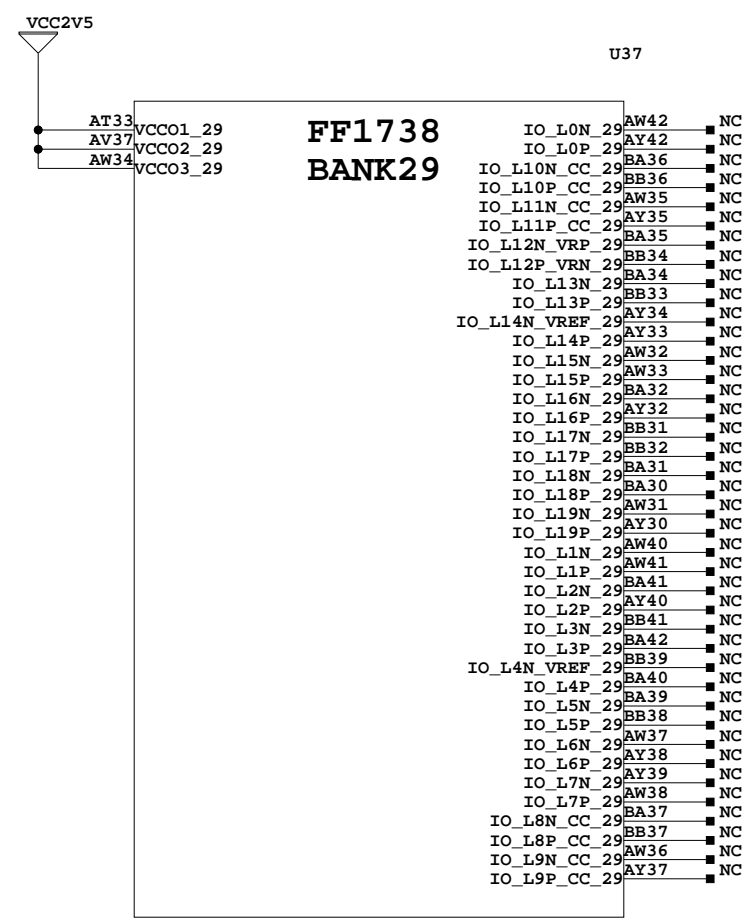
5VLX330TFF1738



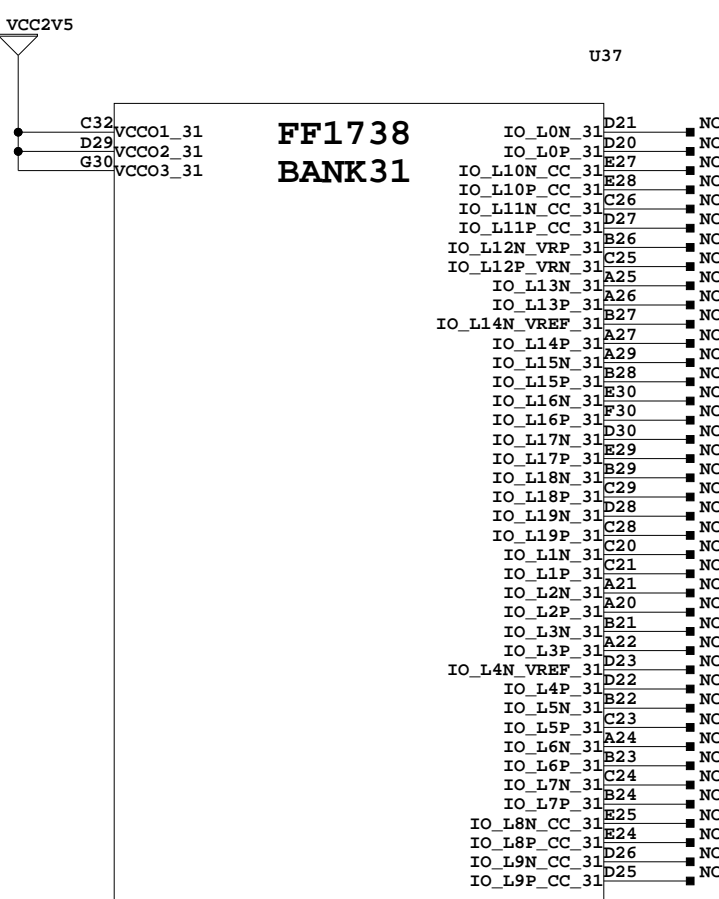
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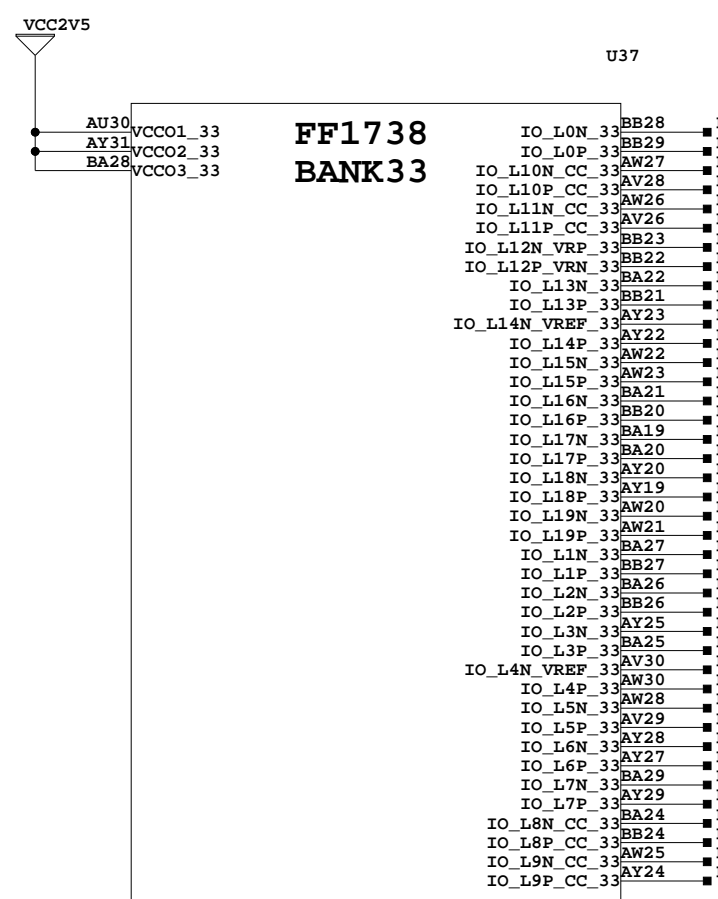
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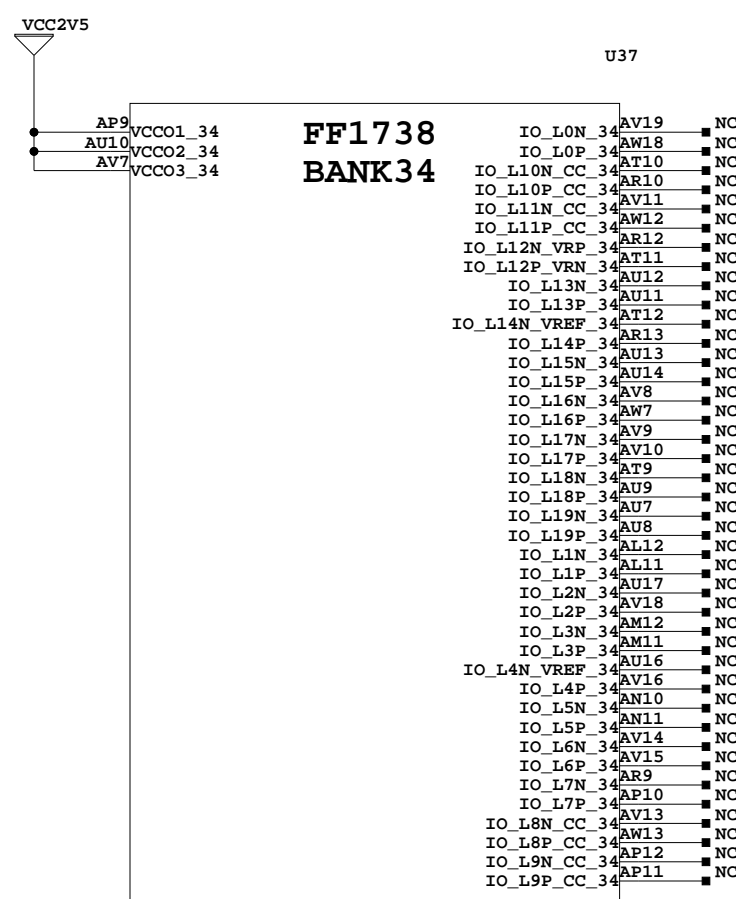
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5VLX330TFF1738

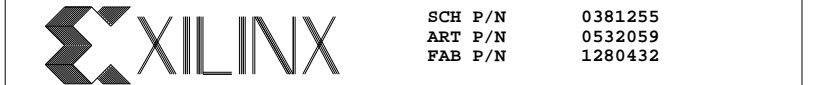


5VLX330TFF1738



5VLX330TFF1738

### FPGA - BANK 7,8,27,29,31,33,34

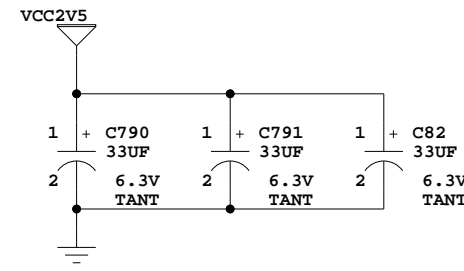


SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

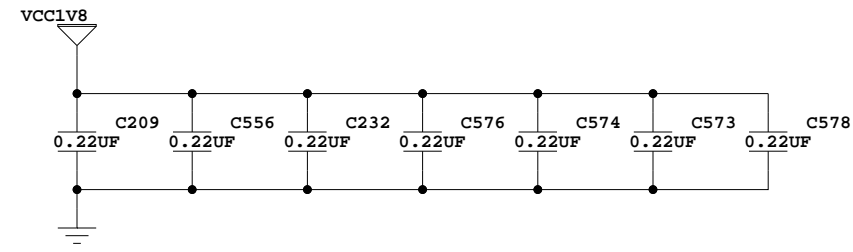
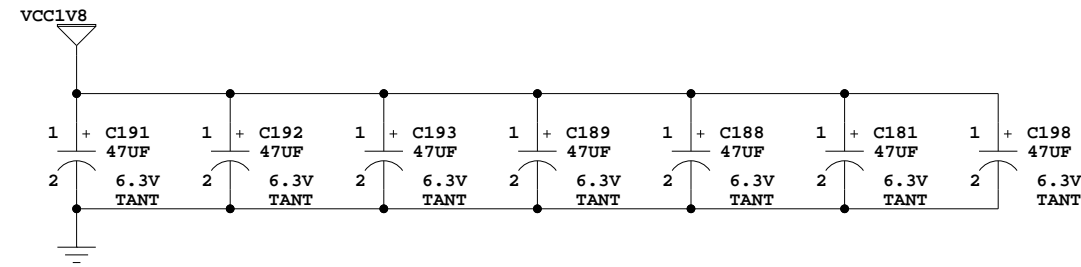
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
FPGA - BANK 7,8,27,29,31,33,34 UNUSED BANKS

Date:	7-10-2008_10:19	Ver:	C
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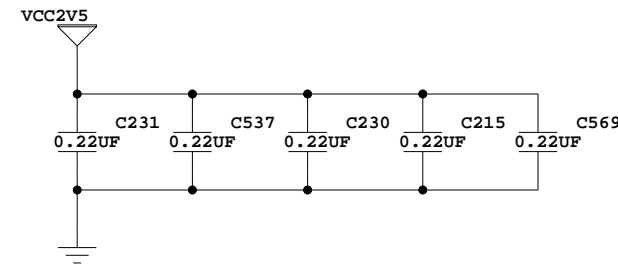
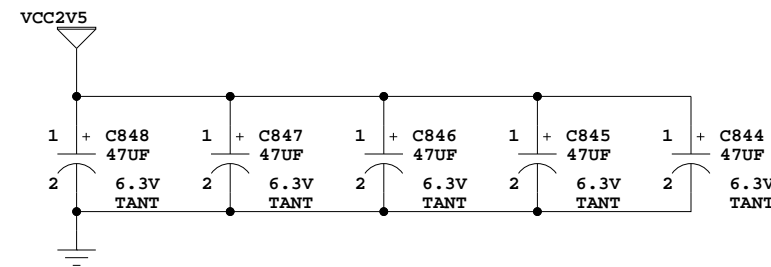
### VCCAUX 2.5V



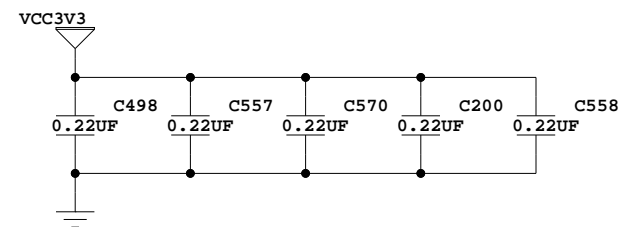
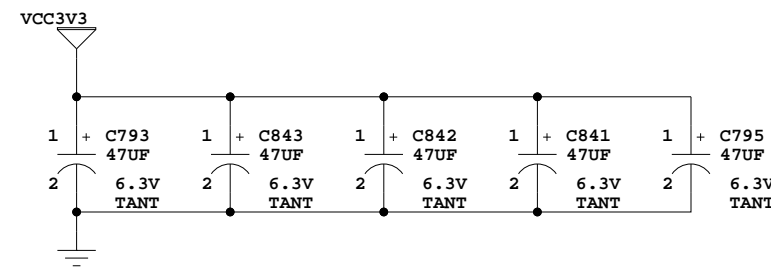
### VCCO 1.8V



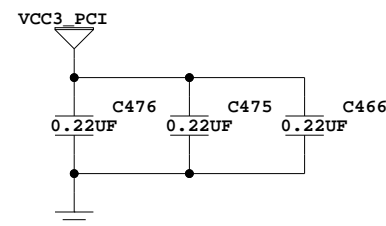
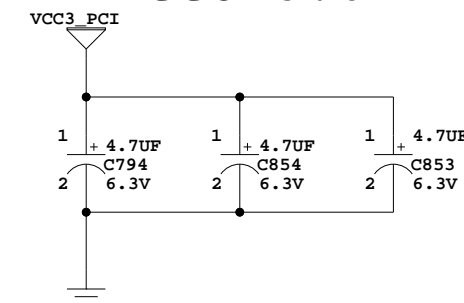
### VCCO 2.5V



### VCCO 3.3V



### VCCO 3.0V PCI



Supply	Banks Used	Capacitors Used
VCCAUX 2.5V	N/A	33uf: 3
VCCINT 1.0V	N/A	330uf: 7 / 0.22uf: 52
VCCO 3.3V	0,1,2,4,26	47uf: 5 / 0.22uf: 5
VCCO 2.5V	3,5,6,18,25	47uf: 5 / 0.22uf: 5
VCCO 1.8V	11,13,15,17,19,21,23	47uf: 7 / 0.22uf: 7
VCCO 3.0V PCI	12,20,24	47uf: 3 / 0.22uf: 3

Note: Bank 12 defaults to 3.0V\_PCI

### FPGA DECOUPLING

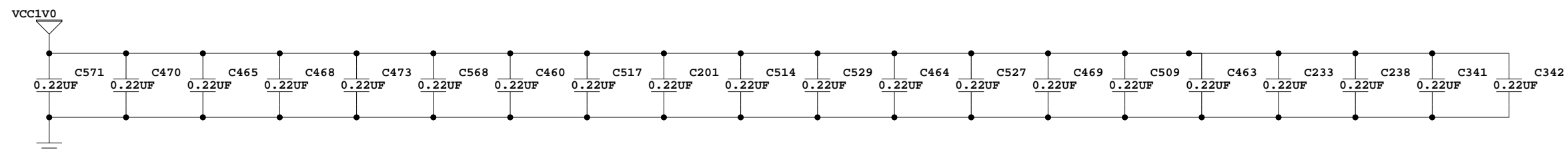
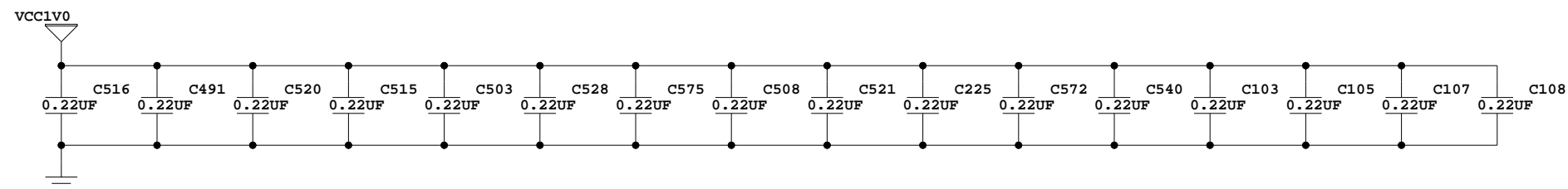
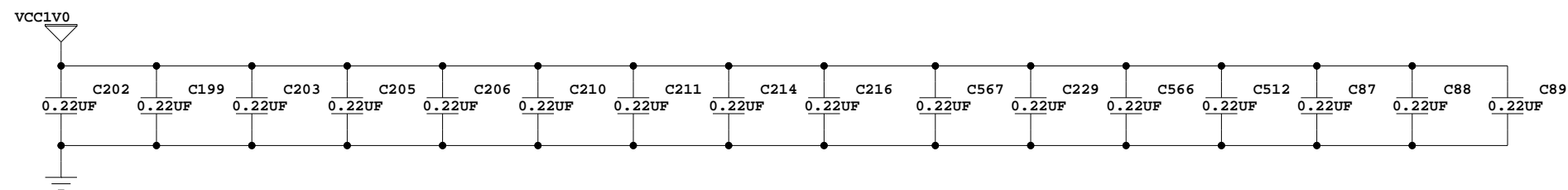
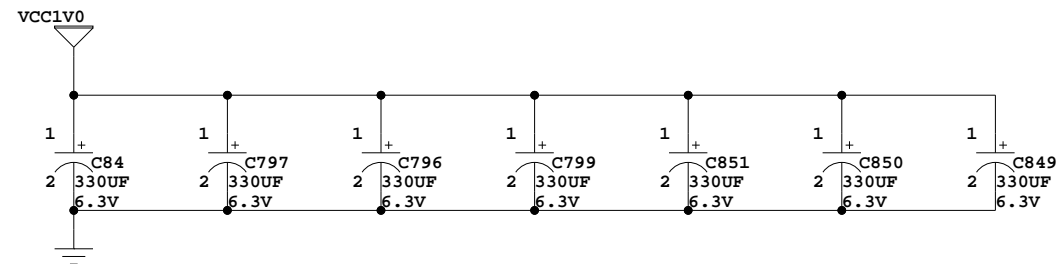


SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOrm  
FPGA DECOUPLING

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# VCCINT 1.0V



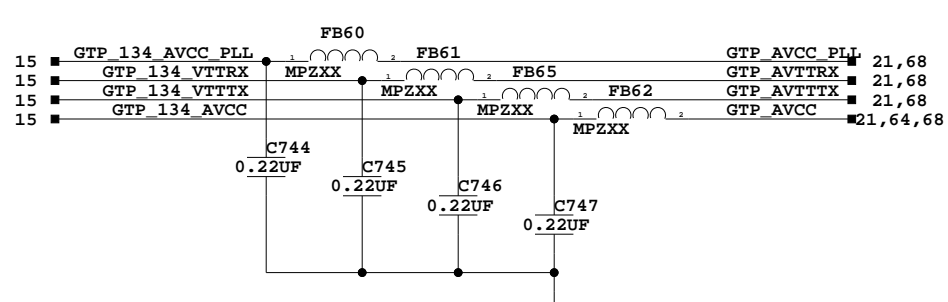
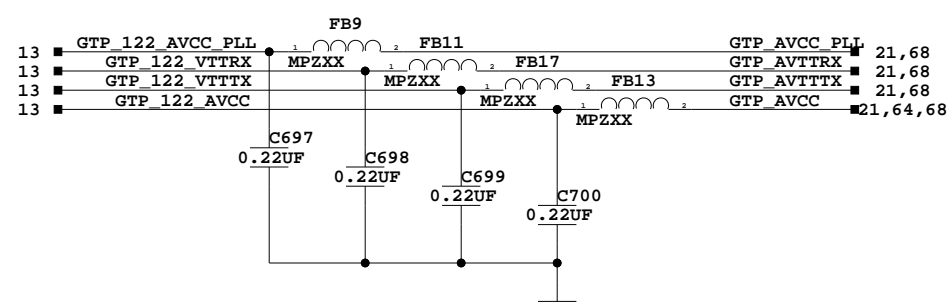
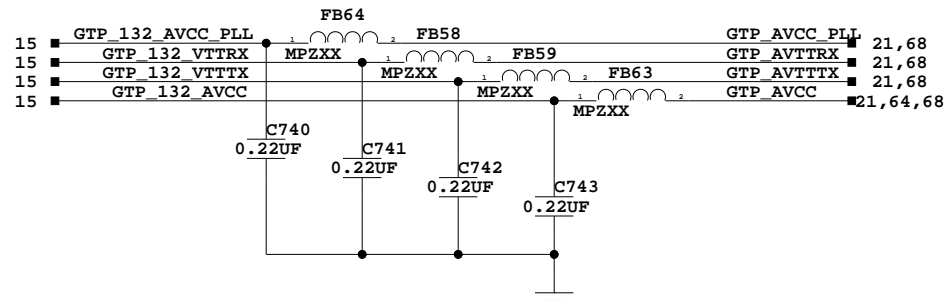
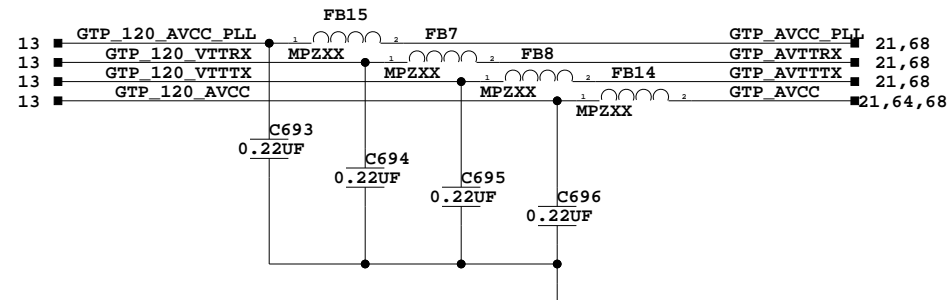
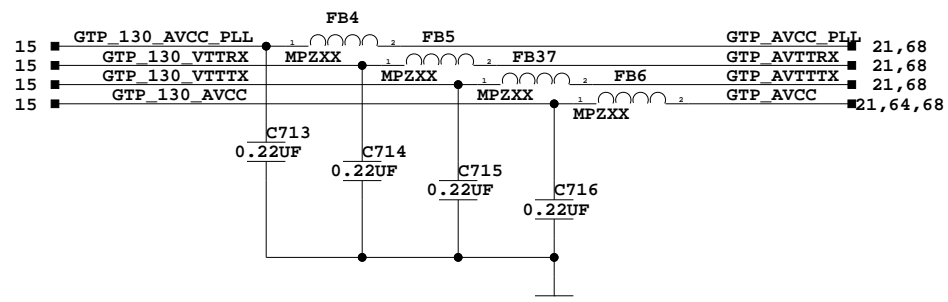
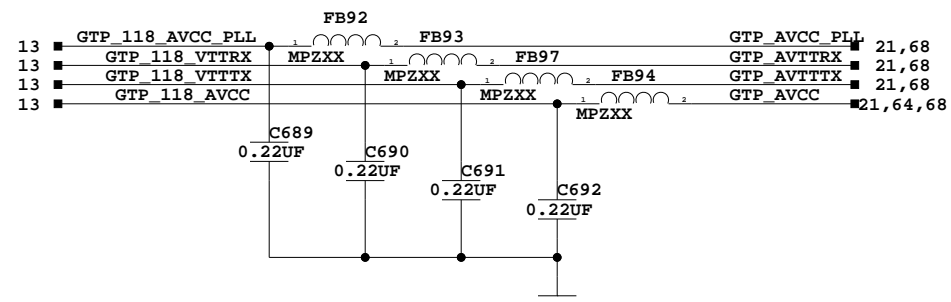
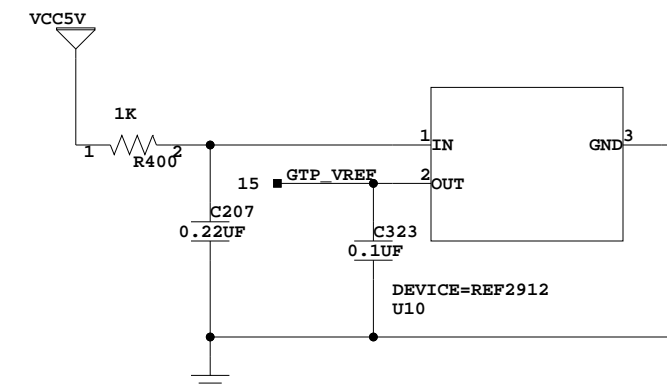
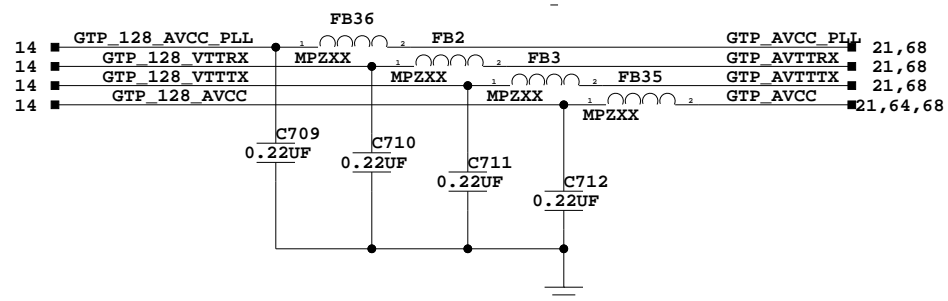
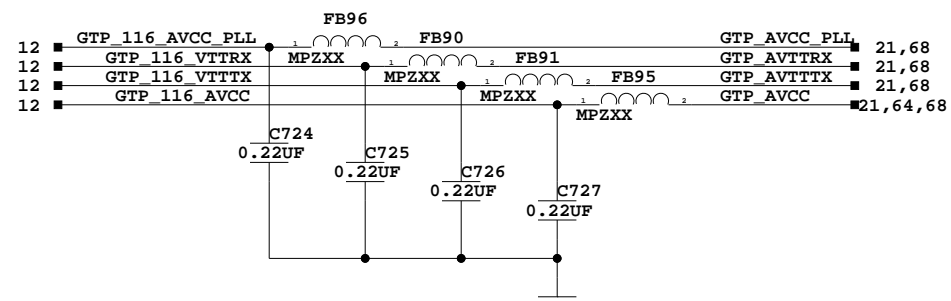
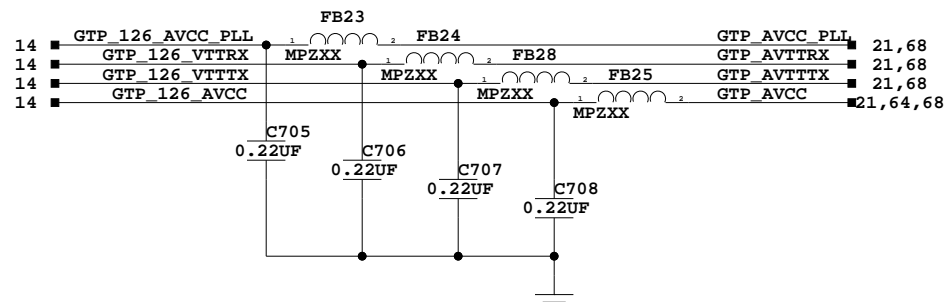
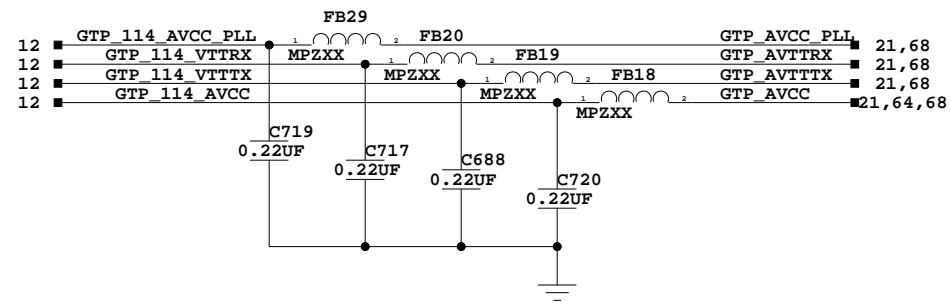
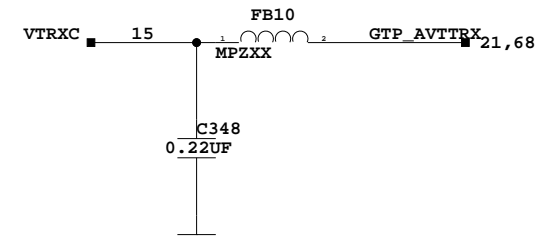
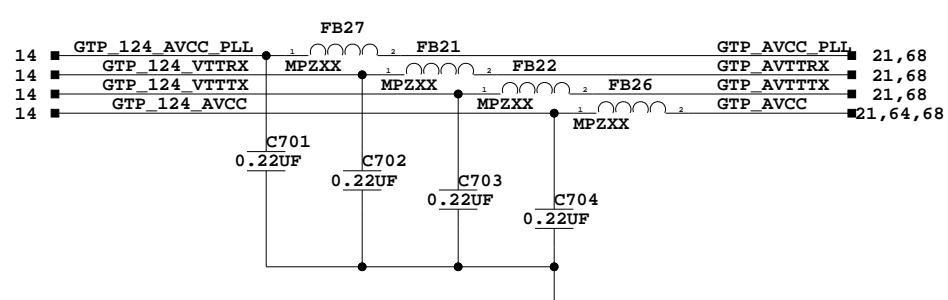
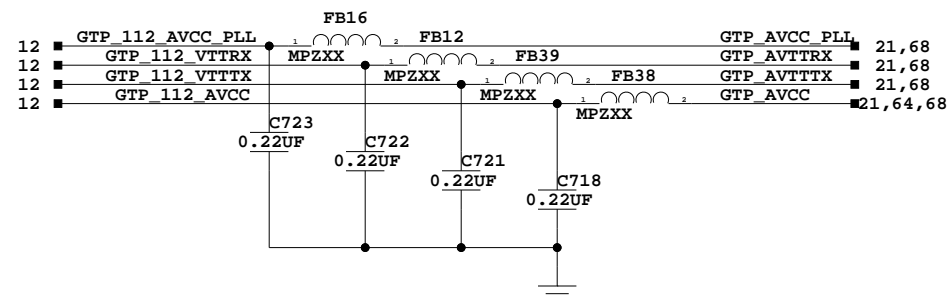
## FPGA DECOUPLING PAGE 2



SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 FPGA DECOUPLING PAGE 2

Date:	7-10-2008_10:19	Ver:	C
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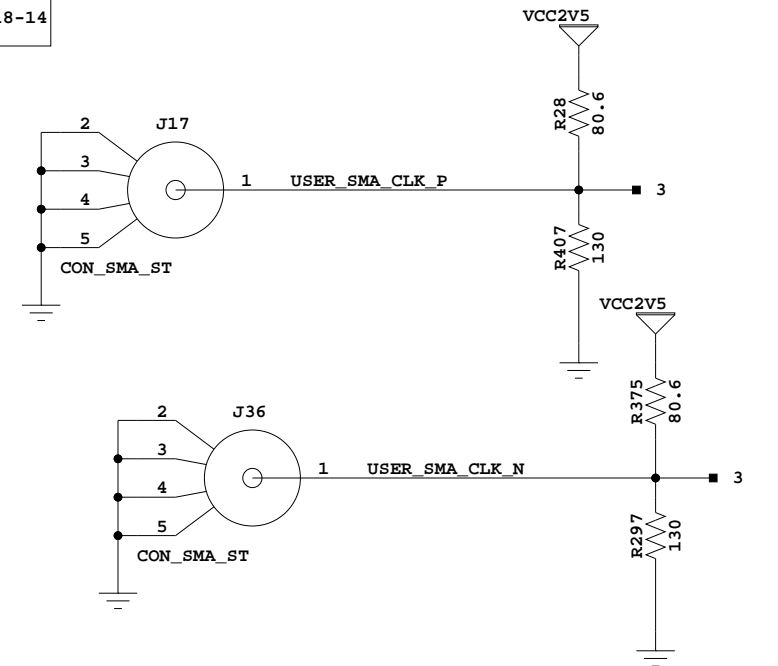
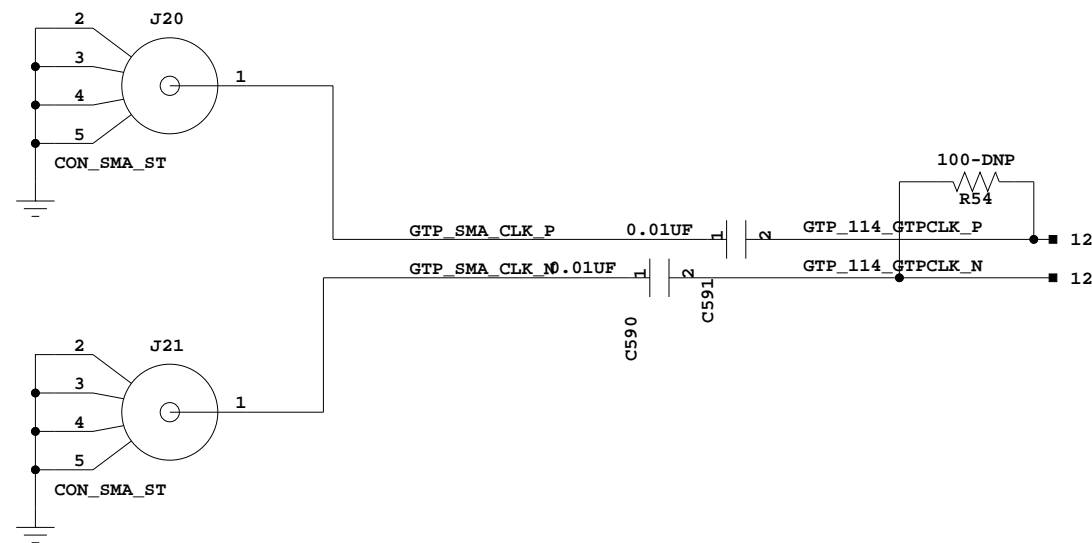
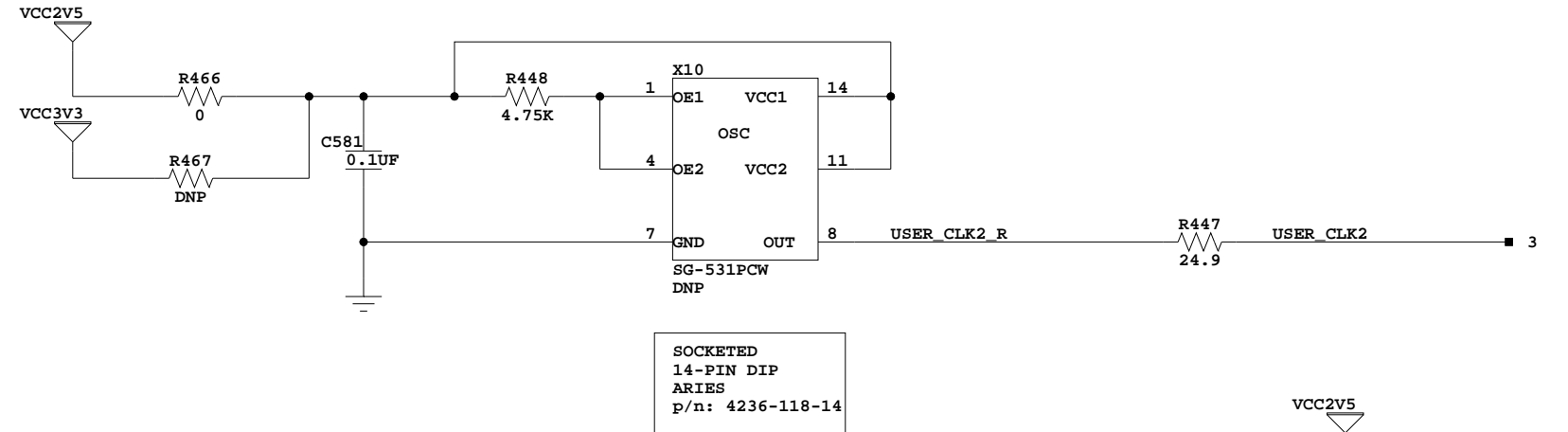
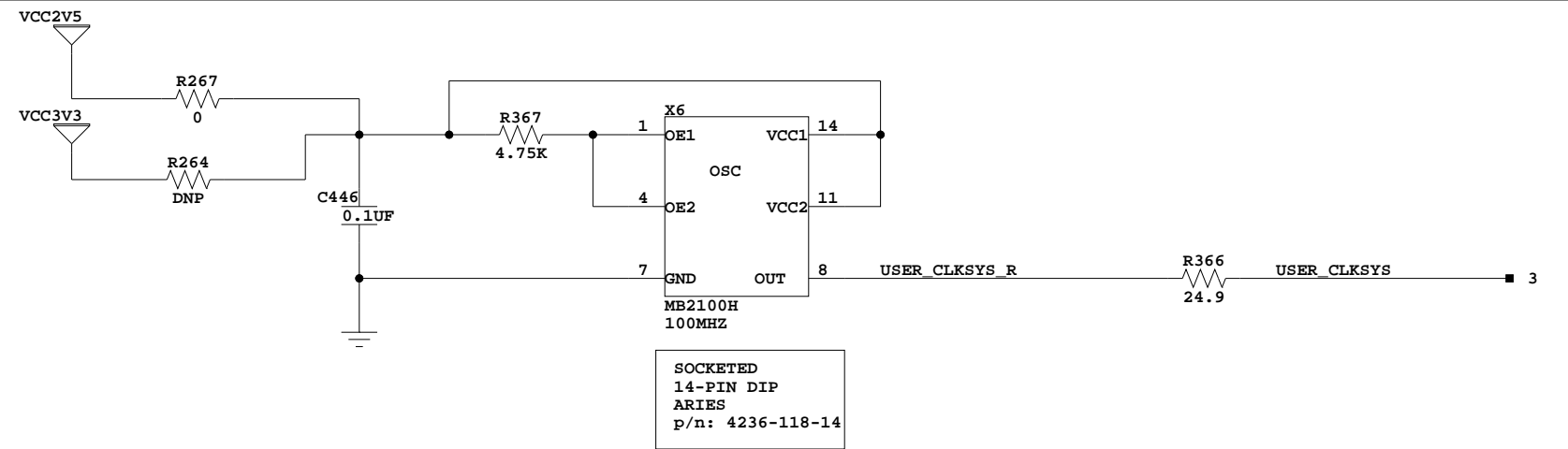
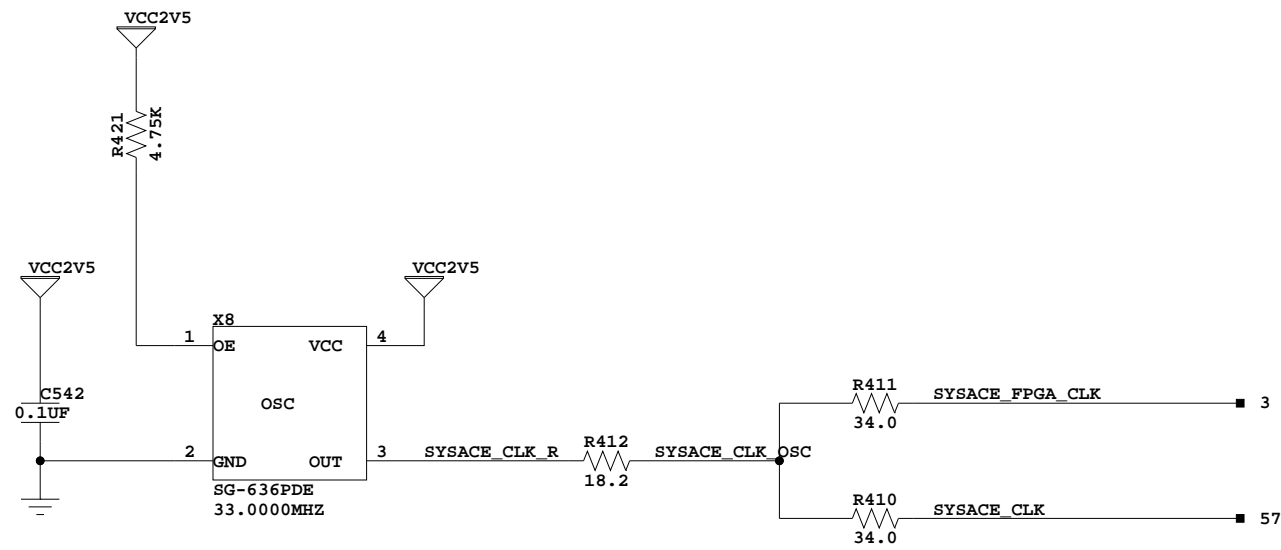
### GTP POWER FILTER



SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 GTP POWER FILTER

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	21 of 70	Drawn By	BF

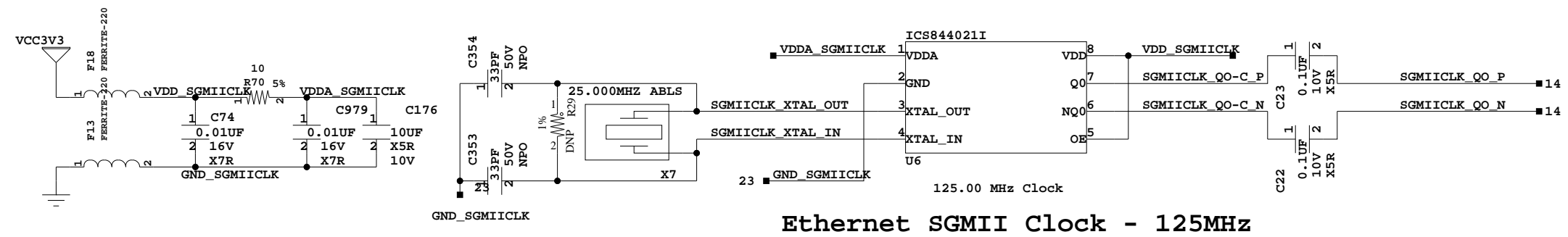
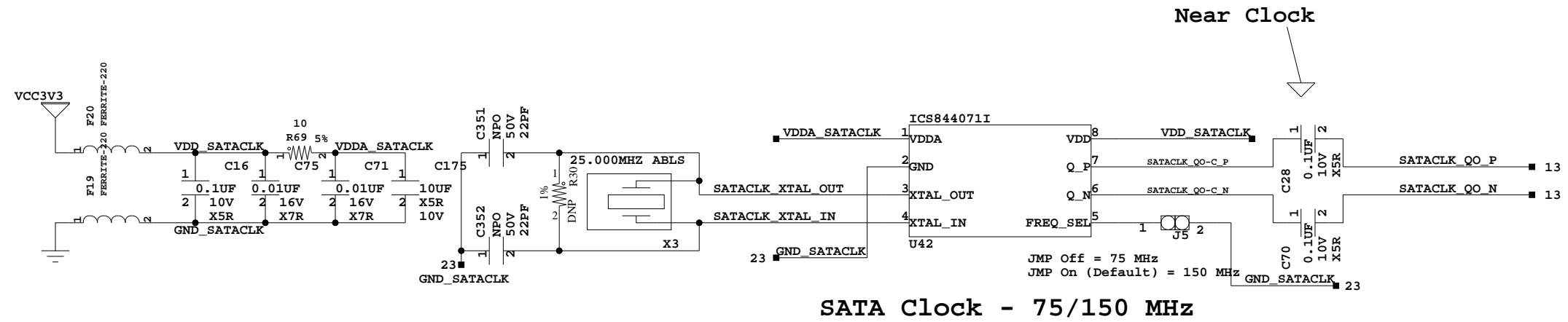


### CLOCKS: USER, MGT, SYSACE

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432

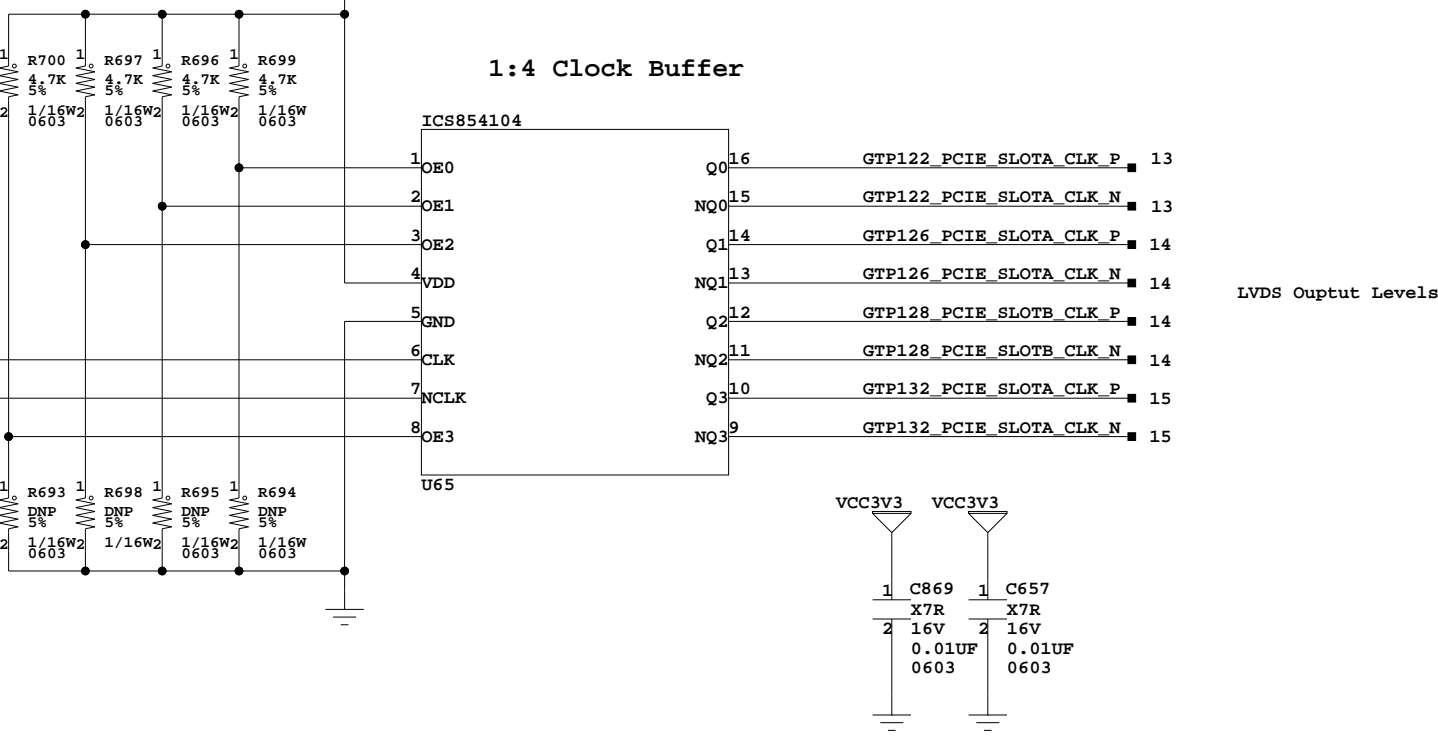
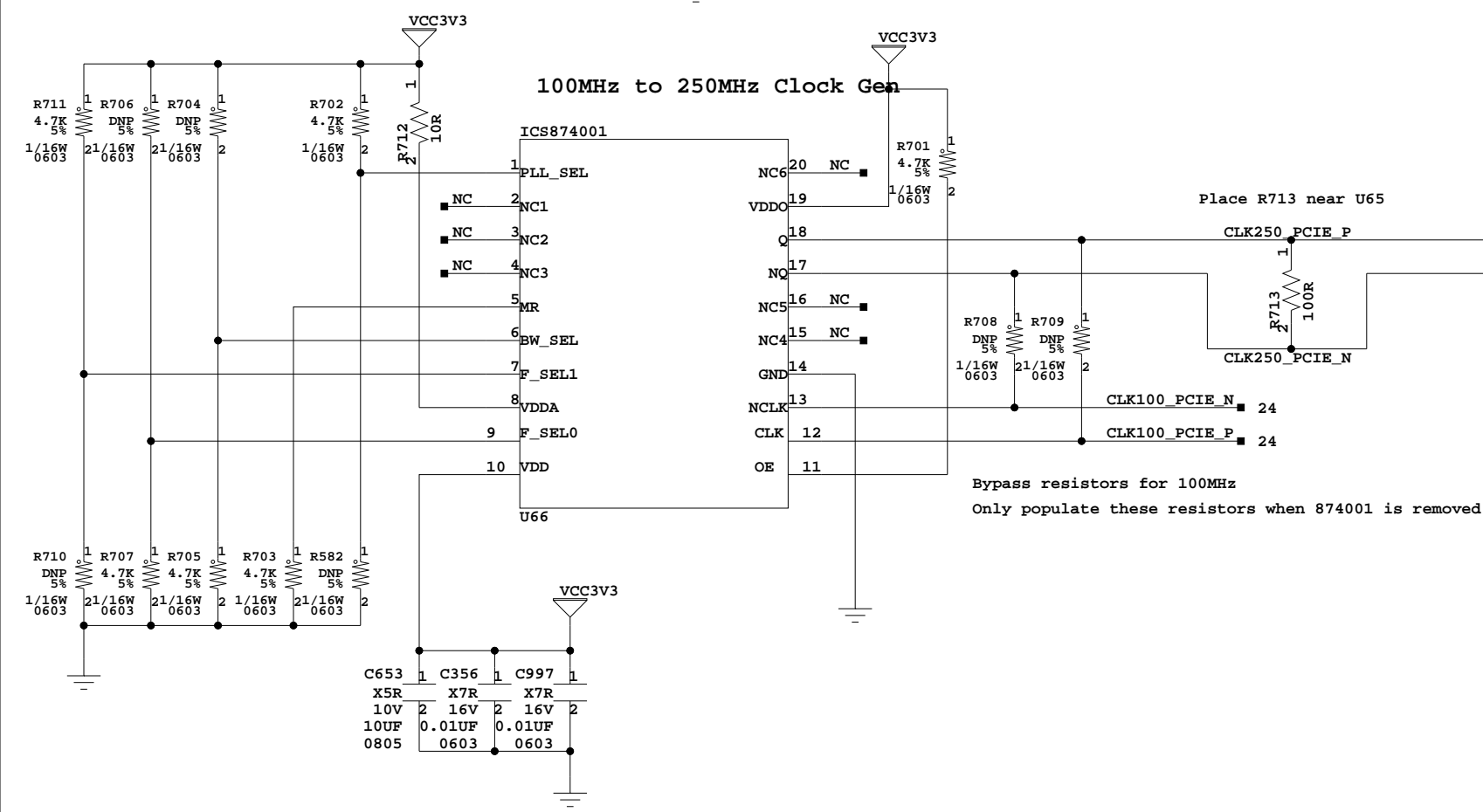
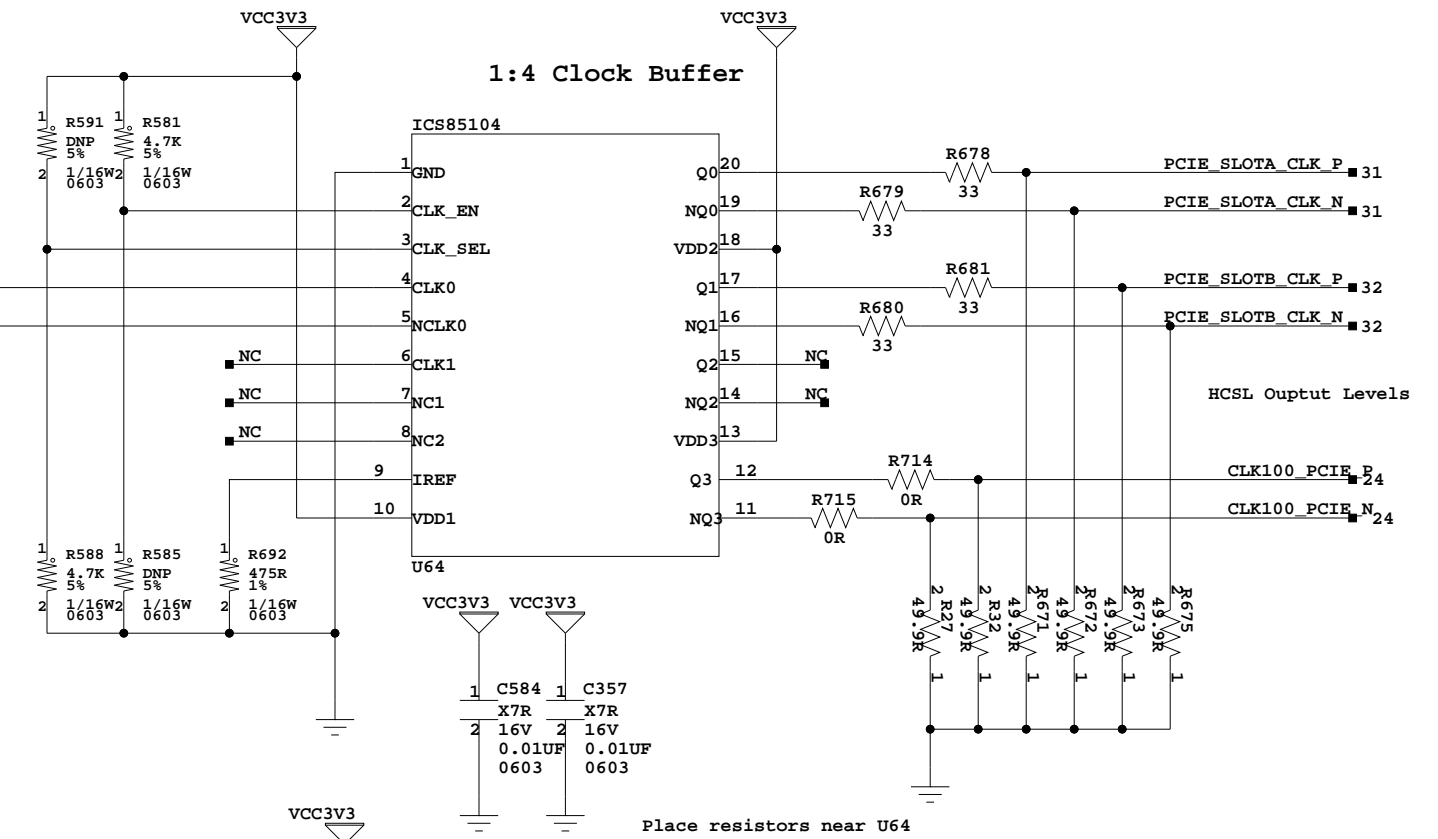
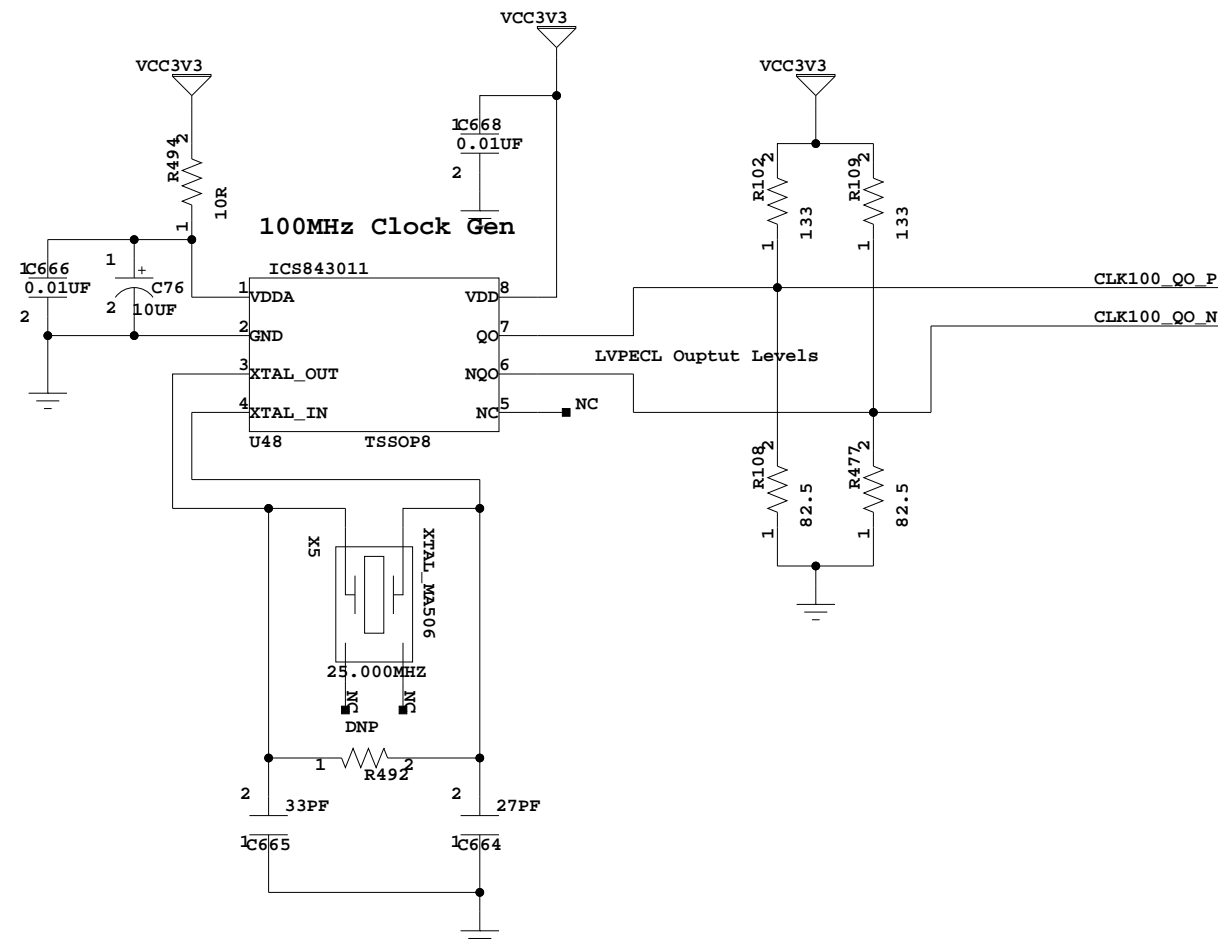
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
CLKS: USR, MGT, SYSACE

Date:	7-10-2008_10:19	Ver:	C
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### SATA, SGMII CLOCKS

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM SATA, SGMII CLOCKS		
Date:	7-10-2008_10:19	Ver: C
Sheet Size:	B	Rev: 01
Sheet	<b>23</b> of <b>70</b>	Drawn By BF



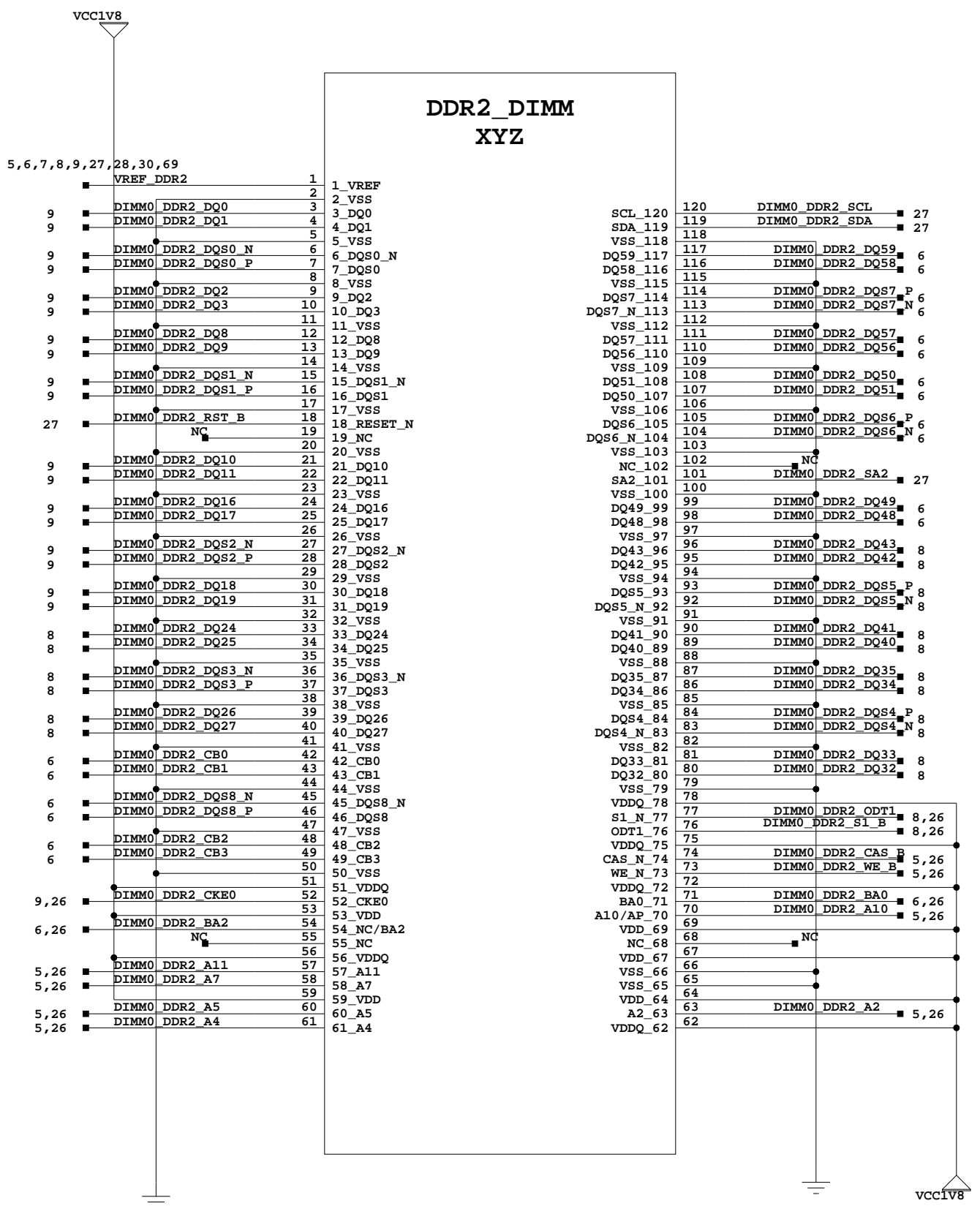
**PCie CLOCKS**

SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

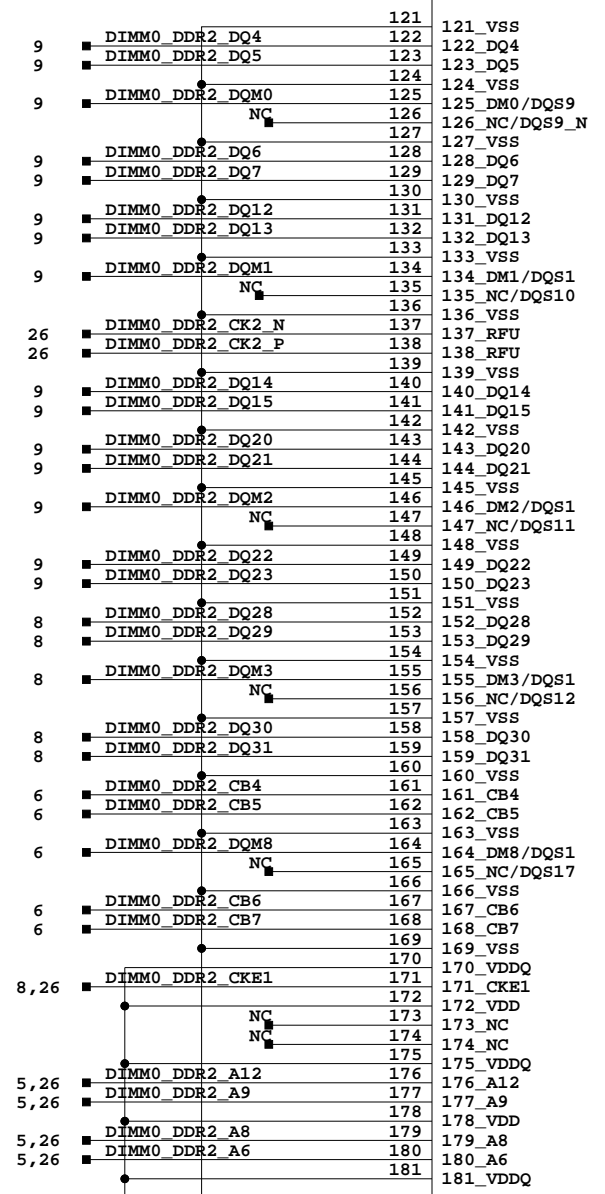
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
PCIE CLOCKS

Date: 7-10-2008\_10:19 Ver: C  
Sheet Size: B Rev: 01  
Sheet 24 of 70 Drawn By BF





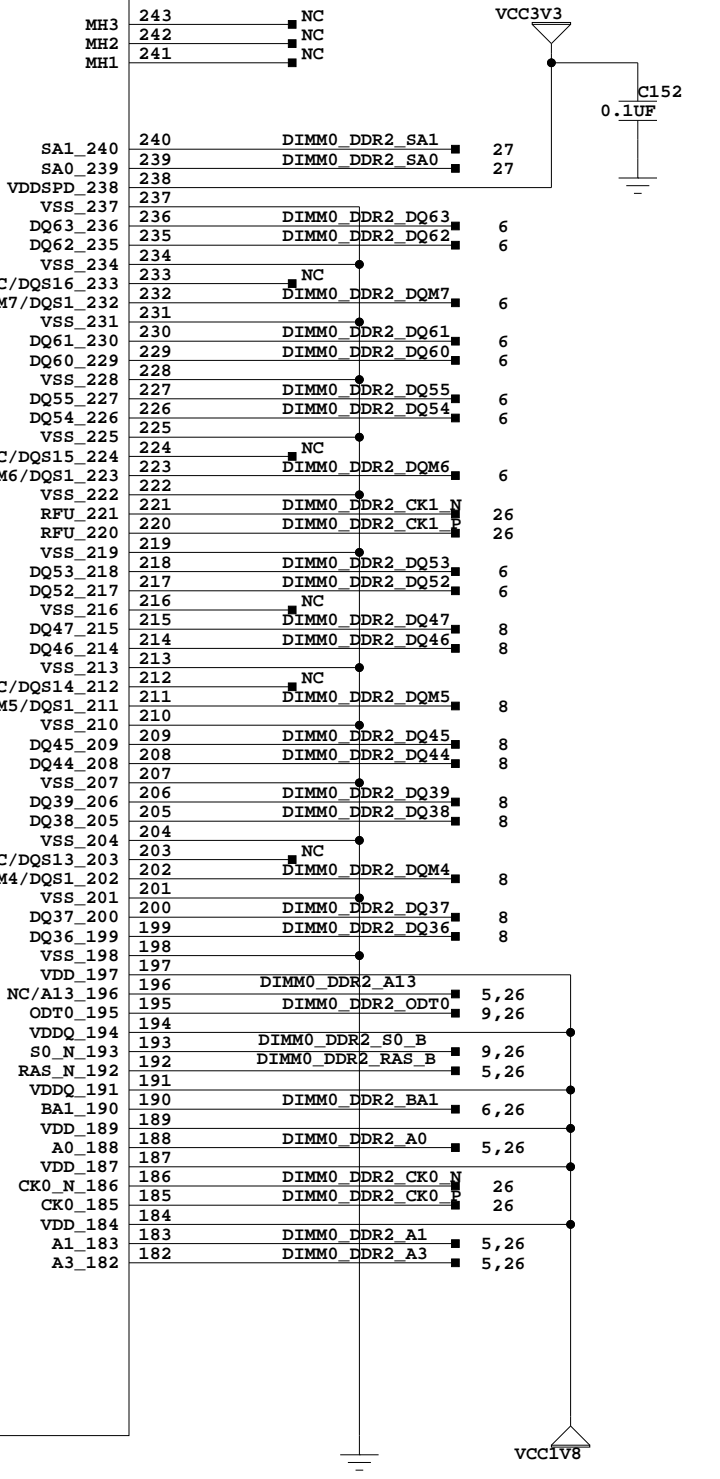
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 PKG\_TYPE=CON-240-DDRAM  
 PARTS=1  
 LEVEL=STD



P48  
 DEVICE=DDR2\_DIMM  
 PKG\_TYPE=CON-240-DDRAM  
 PARTS=1  
 LEVEL=STD

I2C ADDR = 0x8

### DDR2\_DIMM XYZ



### DDR2 DIMM0 CONNECTOR

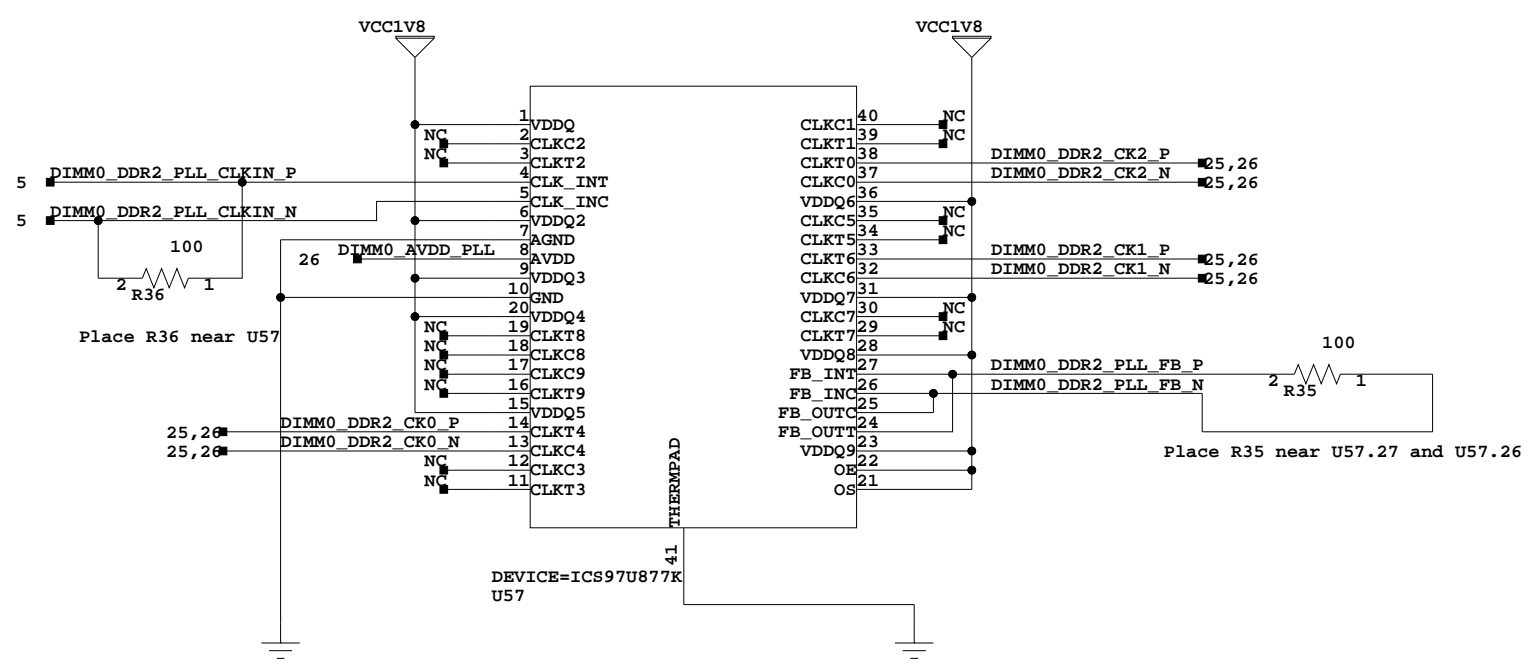
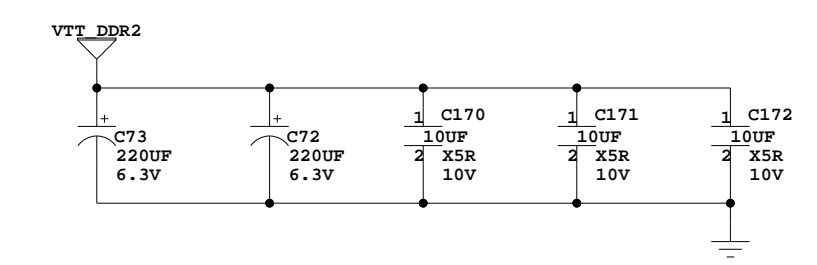
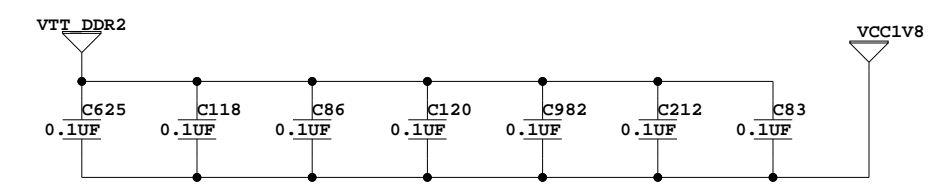
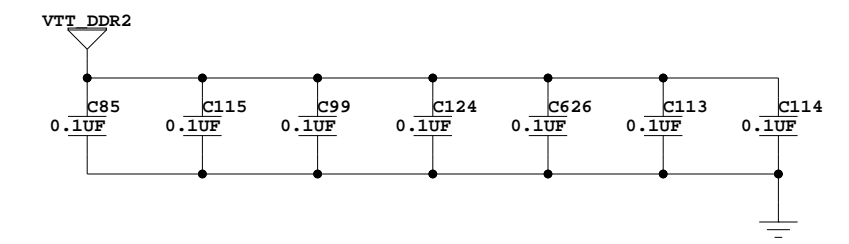
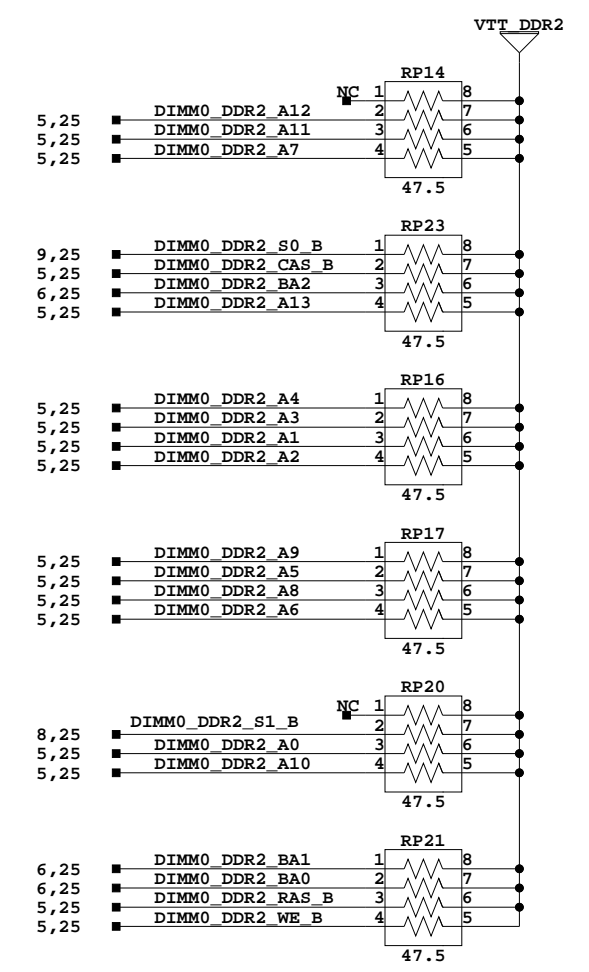
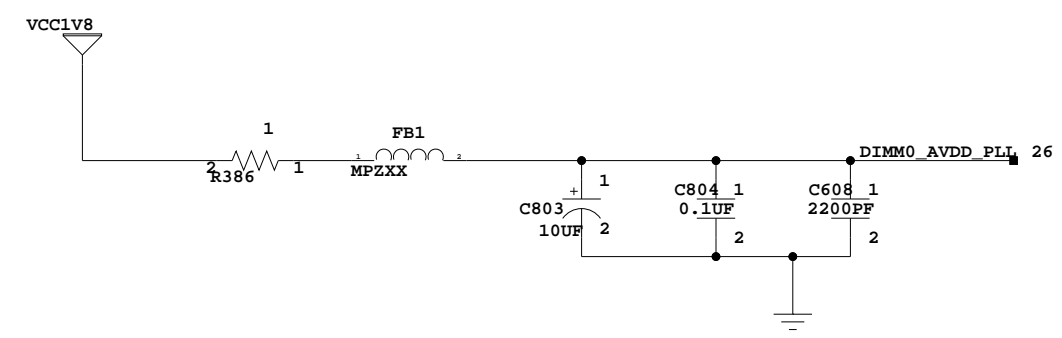


SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

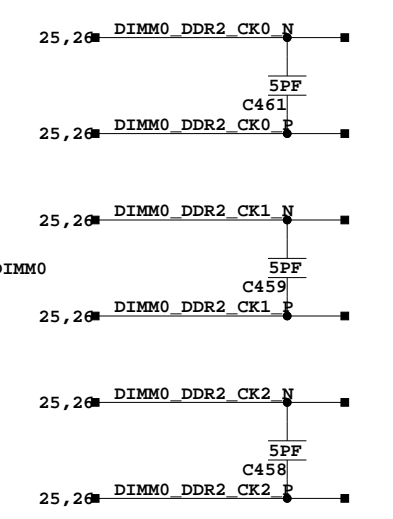
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 DDR2 DIMM0 CONNECTOR

Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	25 of 70	Drawn By	BF

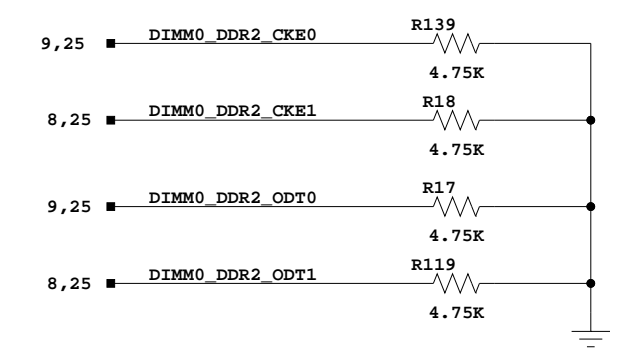
Since this is a source-sink power supply, split of decoupling capacitors between VTT-GND and VTT-VCC1V8



DIMM0\_DDR2\_PLL\_FB\* to be length matched to DIMM0\_DDR2\_CLKIN\*



Place these 5pf caps near DDR2 DIMM0



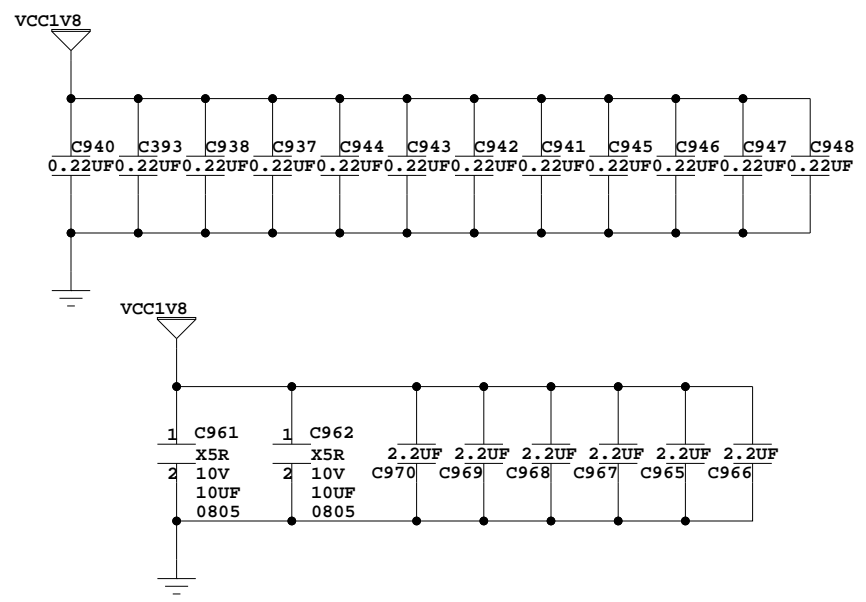
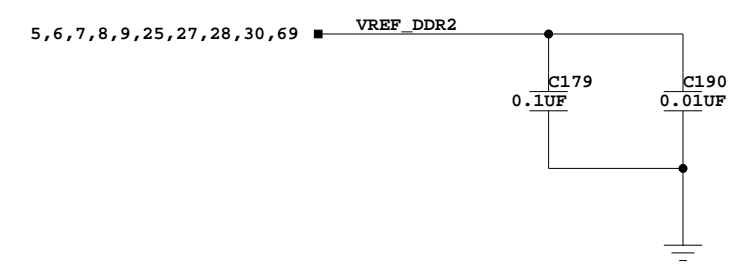
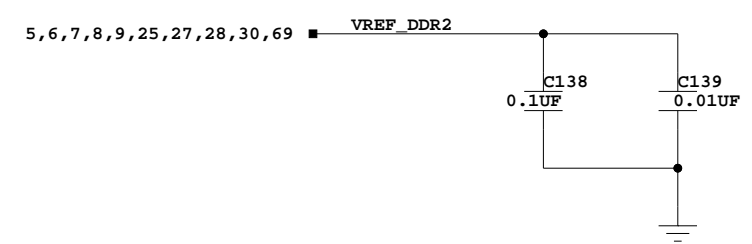
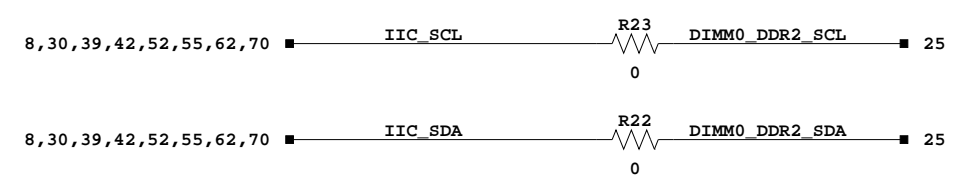
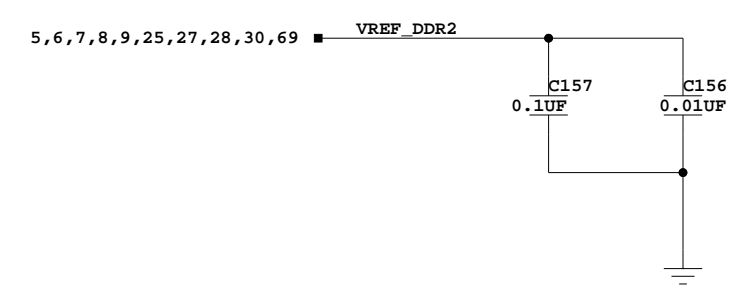
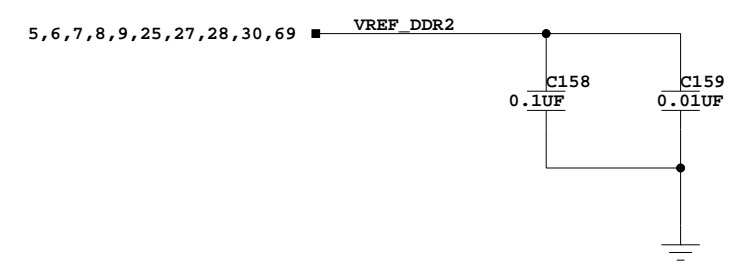
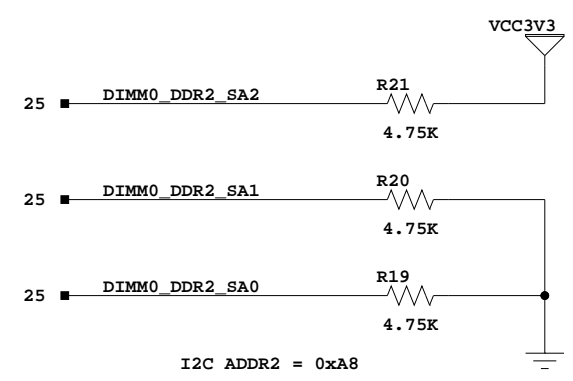
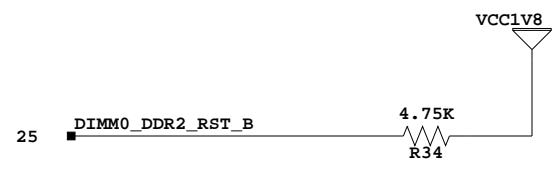
### DIMM0 DDR2 SSTL-2 TERMINATION



SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
DIMM0 DDR2 SSTL-2 TERMINATION

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	26 of 70	Drawn By	BF

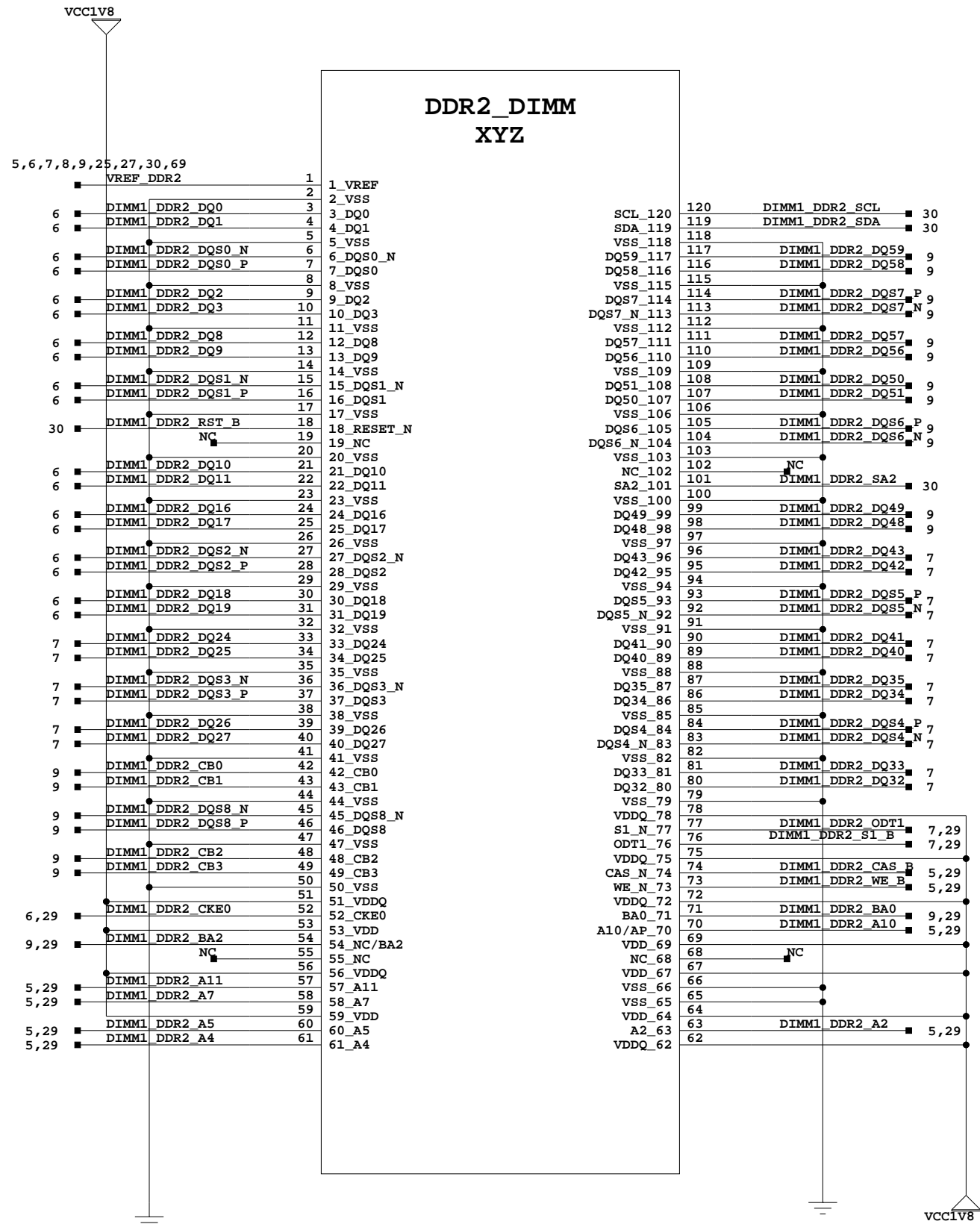


### DIMM0 DDR2 DECOUPLING



SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM DIMM0 DDR2 DECOUPLING	
Date: 7-10-2008_10:19	Ver: C
Sheet Size: B	Rev: 01
Sheet 27 of 70	Drawn By BF

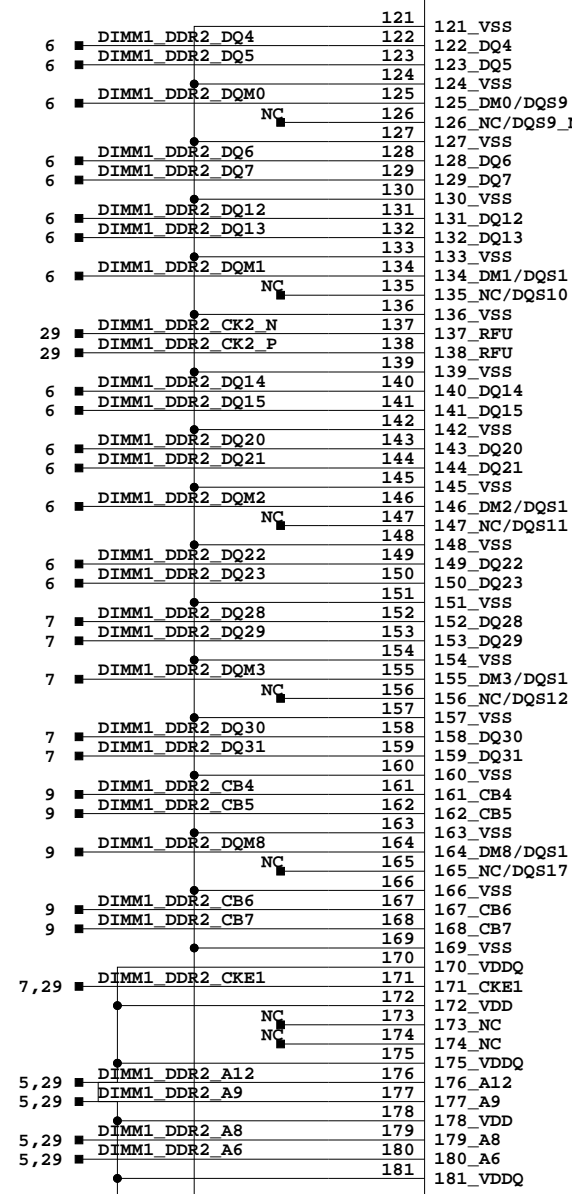


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 PKG\_TYPE=CON-240-DDRAM  
 PARTS=1  
 LEVEL=STD

### DDR2\_DIMM XYZ

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119	DIMM1_DDR2_SDA	30
118	VSS_118	
117	DIMM1_DDR2_DQ59	9
116	DIMM1_DDR2_DQ58	9
115	VSS_115	
114	DIMM1_DDR2_DQ57	9
113	DIMM1_DDR2_DQ57_N	9
112	VSS_112	
111	DIMM1_DDR2_DQ57	9
110	DIMM1_DDR2_DQ56	9
109	VSS_109	
108	DIMM1_DDR2_DQ50	9
107	DIMM1_DDR2_DQ51	9
106	VSS_106	
105	DIMM1_DDR2_DQ56	9
104	DIMM1_DDR2_DQ56_N	9
103	VSS_103	
102	NC_102	
101	DIMM1_DDR2_SA2	30
100	VSS_100	
99	DIMM1_DDR2_DQ49	9
98	DIMM1_DDR2_DQ48	9
97	VSS_97	
96	DIMM1_DDR2_DQ43	7
95	DIMM1_DDR2_DQ42	7
94	VSS_94	
93	DIMM1_DDR2_DQ85	7
92	DIMM1_DDR2_DQ85_N	7
91	VSS_91	
90	DIMM1_DDR2_DQ41	7
89	DIMM1_DDR2_DQ40	7
88	VSS_88	
87	DIMM1_DDR2_DQ35	7
86	DIMM1_DDR2_DQ34	7
85	VSS_85	
84	DIMM1_DDR2_DQS4	7
83	DIMM1_DDR2_DQS4_N	7
82	VSS_82	
81	DIMM1_DDR2_DQ33	7
80	DIMM1_DDR2_DQ32	7
79	VSS_79	
78	VDDQ_78	
77	DIMM1_DDR2_ODT1	7,29
76	DIMM1_DDR2_S1_B	7,29
75	VDDQ_75	
74	DIMM1_DDR2_CAS_B	5,29
73	DIMM1_DDR2_WE_B	5,29
72	VDDQ_72	
71	DIMM1_DDR2_BA0	9,29
70	DIMM1_DDR2_A10	5,29
69	VDD_69	
68	NC_68	
67	VDD_67	
66	VSS_66	
65	VSS_65	
64	VDD_64	
63	DIMM1_DDR2_A2	5,29
62	VDDQ_62	

vcc1v8



### DDR2\_DIMM XYZ

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 PKG\_TYPE=CON-240-DDRAM  
 PARTS=1  
 LEVEL=STD

I2C ADDR = 0xA6

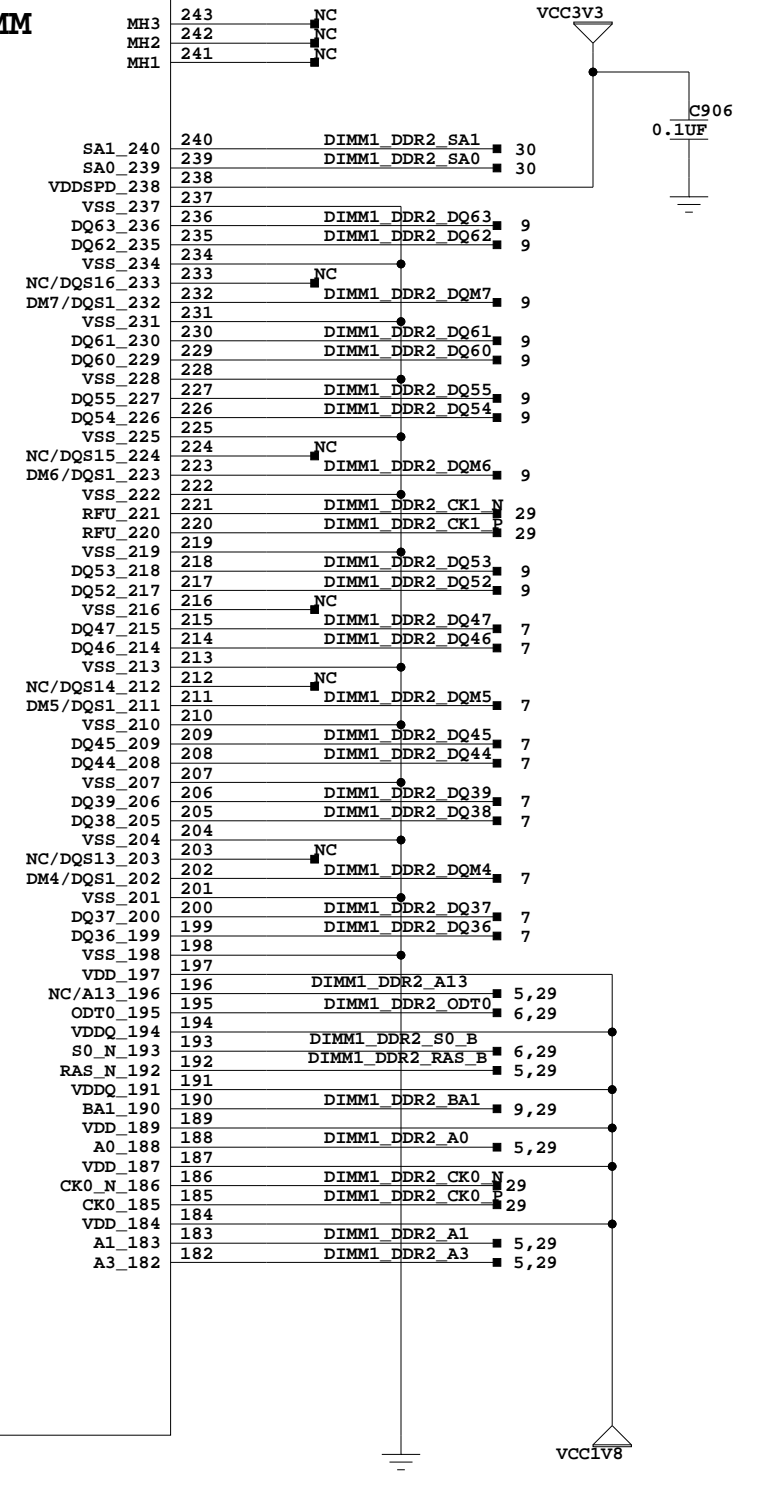
vcc1v8

### DDR2 DIMM1 CONNECTOR

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 DDR2 DIMM2 CONNECTOR

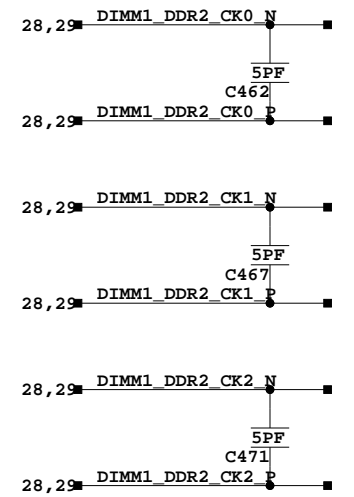
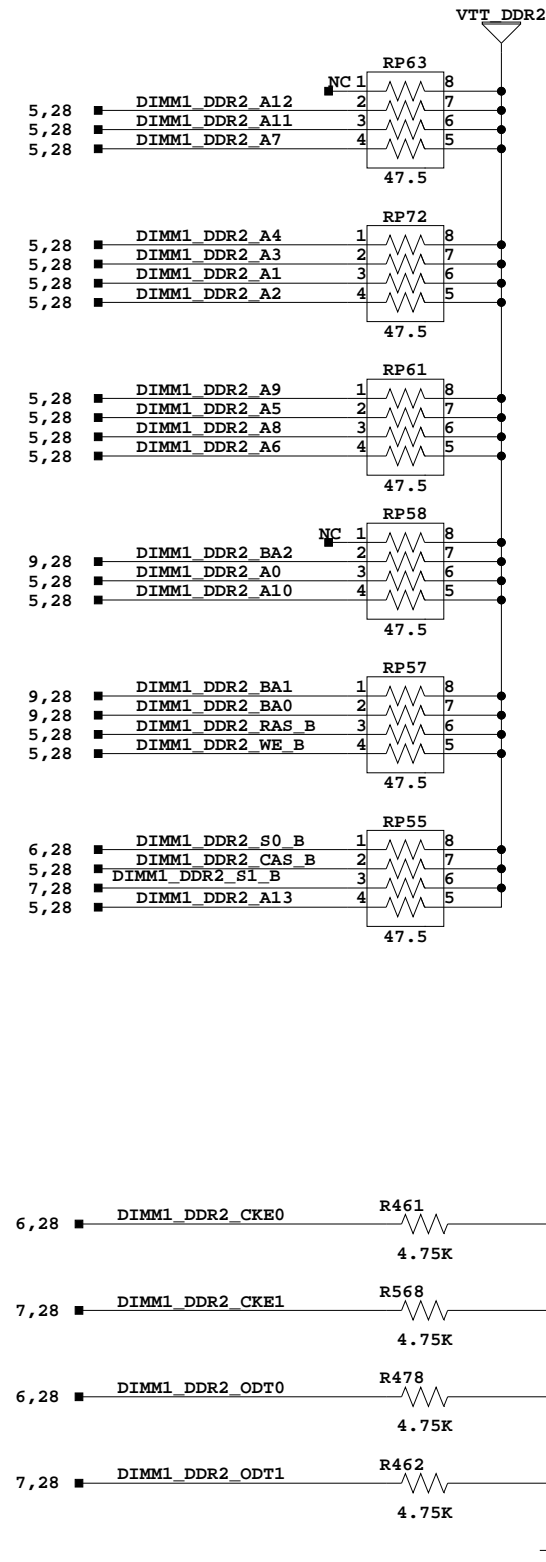
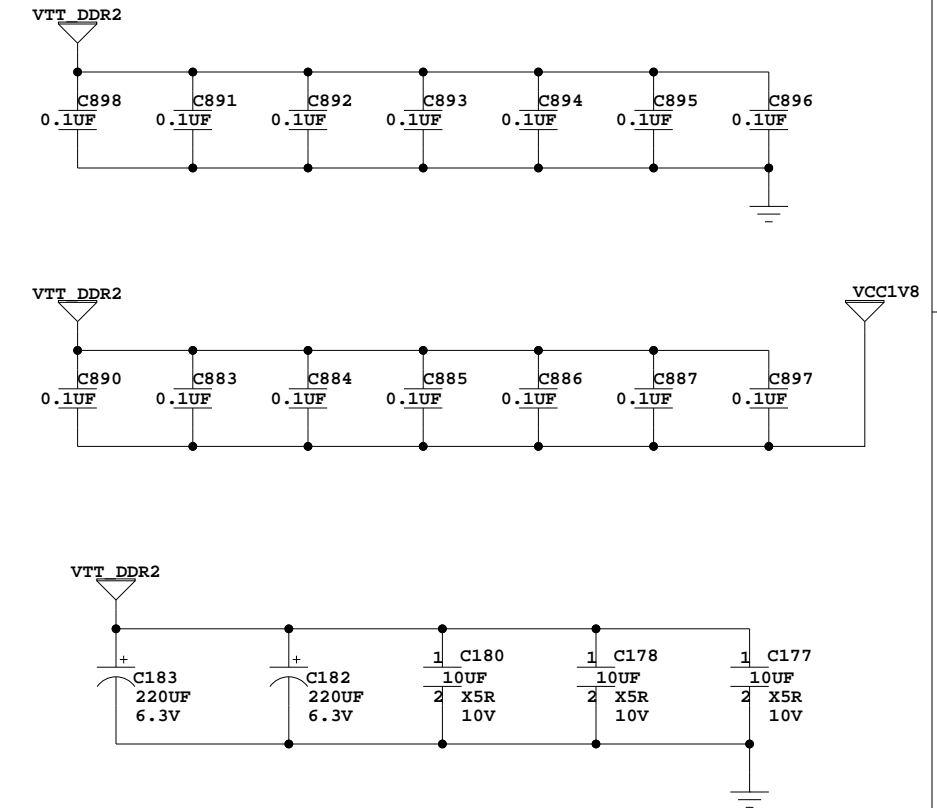
Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
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vcc1v8

C906  
0.1UF

Since this is a source-sink power supply, split of decoupling capacitors between VTT-GND and VTT-VCC1V8



Place these 5pf caps near DDR2 DIMM1

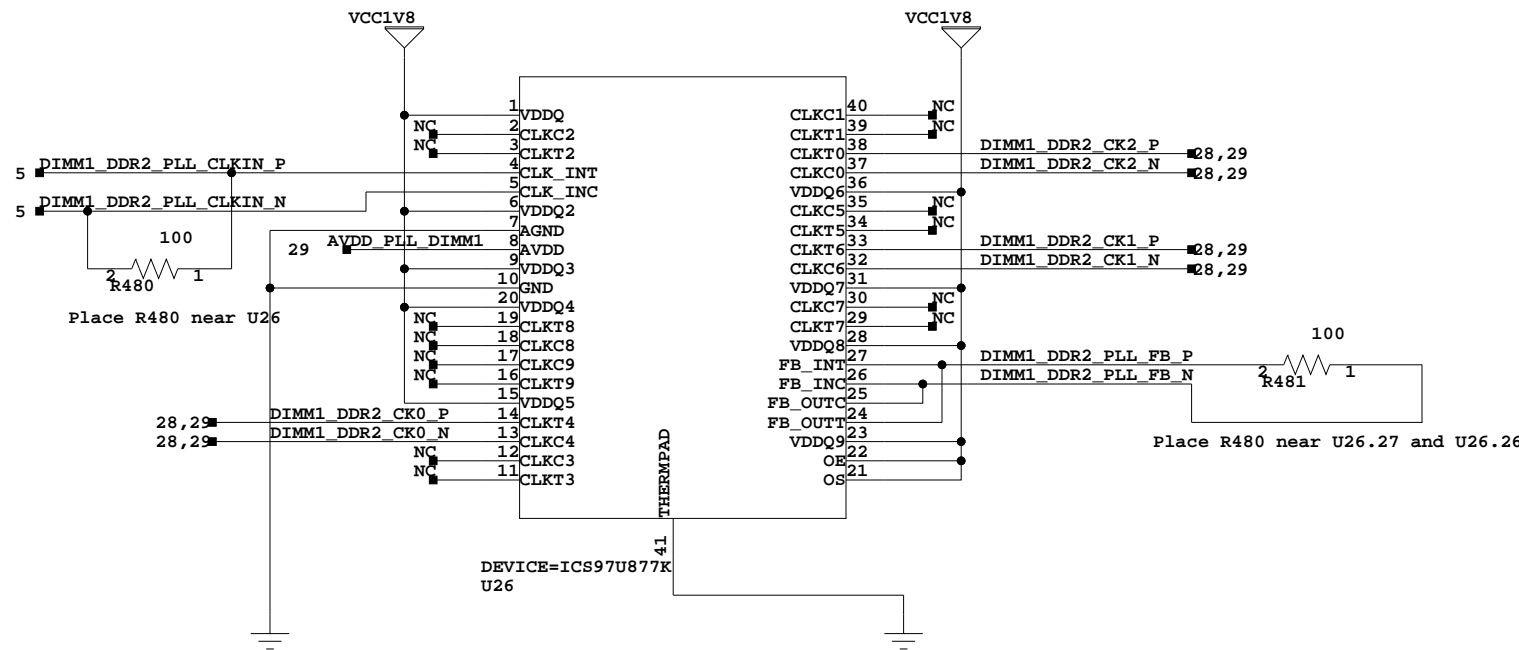
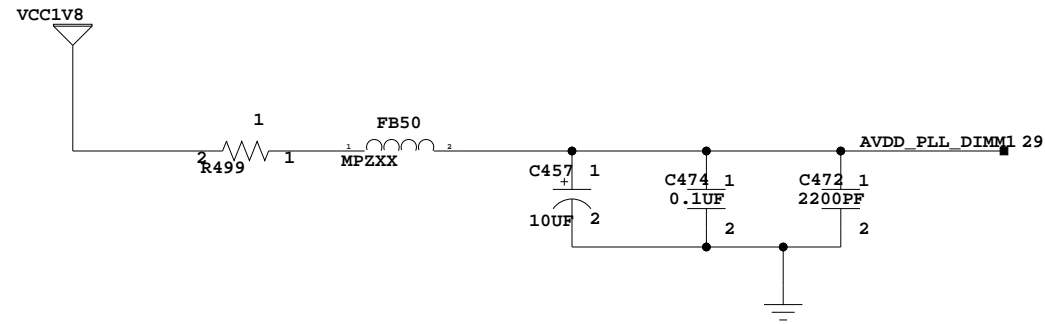
### DIMM1 DDR2 SSTL-2 TERMINATION



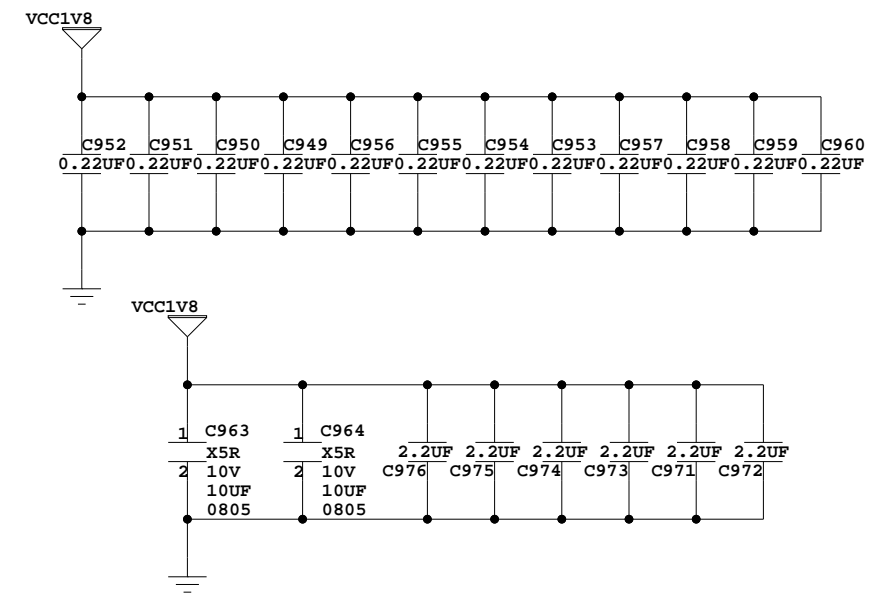
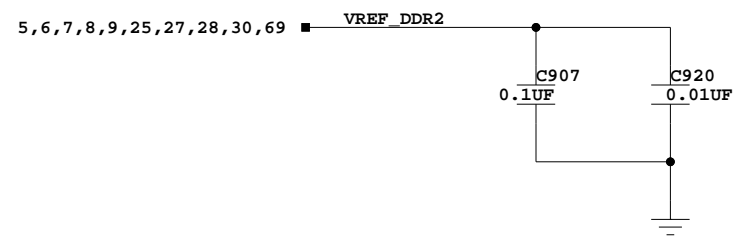
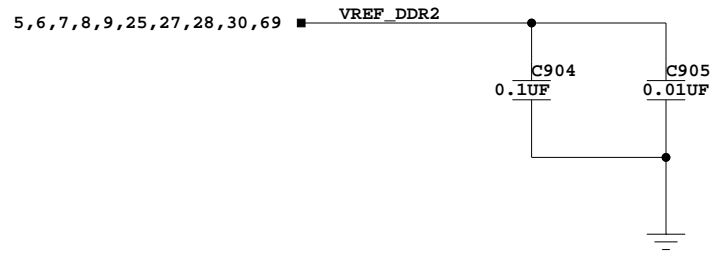
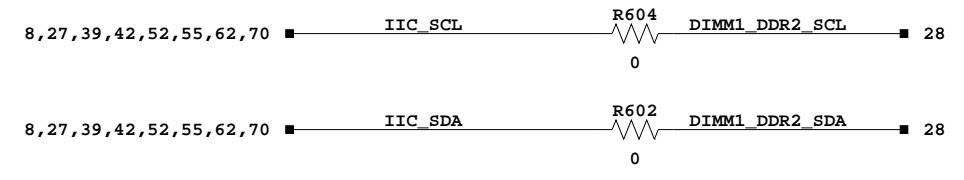
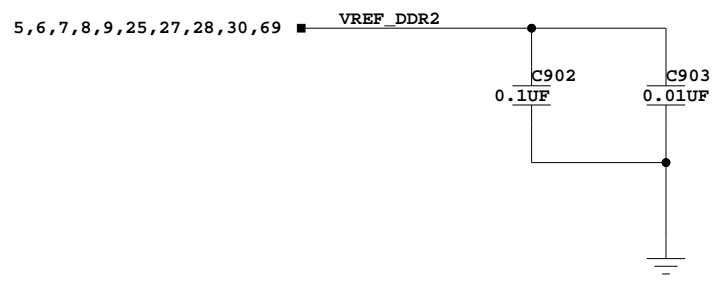
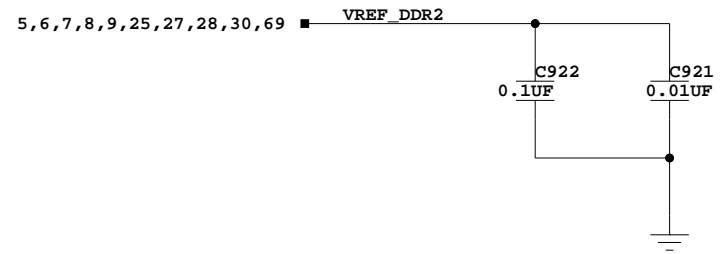
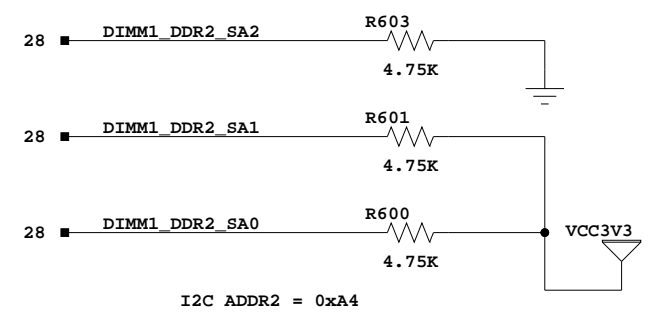
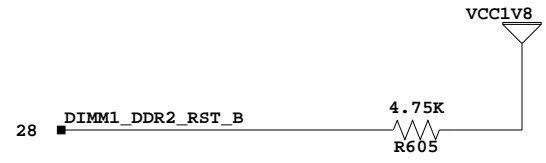
SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
DIMM1 DDR2 SSTL-2 TERMINATION

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
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DIMM1\_DDR2\_PLL\_FB\* to be length matched to DIMM0\_DDR2\_CLKIN\_\*



### DIMM1 DDR2 DECOUPLING

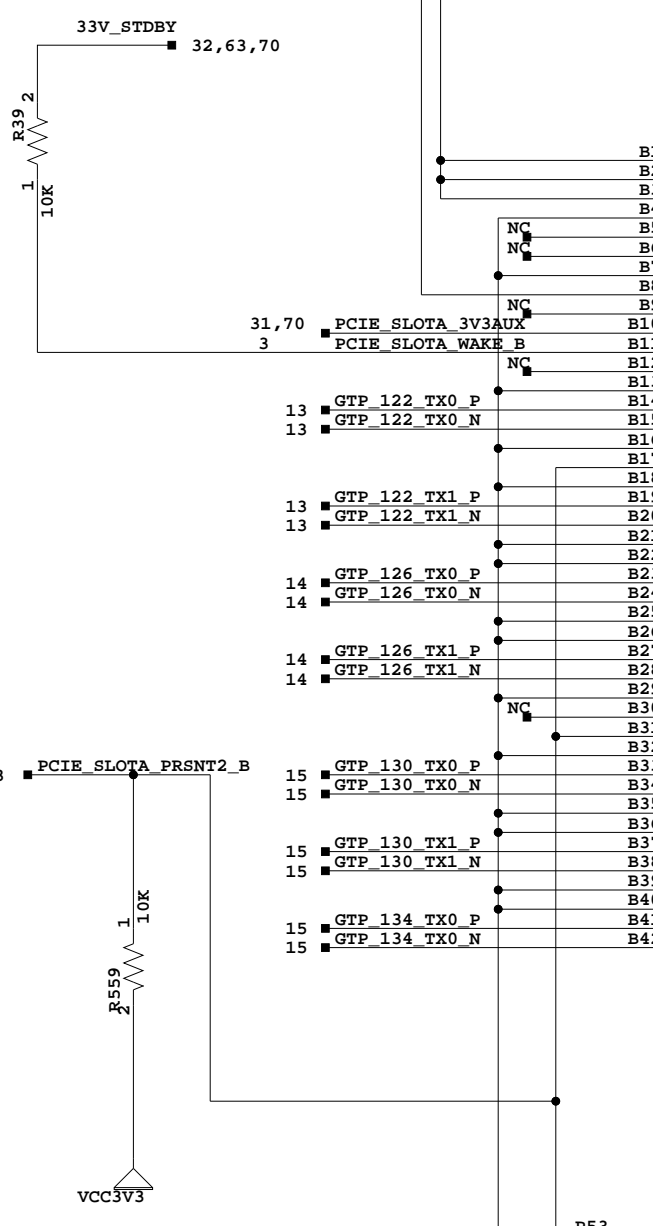


SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 DIMM1 DDR2 DECOUPLING

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	30 of 70	Drawn By	BF

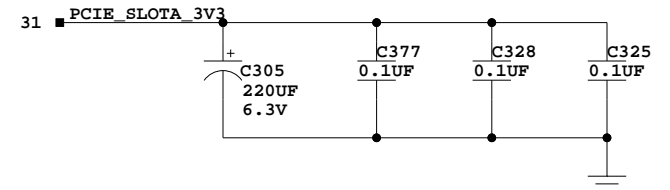
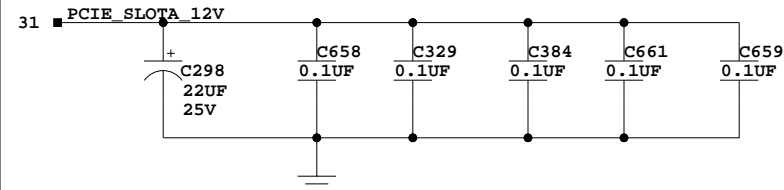
31 PCIE\_SLOTA\_12V  
 31 PCIE\_SLOTA\_3V3



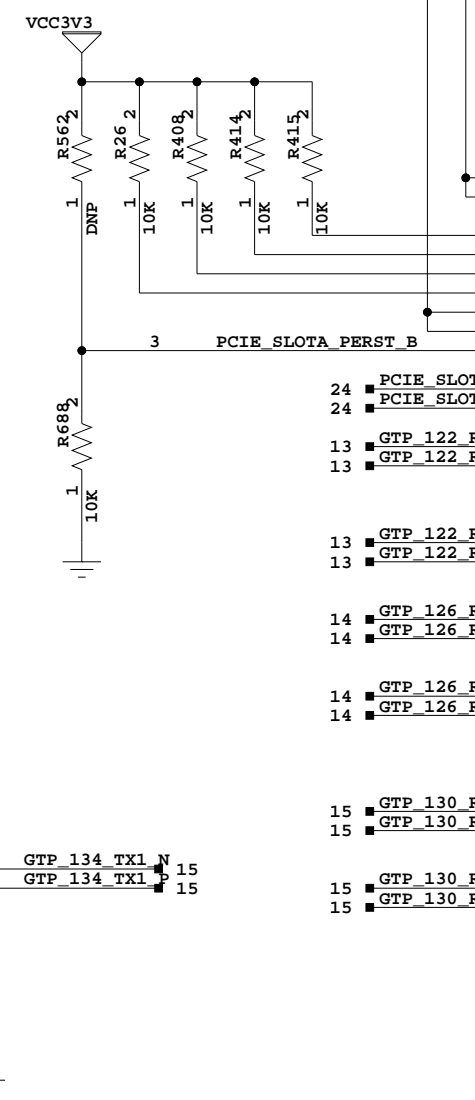
**PCI\_E  
XYZ**

- B1 1B\_12v
- B2 2B\_12v
- B3 3B\_12v
- B4 4B\_GND
- B5 5B\_SMCLK
- B6 6B\_SMDAT
- B7 7B\_GND
- B8 8B\_3v3
- B9 9B\_TRST\_N
- B10 10B\_3v3aux
- B11 11B\_WAKE\_N
- B12 12B\_RSVD
- B13 13B\_GND
- B14 14B\_HSOp0
- B15 15B\_HSON0
- B16 16B\_GND
- B17 17B\_PRSNT2\_N
- B18 18B\_GND
- B19 19B\_HSOp1
- B20 20B\_HSON1
- B21 21B\_GND
- B22 22B\_GND
- B23 23B\_HSOp2
- B24 24B\_HSON2
- B25 25B\_GND
- B26 26B\_GND
- B27 27B\_HSOp3
- B28 28B\_HSON3
- B29 29B\_GND
- B30 30B\_RSVD
- B31 31B\_PRSNT2\_N
- B32 32B\_GND
- B33 33B\_HSOp4
- B34 34B\_HSON4
- B35 35B\_GND
- B36 36B\_GND
- B37 37B\_HSOp5
- B38 38B\_HSON5
- B39 39B\_GND
- B40 40B\_GND
- B41 41B\_HSOp6
- B42 42B\_HSON6

P53  
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 PKG\_TYPE=CON\_PCI-E\_164  
 PARTS=1  
 LEVEL=STD



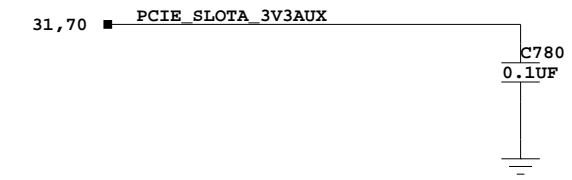
31 PCIE\_SLOTA\_12V  
 31 PCIE\_SLOTA\_3V3



**PCI\_E  
XYZ**

- A1 1A\_PRSNT1\_N
- A2 2A\_12v
- A3 3A\_12v
- A4 4A\_GND
- A5 5A\_TCK
- A6 6A\_TDI
- A7 7A\_TDO
- A8 8A\_TMS
- A9 9A\_3v3
- A10 10A\_3v3
- A11 11A\_PERST\_N
- A12 12A\_GND
- A13 13A\_REFCLKP
- A14 14A\_REFCLKN
- A15 15A\_GND
- A16 16A\_HSIp0
- A17 17A\_HSIp1
- A18 18A\_GND
- A19 19A\_RSVD
- A20 20A\_GND
- A21 21A\_HSIp1
- A22 22A\_HSIp1
- A23 23A\_GND
- A24 24A\_GND
- A25 25A\_HSIp2
- A26 26A\_HSIp2
- A27 27A\_GND
- A28 28A\_GND
- A29 29A\_HSIp3
- A30 30A\_HSIp3
- A31 31A\_GND
- A32 32A\_RSVD
- A33 33A\_RSVD
- A34 34A\_GND
- A35 35A\_HSIp4
- A36 36A\_HSIp4
- A37 37A\_GND
- A38 38A\_GND
- A39 39A\_HSIp5
- A40 40A\_HSIp5
- A41 41A\_GND
- A42 42A\_GND

P53  
 DEVICE=PCI\_E  
 PKG\_TYPE=CON\_PCI-E\_164  
 PARTS=1  
 LEVEL=STD



- A82 GND\_82A
- A81 HSIp15\_81A
- A80 HSIp15\_80A
- A79 GND\_79A
- A78 7A\_TDO
- A77 HSIp14\_77A
- A76 HSIp14\_76A
- A75 GND\_75A
- A74 GND\_74A
- A73 HSIp13\_73A
- A72 HSIp13\_72A
- A71 GND\_71A
- A70 GND\_70A
- A69 HSIp12\_69A
- A68 HSIp12\_68A
- A67 GND\_67A
- A66 GND\_66A
- A65 HSIp11\_65A
- A64 HSIp11\_64A
- A63 GND\_63A
- A62 GND\_62A
- A61 HSIp10\_61A
- A60 HSIp10\_60A
- A59 GND\_59A
- A58 GND\_58A
- A57 HSIp9\_57A
- A56 HSIp9\_56A
- A55 GND\_55A
- A54 GND\_54A
- A53 HSIp8\_53A
- A52 HSIp8\_52A
- A51 GND\_51A
- A50 RSVD\_50A
- A49 GND\_49A
- A48 HSIp7\_48A
- A47 HSIp7\_47A
- A46 GND\_46A
- A45 GND\_45A
- A44 HSIp6\_44A
- A43 HSIp6\_43A

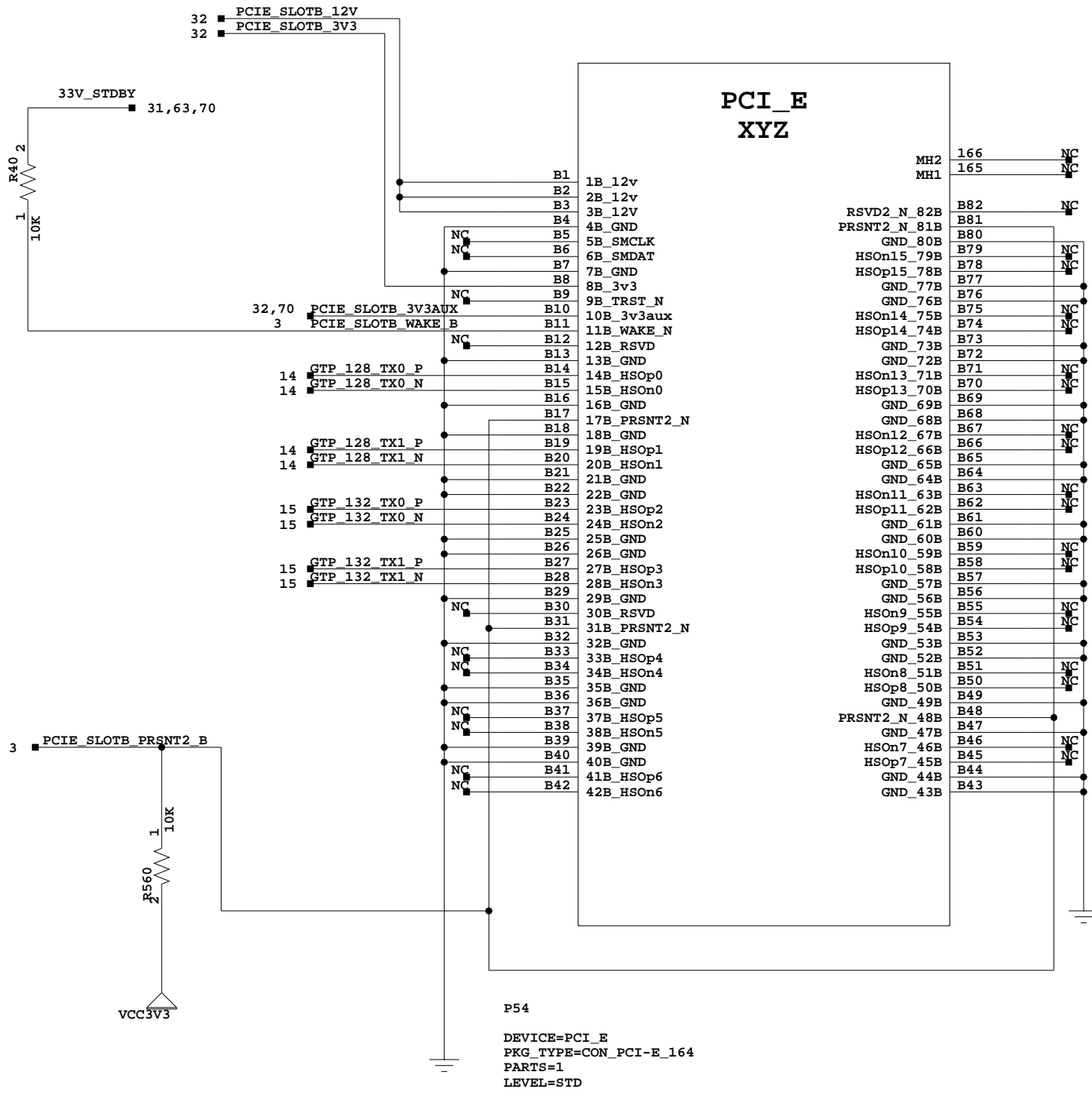
**PCI-E SLOT A**



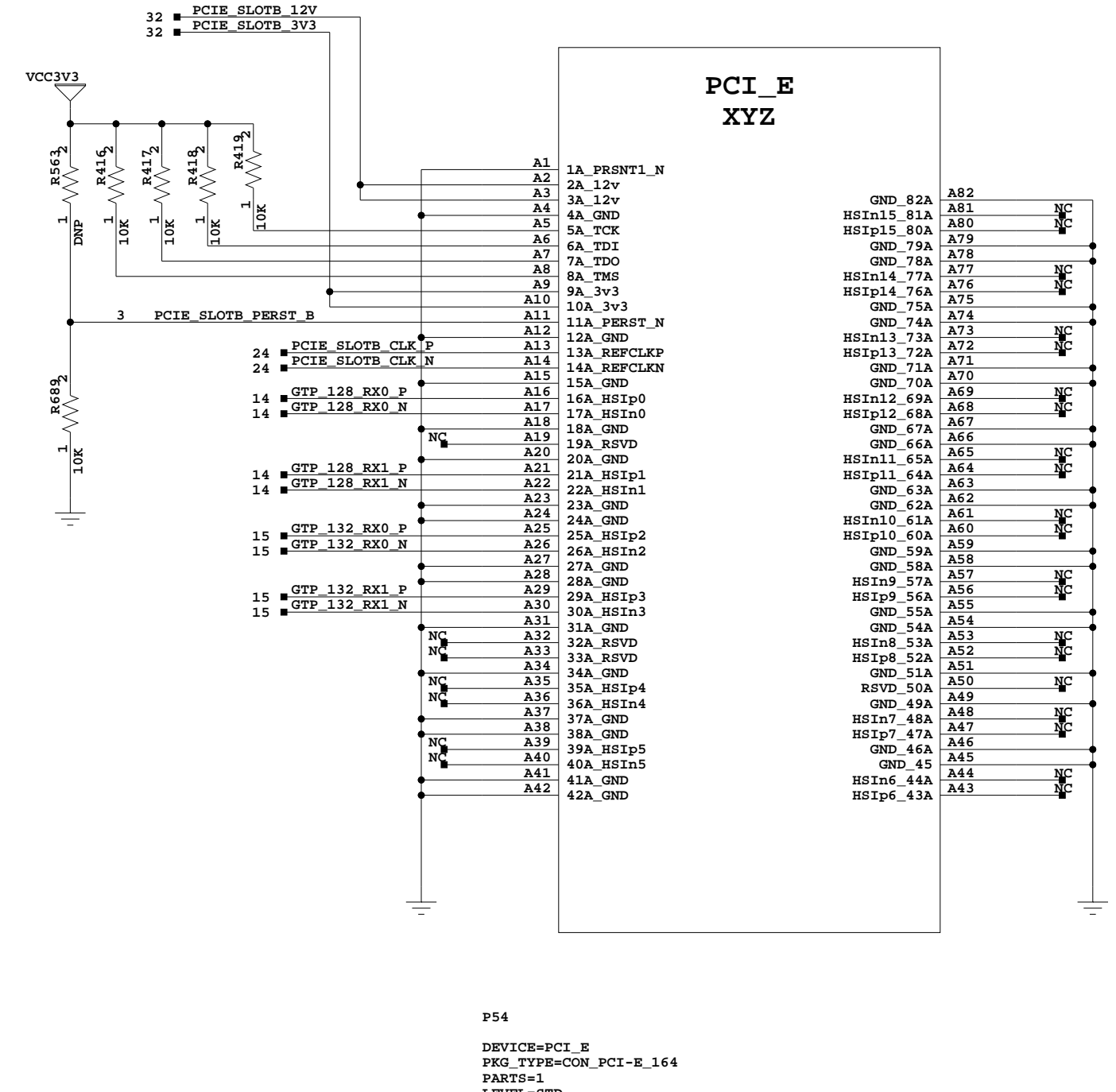
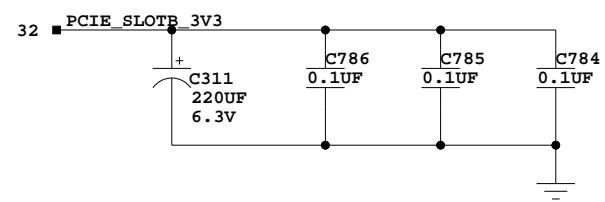
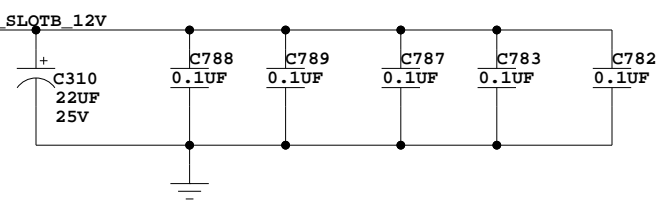
SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 PCI-E SLOT A

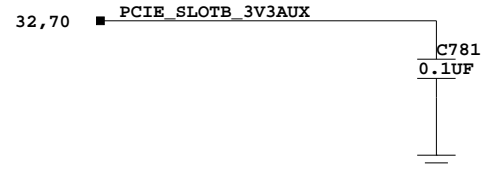
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P54  
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 PKG\_TYPE=CON\_PCI-E\_164  
 PARTS=1  
 LEVEL=STD



P54  
 DEVICE=PCI\_E  
 PKG\_TYPE=CON\_PCI-E\_164  
 PARTS=1  
 LEVEL=STD



**PCI-E SLOT B**



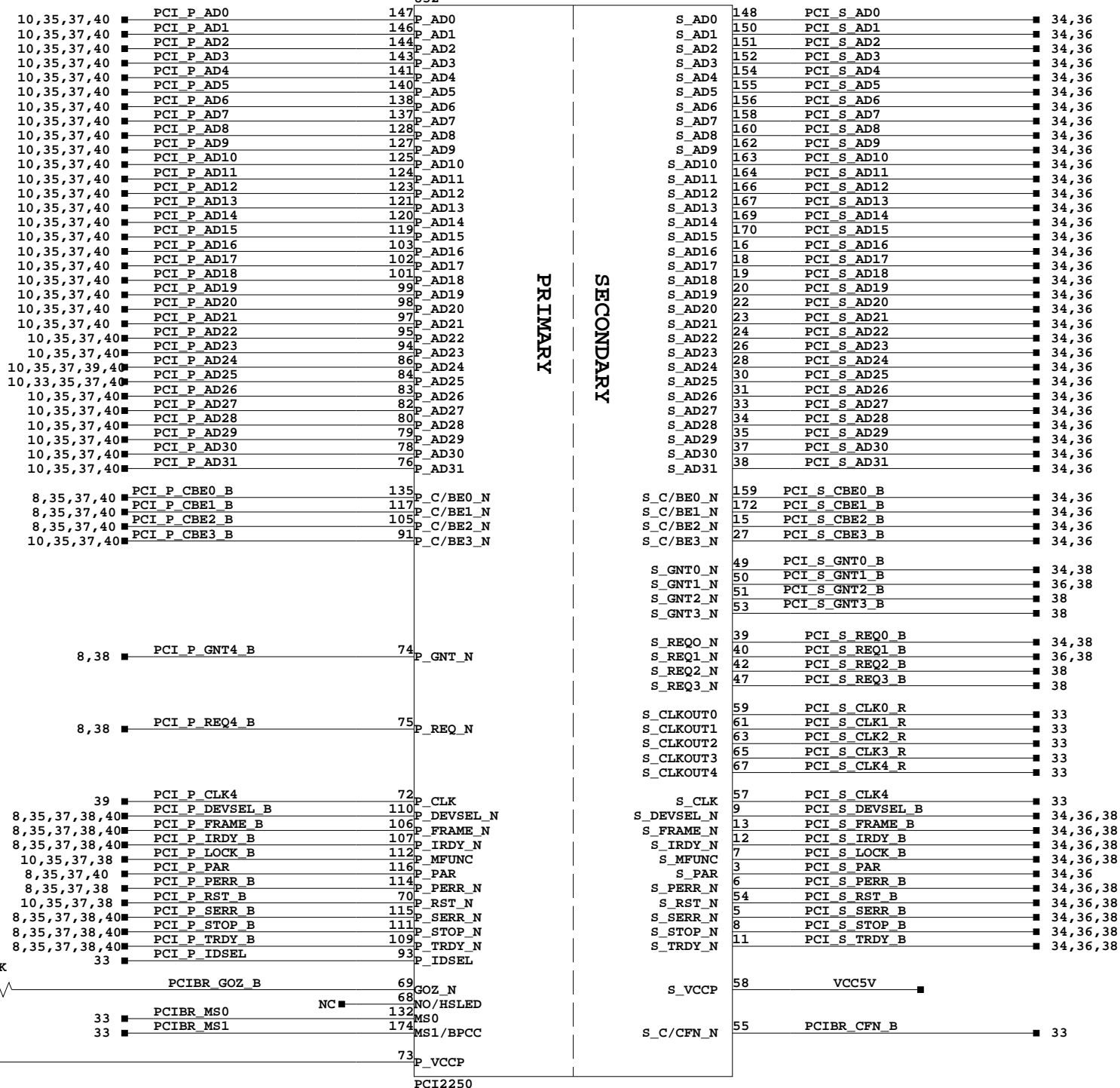
SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

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PCI-E SLOT B	
Date: 8-1-2008_15:08	Ver: C
Sheet Size: B	Rev: 01
Sheet 32 of 70	Drawn By BF

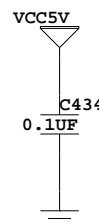
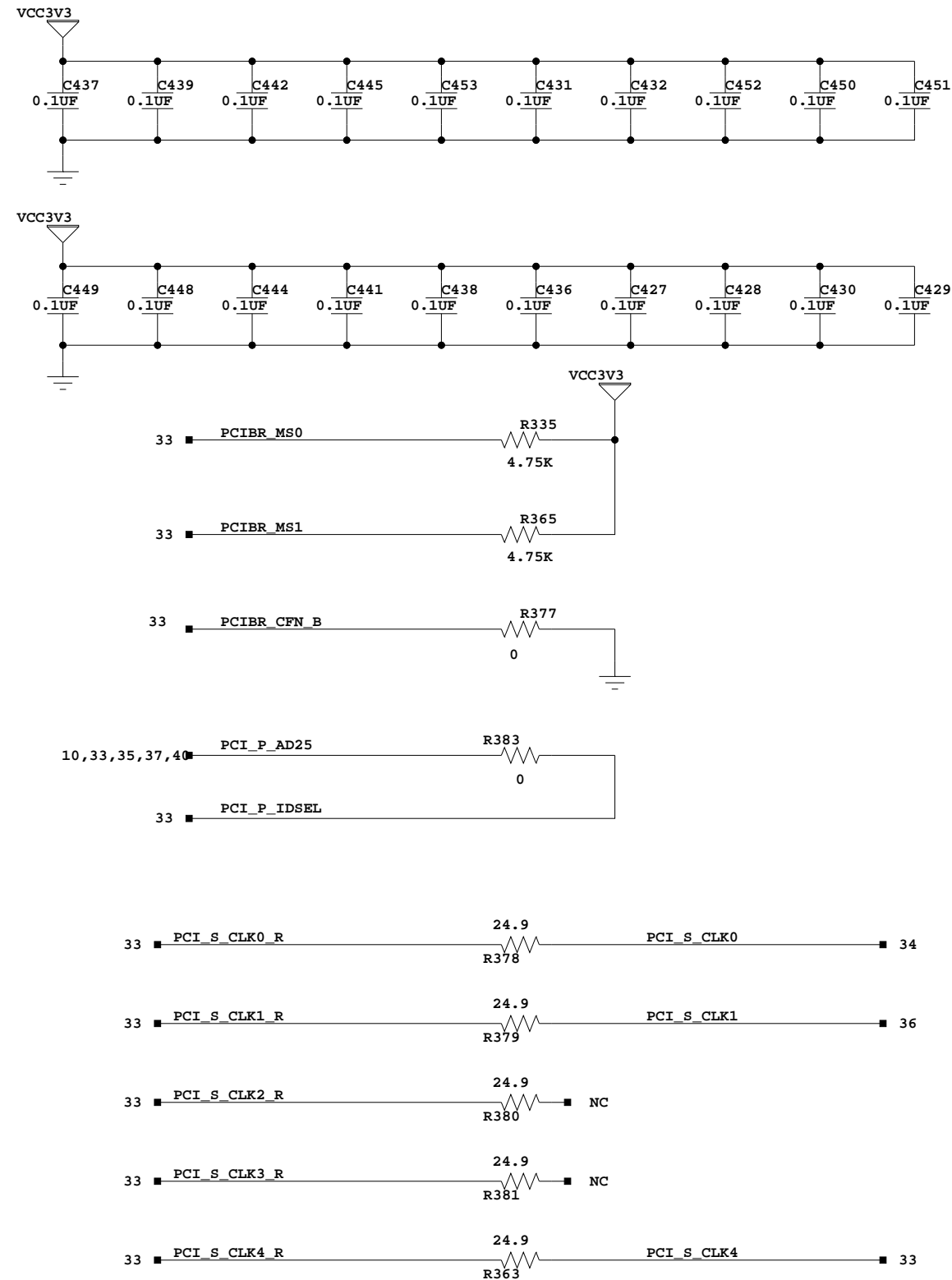


PCI-PCI BRIDGE  
PCI2250\_PGF

U32



VCC3V3;10,17,25,32,44,52,62,66,81,88,100  
VCC3V3;108,118,126,139,145,153,161,168,176  
GND;1,14,21,29,36,45,56,60,64,71,77,89  
GND;96,104,113,122,130,133,142,149,157,165,171  
NC=2,4,41,43,46,48,85,87,90,92,129,131,134,136,173,175



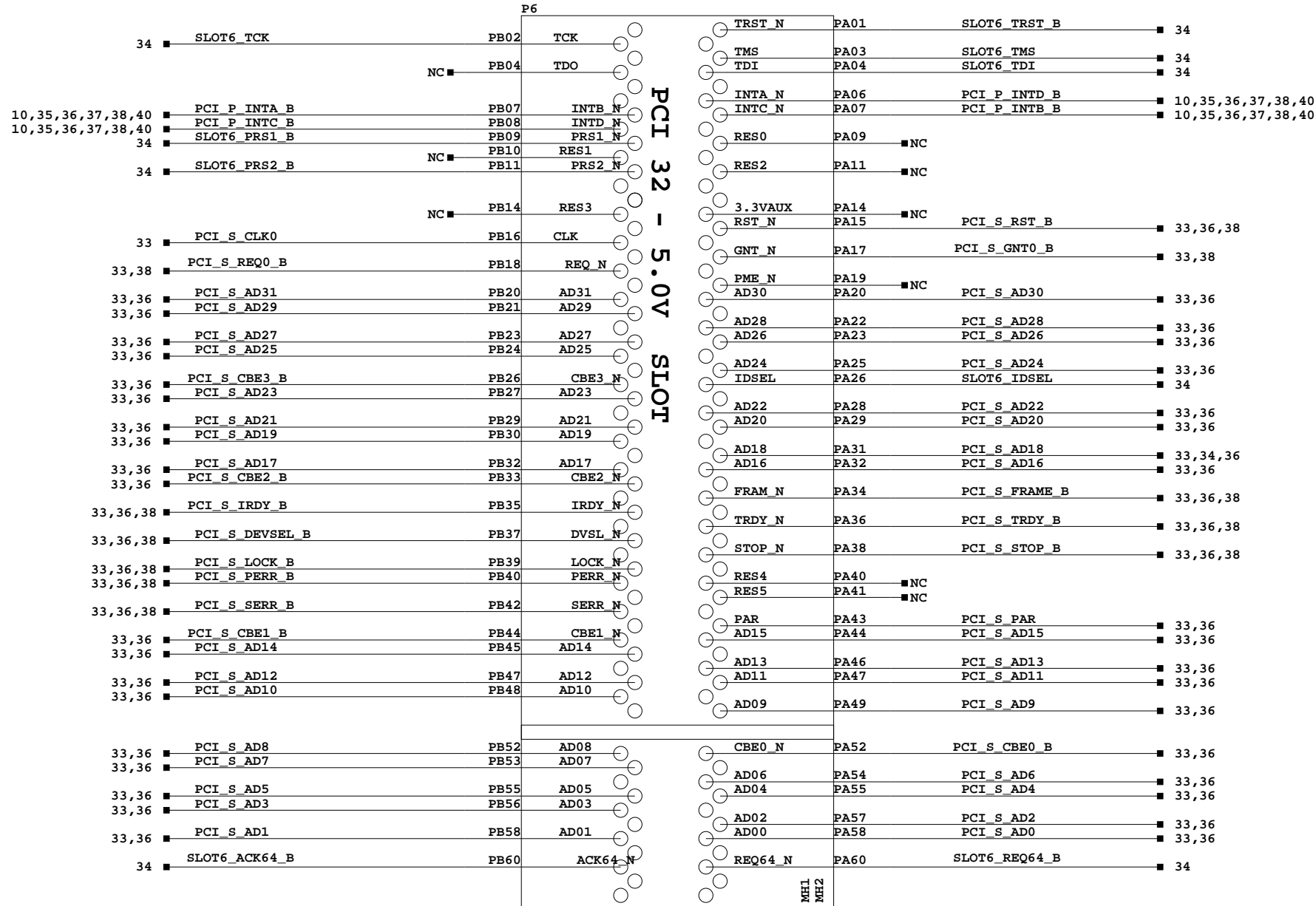
PCI-PCI BRIDGE



SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
PCI-PCI BRIDGE

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	33 of 70	Drawn By	BF

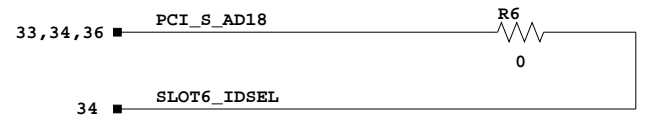
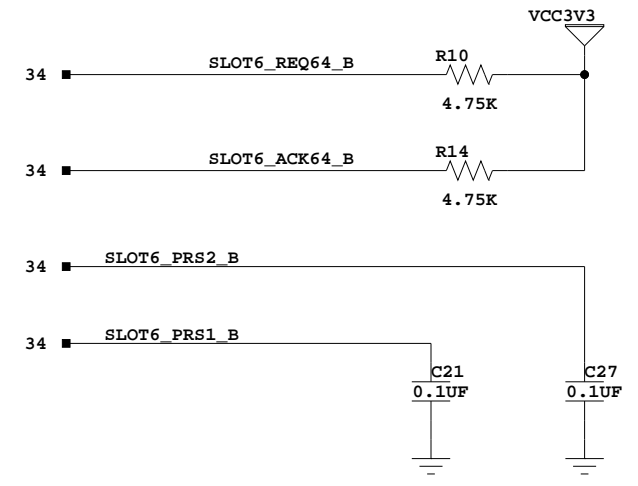
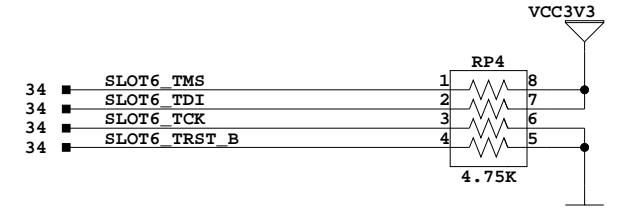
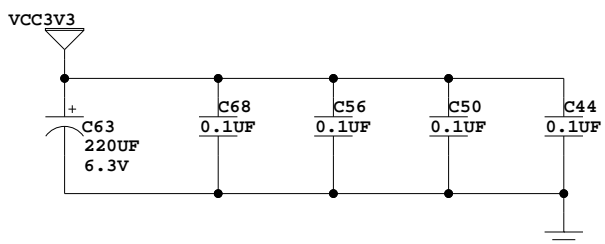
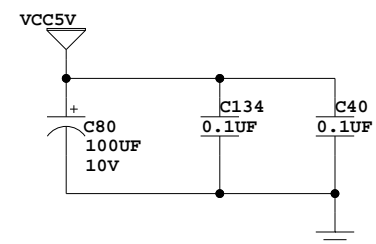
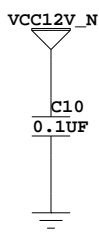
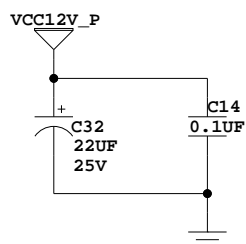


VCC12V\_P;PA02  
 VCC12V\_N;PB01  
 VCC5V;PA05, PB05, PB06, PA08, PA61, PA62, PB61, PB62

VCC3V3;PA21, PB25, PA27, PB31, PA33, PB36  
 VCC3V3;PA39, PB41, PB43, PA45, PA53, PB54

VCCIO VCC5V;PA10, PA16, PB19, PB59, PA59

GND;PB03, PB15, PB17, PA18, PB22, PA24  
 GND;PB28, PA30, PB34, PA35, PA37, PB38  
 GND;PA42, PB46, PA48, PB49, PA56, PB57  
 GND;PB12, PA12, PB13, PA13

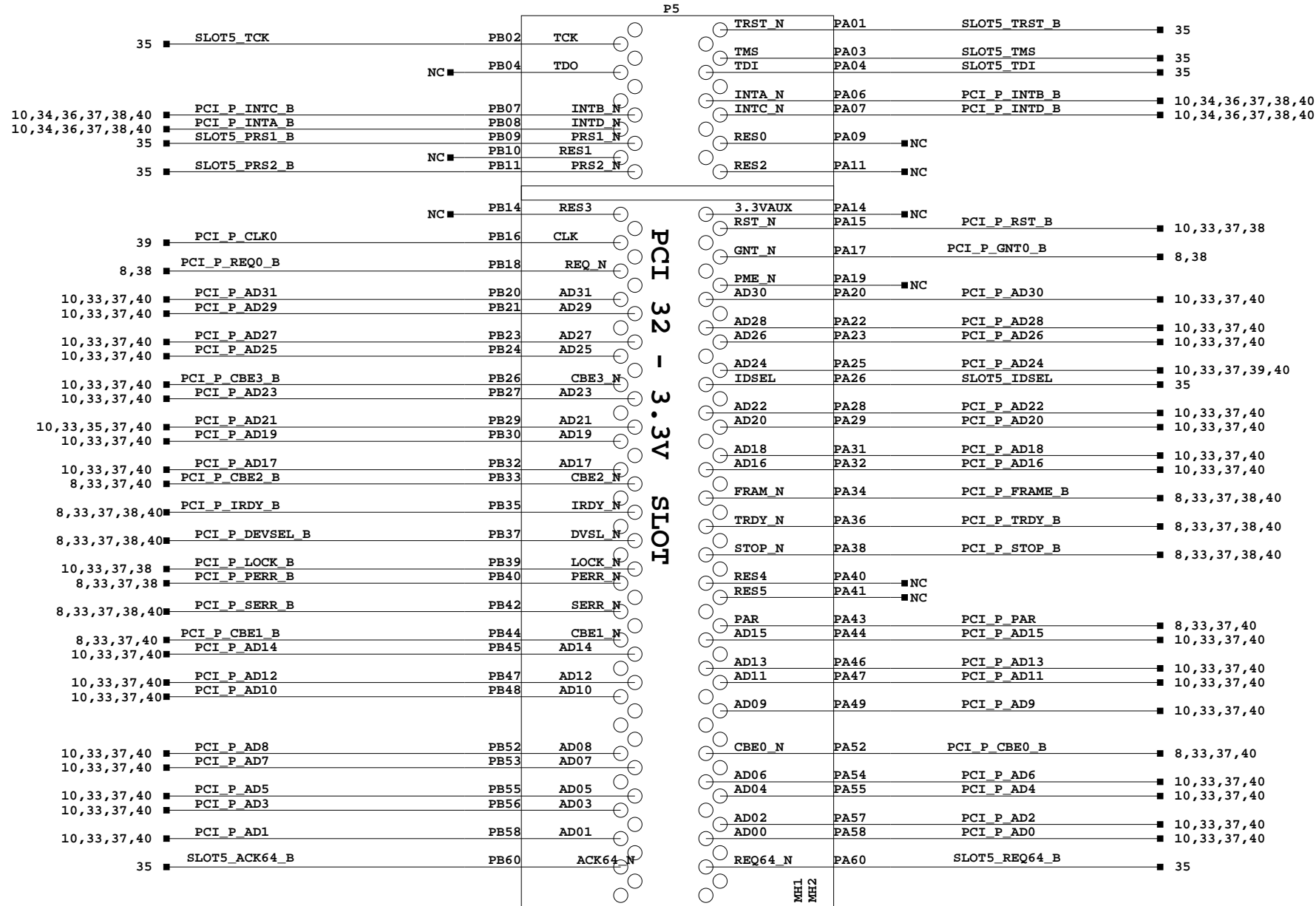


PCI SLOT 6, 5.0V, SECONDARY BUS

**XILINX** SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 PCI SLOT 6, 5.0V, SECONDARY BUS

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Sheet	34 of 70	Drawn By	BF

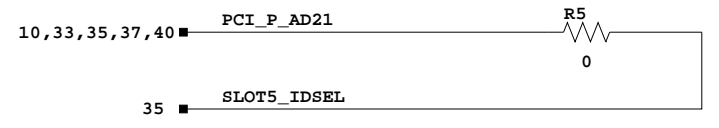
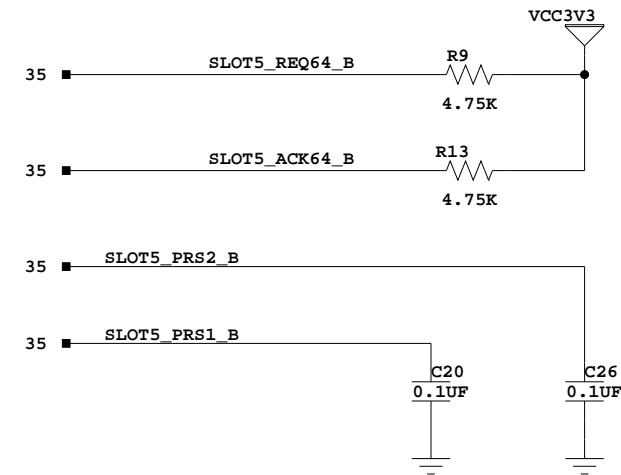
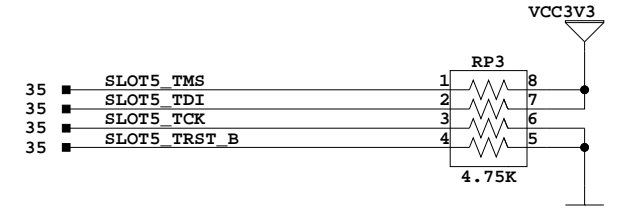
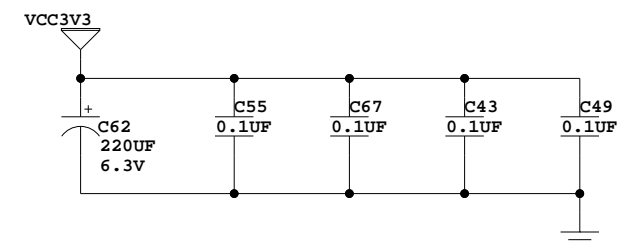
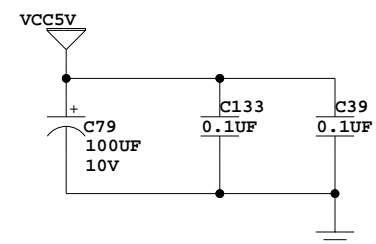
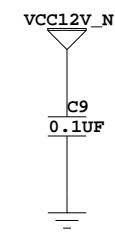
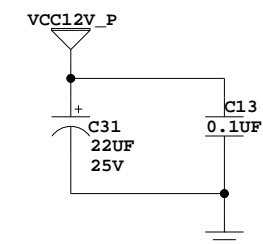


SIGNAL=GND; PA50, PA51, PB50, PB51

VCC12V\_P;PA02  
VCC12V\_N;PB01  
VCC5V;PA05, PB05, PB06, PA08  
VCC5V;PA61, PB61, PA62, PB62  
VCC3V3;PA21, PB25, PA27, PB31, PA33, PB36  
VCC3V3;PA39, PB41, PB43, PA45, PA53, PB54

VCCIO VCC3V3;PA10, PA16, PB19, PB59, PA59

GND;PB03, PB15, PB17, PA18, PB22, PA24  
GND;PB28, PA30, PB34, PA35, PA37, PB38  
GND;PA42, PB46, PA48, PB49, PA56, PB57



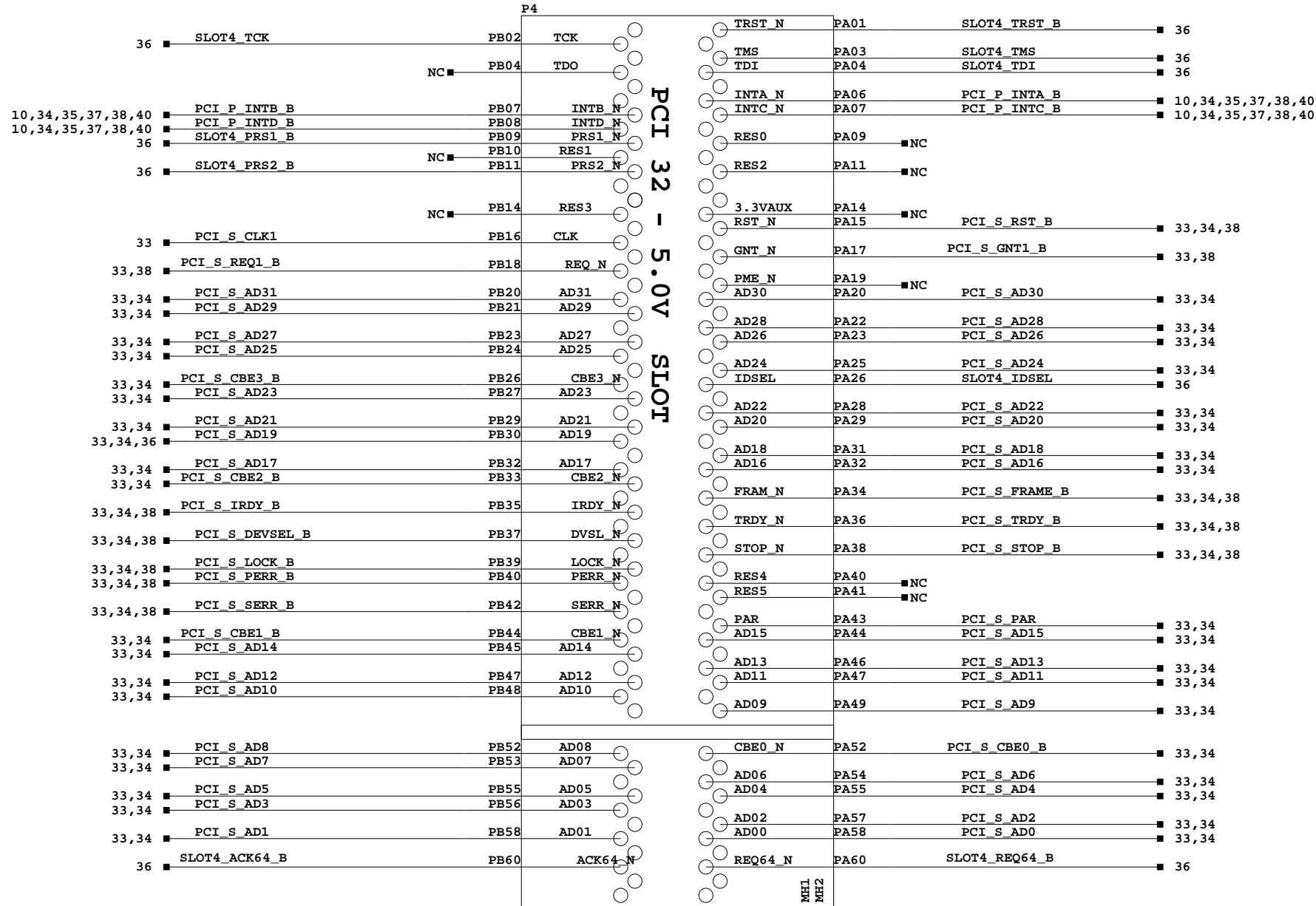
PCI SLOT 5, 3.3V, PRIMARY BUS



SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
PCI SLOT 5, 3.3V, PRIMARY BUS

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	35 of 70	Drawn By	BF

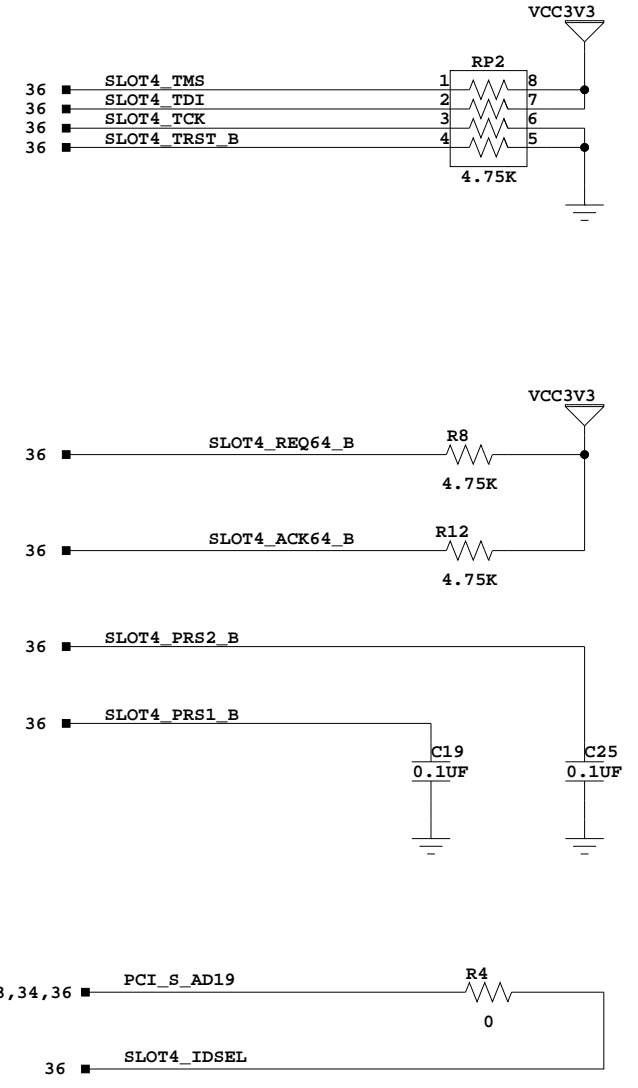
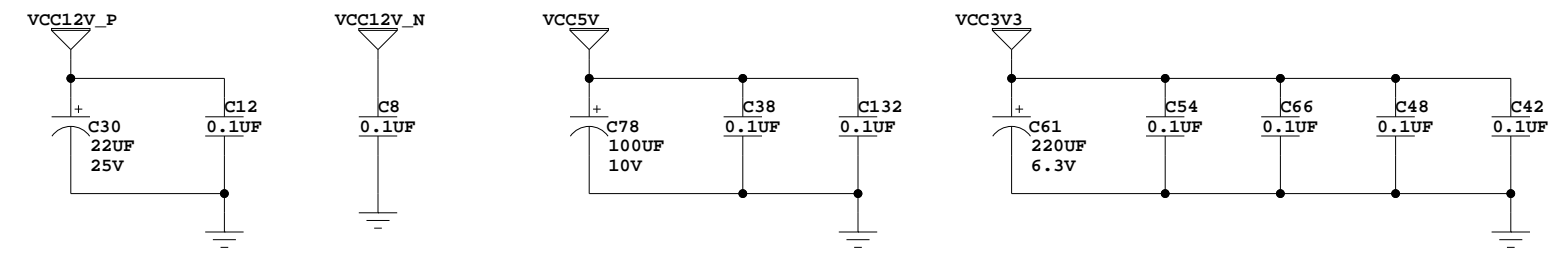


VCC12V\_P;PA02  
VCC12V\_N;PB01  
VCC5V;PA05, PB05, PB06, PA08, PA61, PA62, PB61, PB62

VCC3V3;PA21, PB25, PA27, PB31, PA33, PB36  
VCC3V3;PA39, PB41, PB43, PA45, PA53, PB54

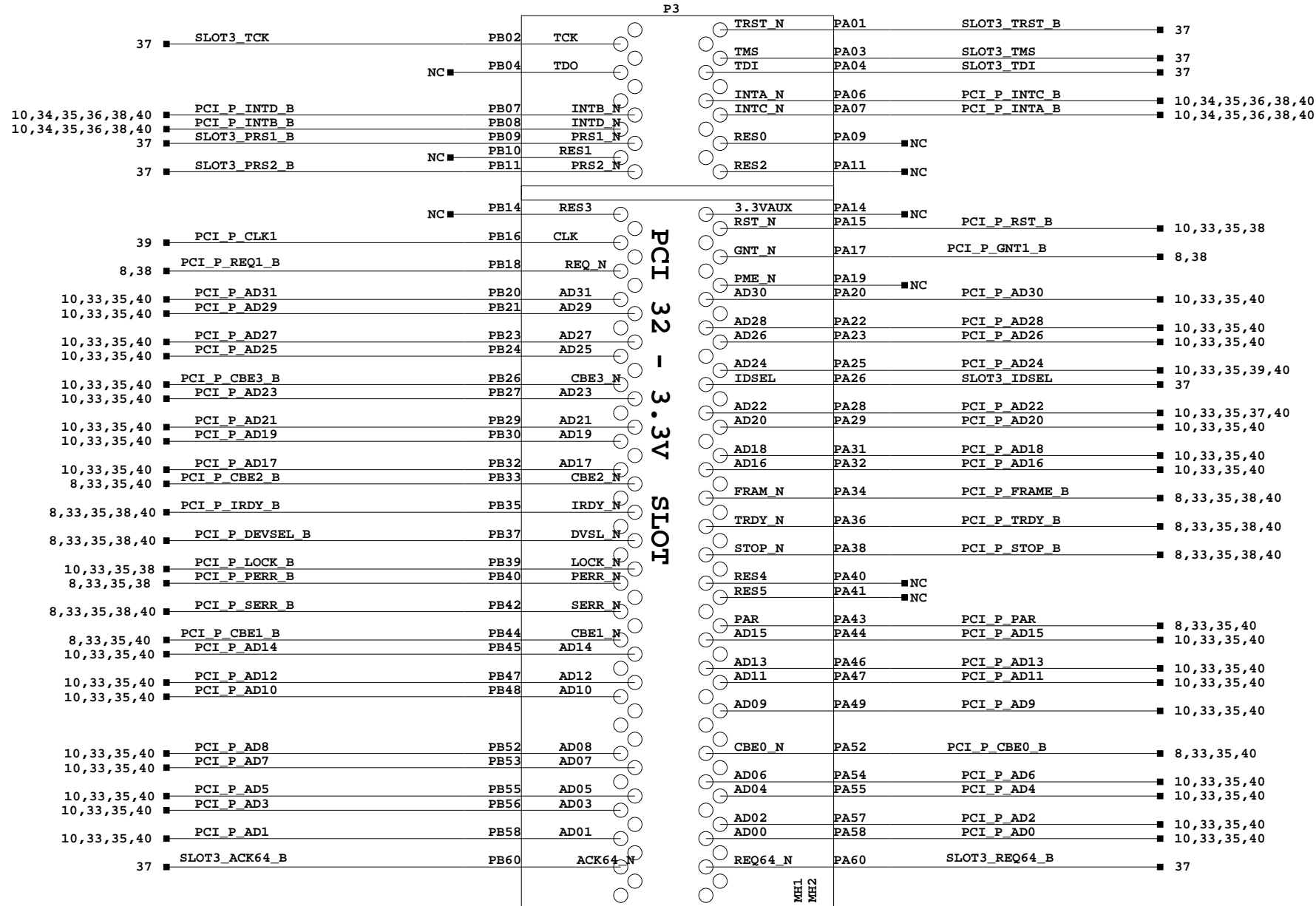
VCCIO VCC5V;PA10, PA16, PB19, PB59, PA59

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GND;PB28, PA30, PB34, PA35, PA37, PB38  
GND;PA42, PB46, PA48, PB49, PA56, PB57  
GND;PB12, PA12, PB13, PA13



**PCI SLOT 4, 5.0V, SECONDARY BUS**

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM		
PCI SLOT 4, 5.0V, SECONDARY BUS		
Date:	7-10-2008_10:19	Ver: C
Sheet Size:	B	Rev: 01
Sheet	<b>36</b> of <b>70</b>	Drawn By BF

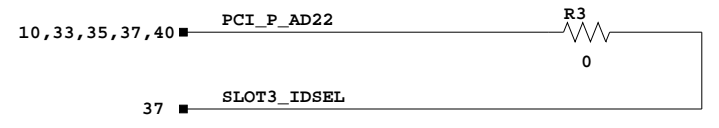
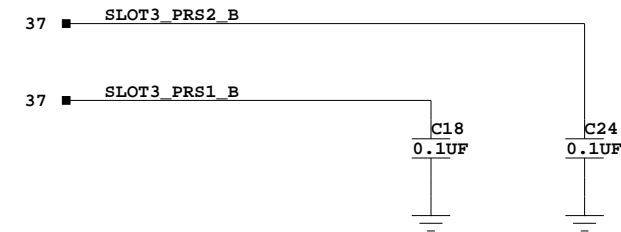
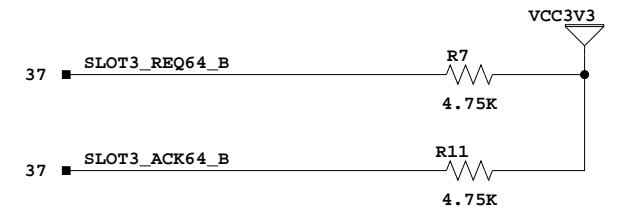
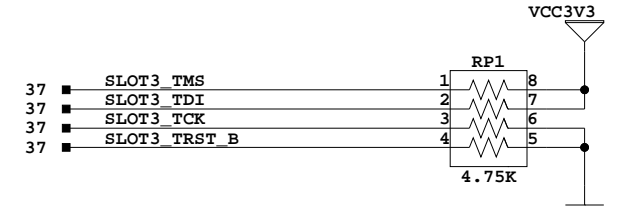
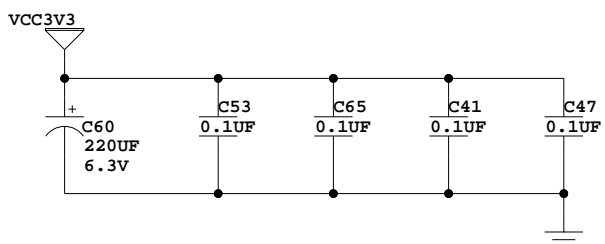
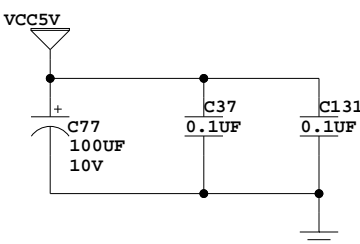
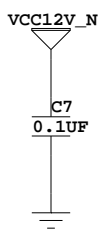
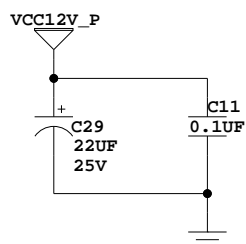


SIGNAL=GND; PA50, PA51, PB50, PB51

VCC12V\_P;PA02  
 VCC12V\_N;PB01  
 VCC5V;PA05, PB05, PB06, PA08  
 VCC5V;PA61, PB61, PA62, PB62  
 VCC3V3;PA21, PB25, PA27, PB31, PA33, PB36  
 VCC3V3;PA39, PB41, PB43, PA45, PA53, PB54

VCCIO VCC3V3;PA10, PA16, PB19, PB59, PA59

GND;PB03, PB15, PB17, PA18, PB22, PA24  
 GND;PB28, PA30, PB34, PA35, PA37, PB38  
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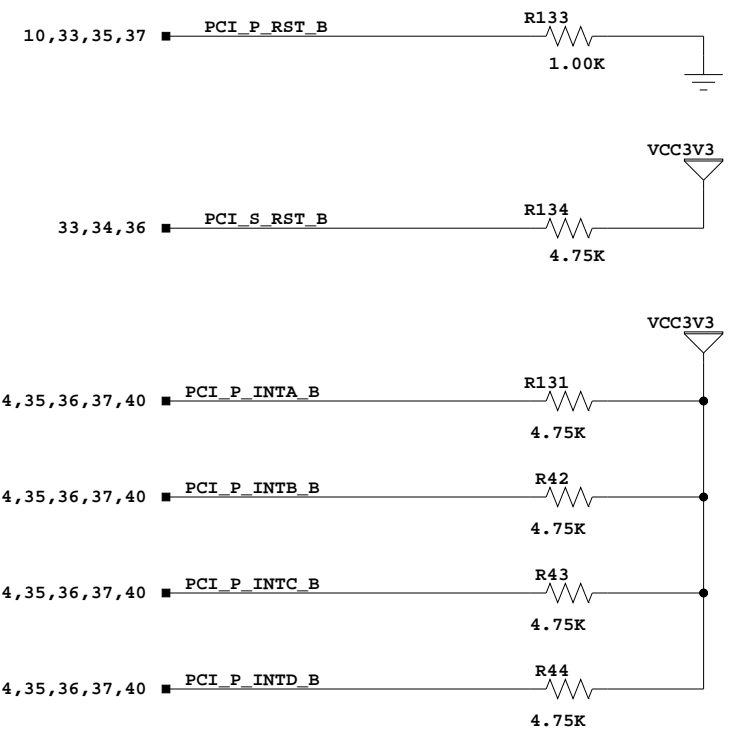
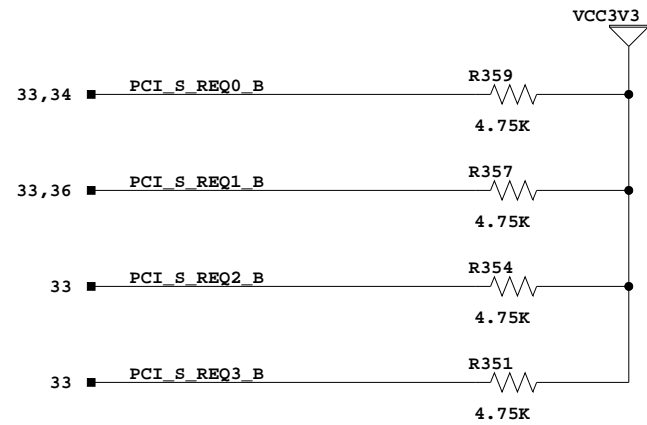
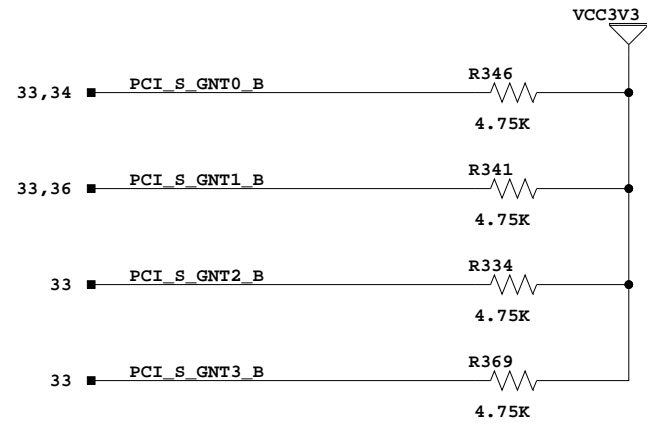
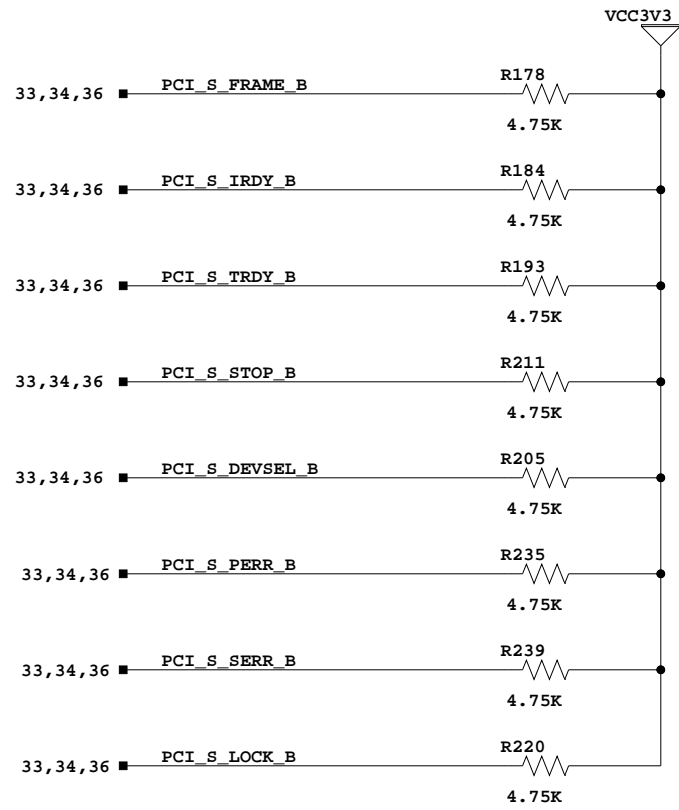
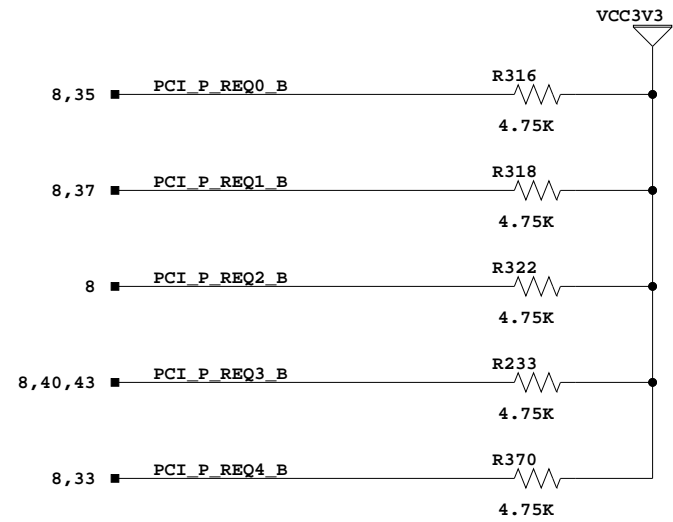
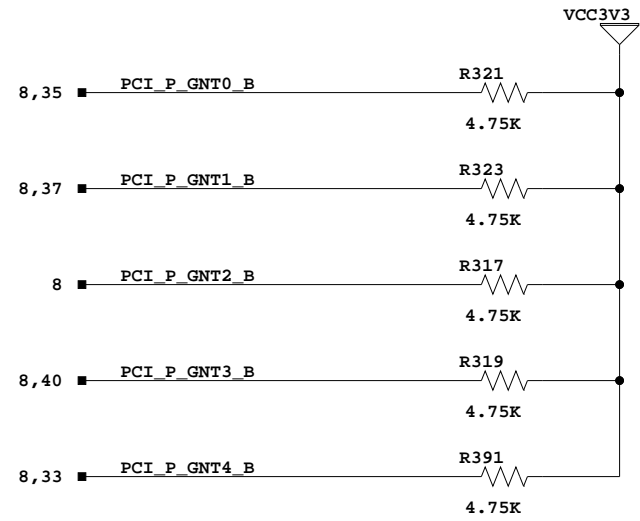
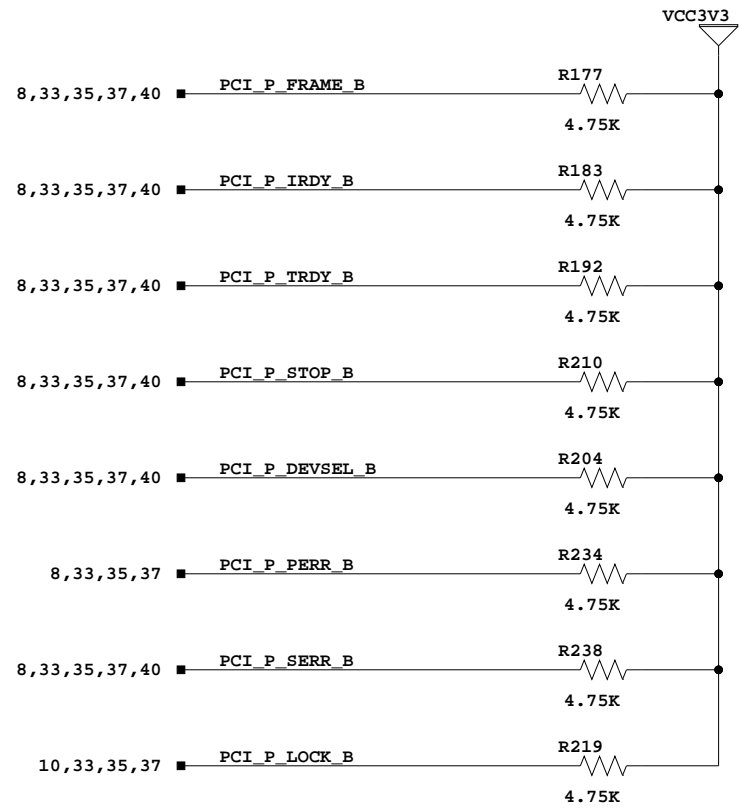
PCI SLOT 3, 3.3V, PRIMARY BUS



SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 PCI SLOT 3, 3.3V, PRIMARY BUS

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	37 of 70	Drawn By	BF



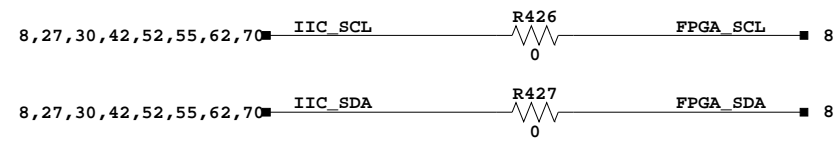
### PCI BUS PULLUPS



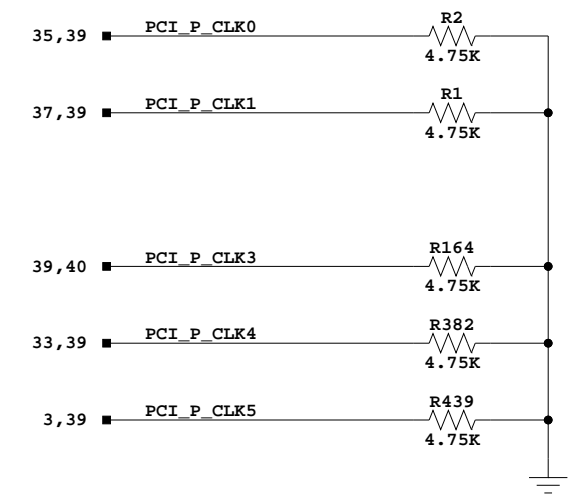
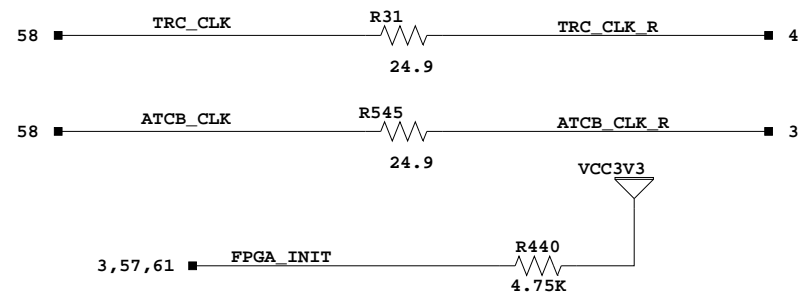
SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 PCI BUS PULLUPS

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	38 of 70	Drawn By	BF

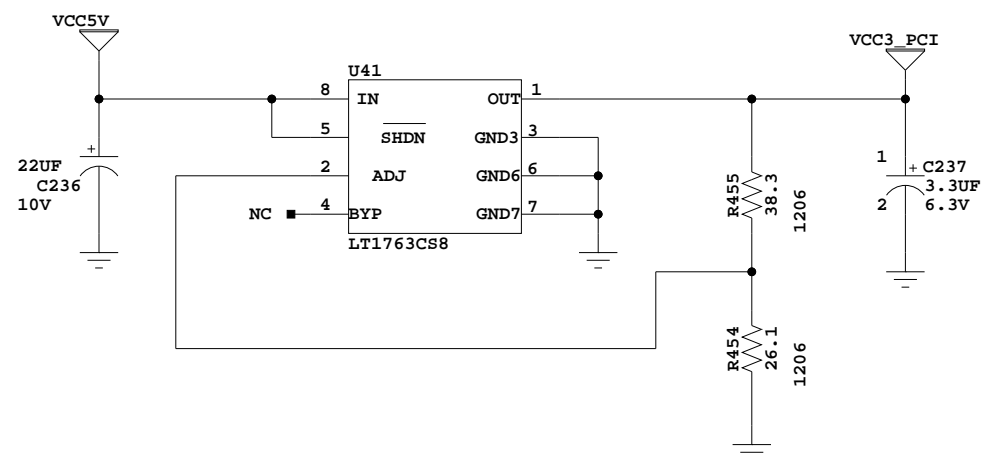
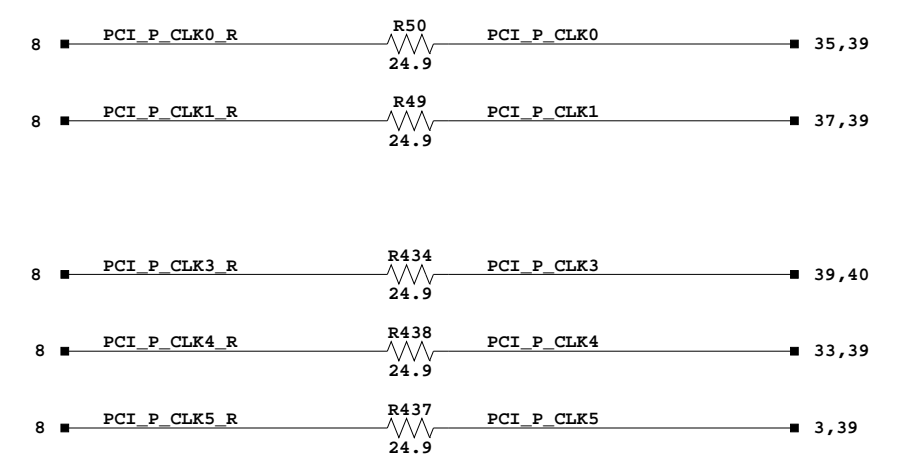


NOTE: TRC\_CLK RESISTOR ALLOWS CLOCK TERMINATION  
 TO BE ADJUSTED INDEPENDENTLY OF OTHER I/O.

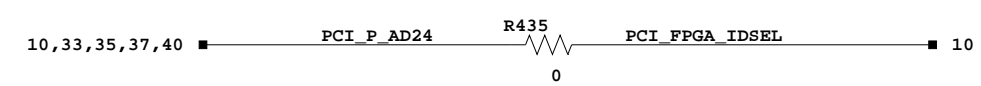


NOTE: THE PCI SPEC RECOMMENDS THAT  
 CLOCKS BE PULLED LOW WHEN THE  
 BUS IS NOT ACTIVELY CLOCKED.

NOTE: PCI\_CLK RESISTORS ALLOW CLOCK TERMINATION  
 TO BE ADJUSTED INDEPENDENTLY OF OTHER I/O.



NOTE: THE COMPONENT VALUES FOR THIS REGULATOR ARE TAKEN  
 FROM XAPP653. THIS DESIGN IS INTENDED TO SINK CURRENT  
 THROUGH THE 1206 RESISTORS WHEN THE CLAMP DIODES ON  
 THE FPGA ARE CONDUCTING DURING OVERSHOOT. THIS IS WHY  
 THE VALUES ARE UNUSUAL RELATIVE TO THE LT1763 DATASHEET.

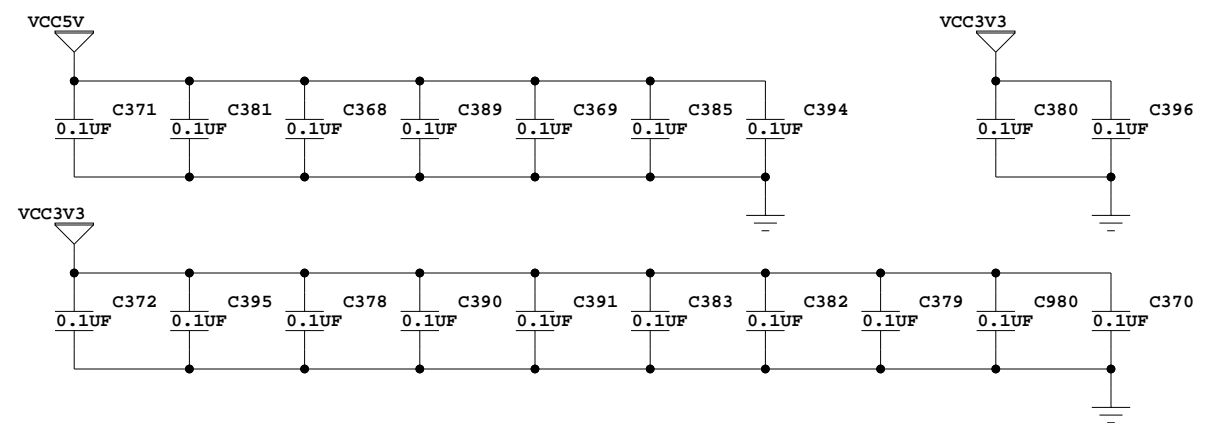
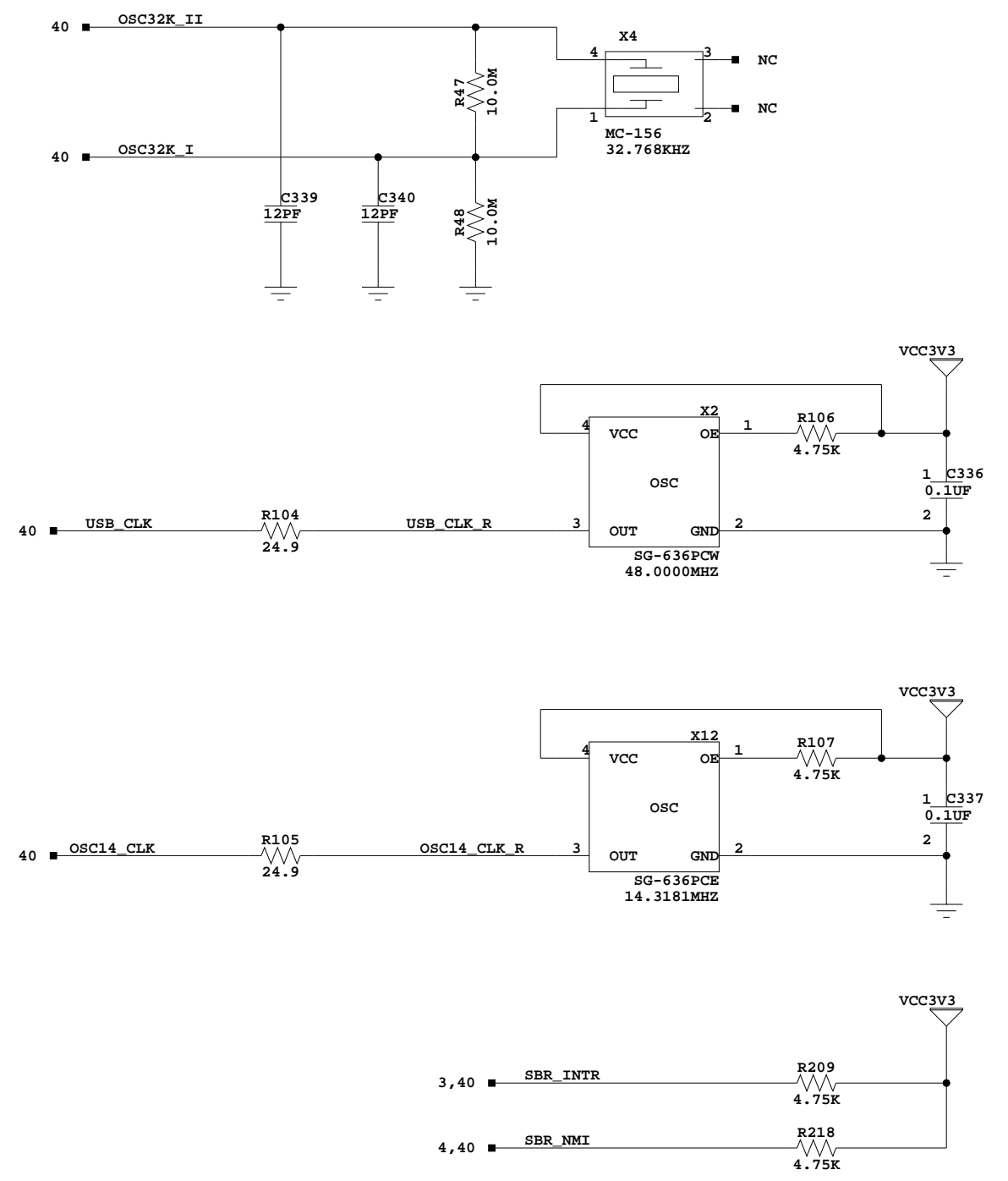
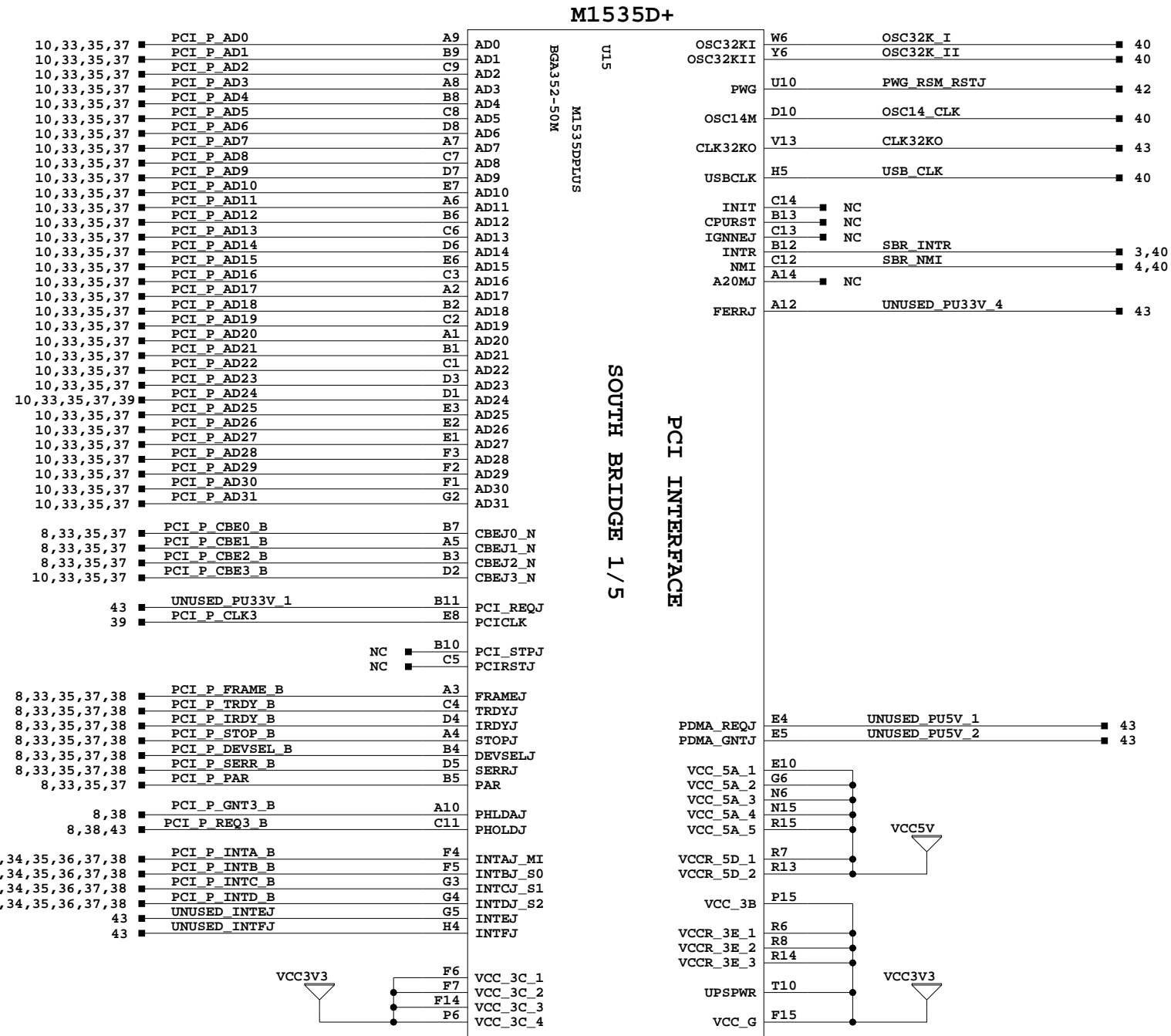


### PCI SUPPLY AND TERMINATION



SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM PCI SUPPLY AND TERMINATION	
Date: 7-10-2008_10:19	Ver: C
Sheet Size: B	Rev: 01
Sheet 39 of 70	Drawn By BF



**PCI SOUTH BRIDGE, PART 1**

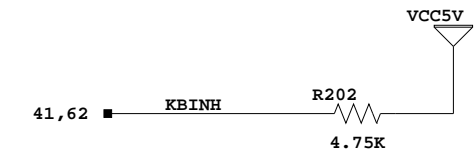
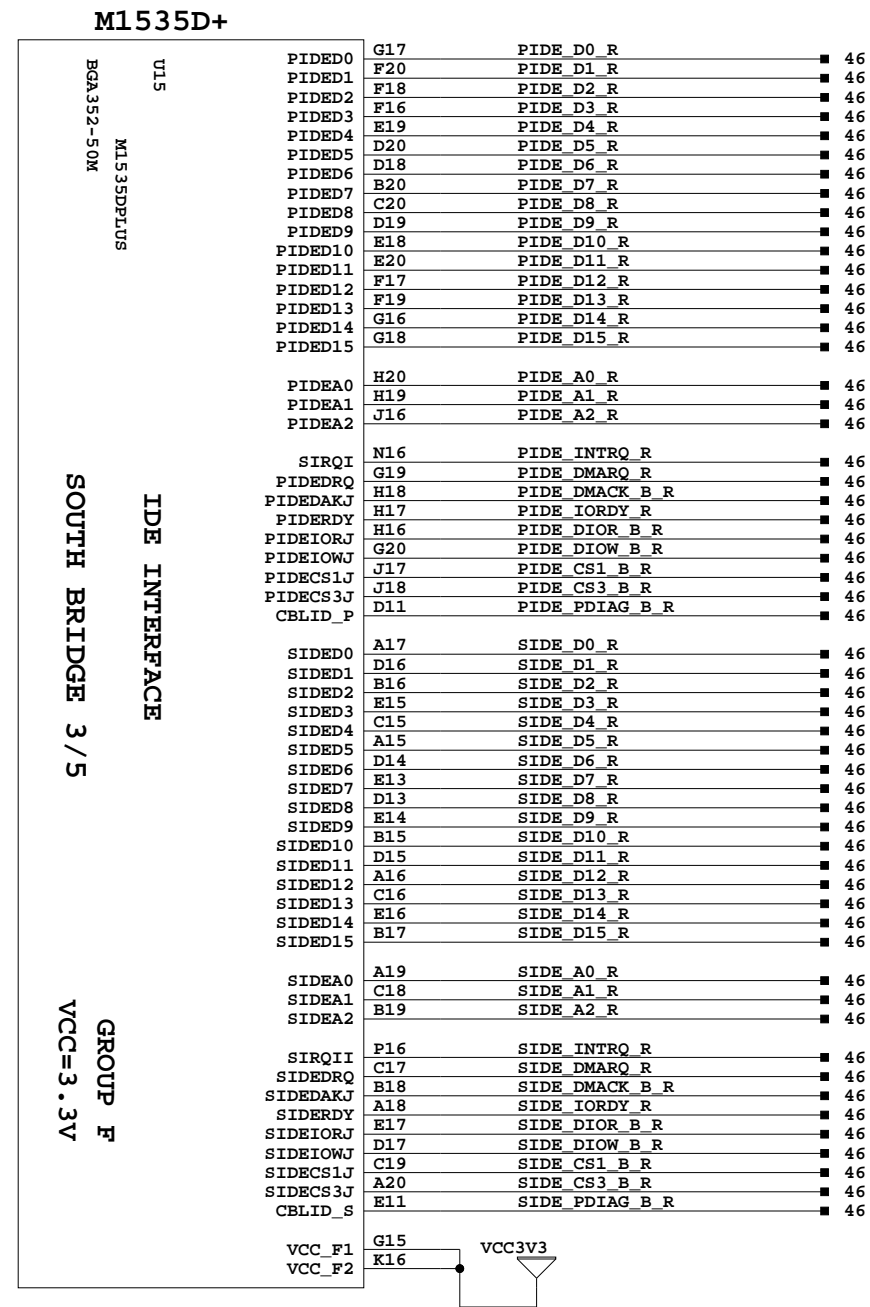
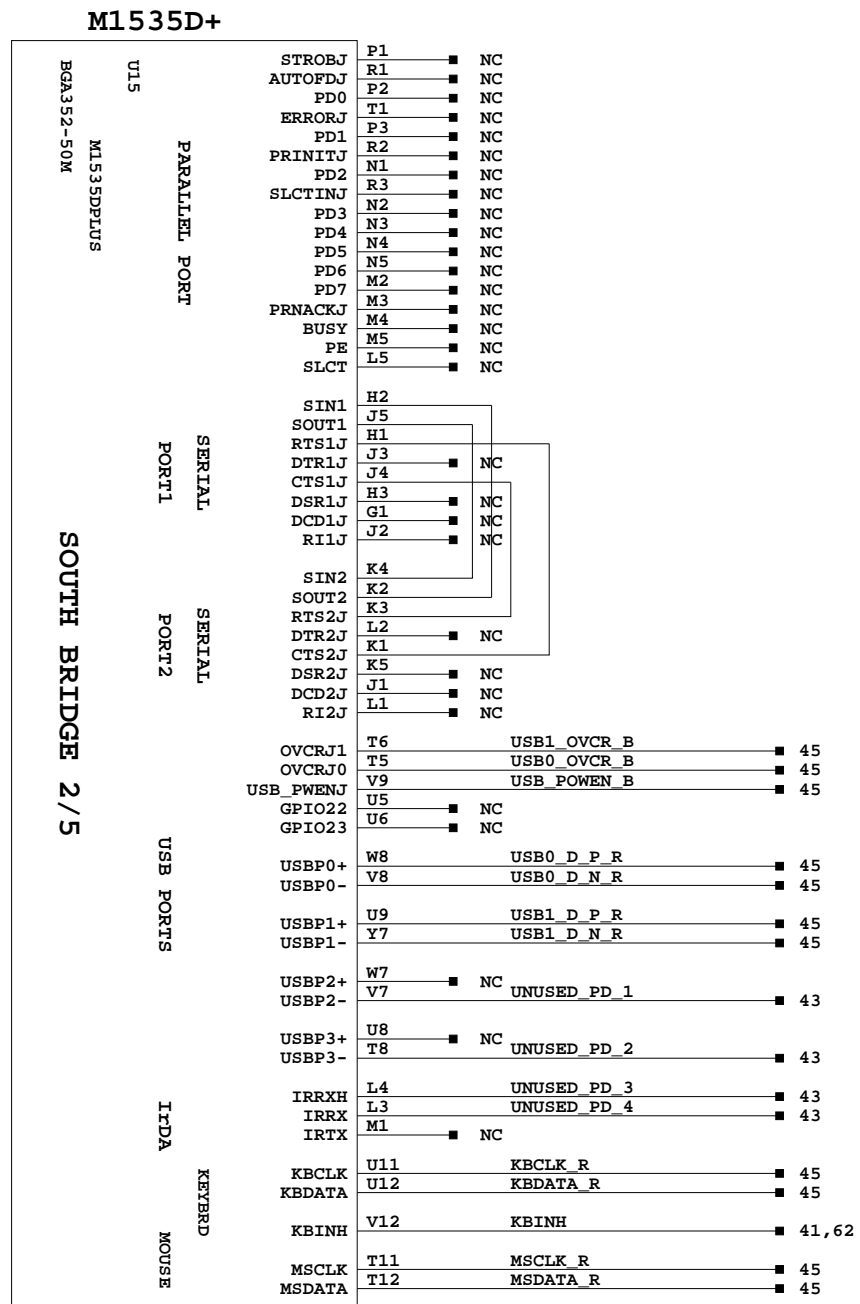


SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 PCI SOUTH BRIDGE, PART 1

Date:	7-10-2008_10:19	Ver:	C
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**PCI SOUTH BRIDGE, PART 2-3**



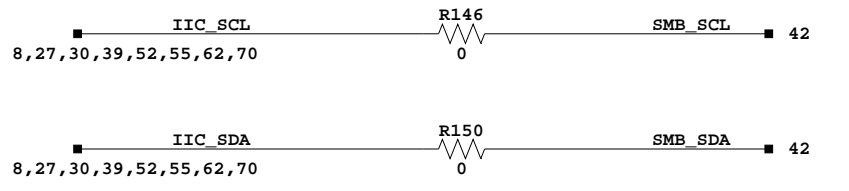
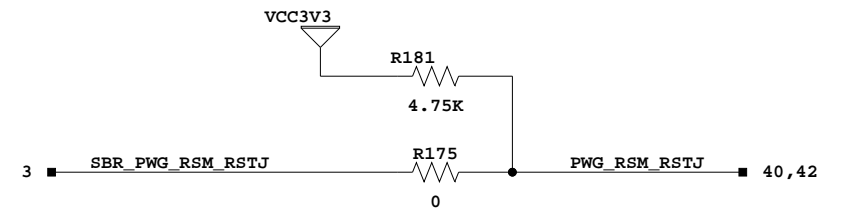
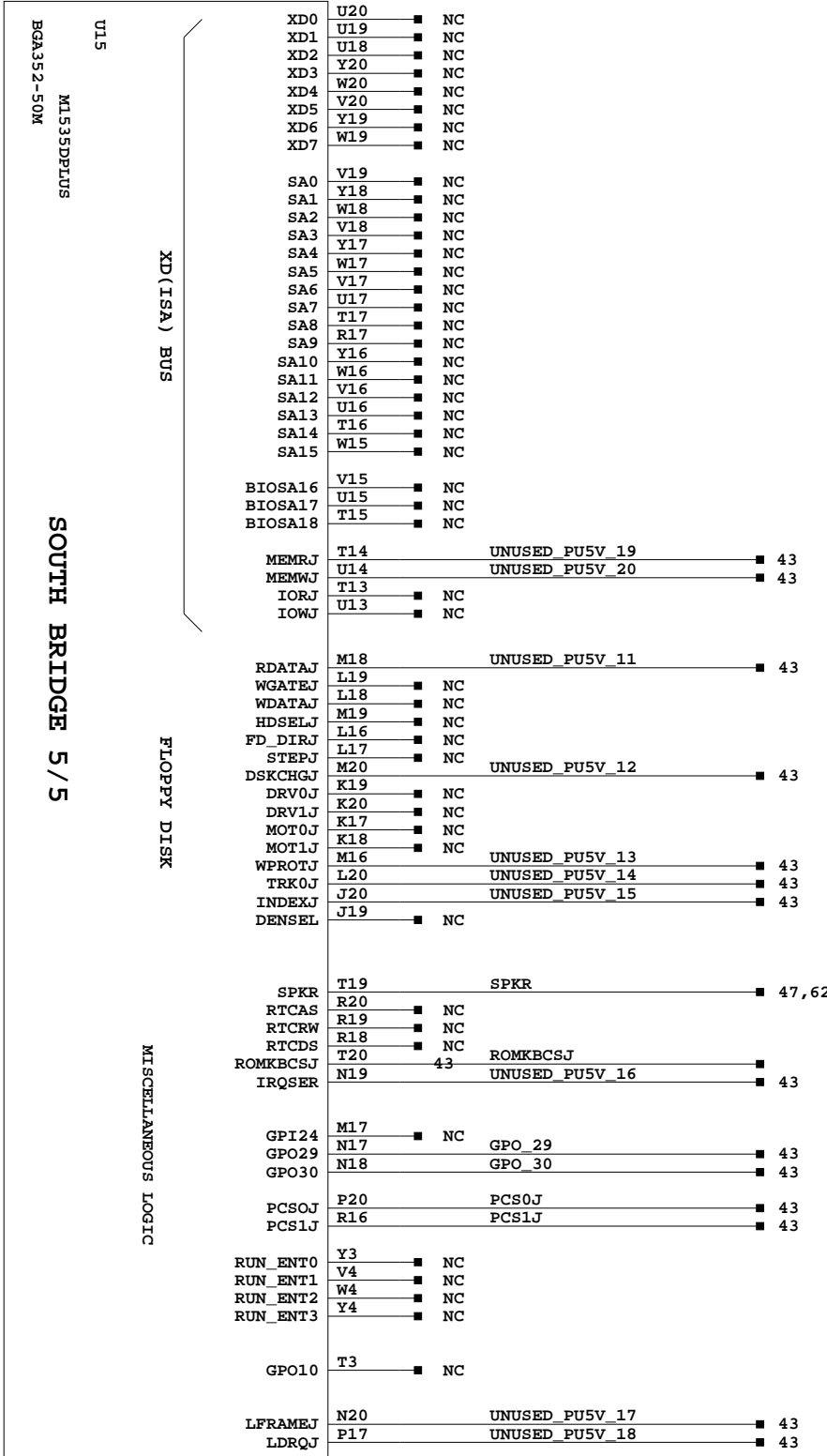
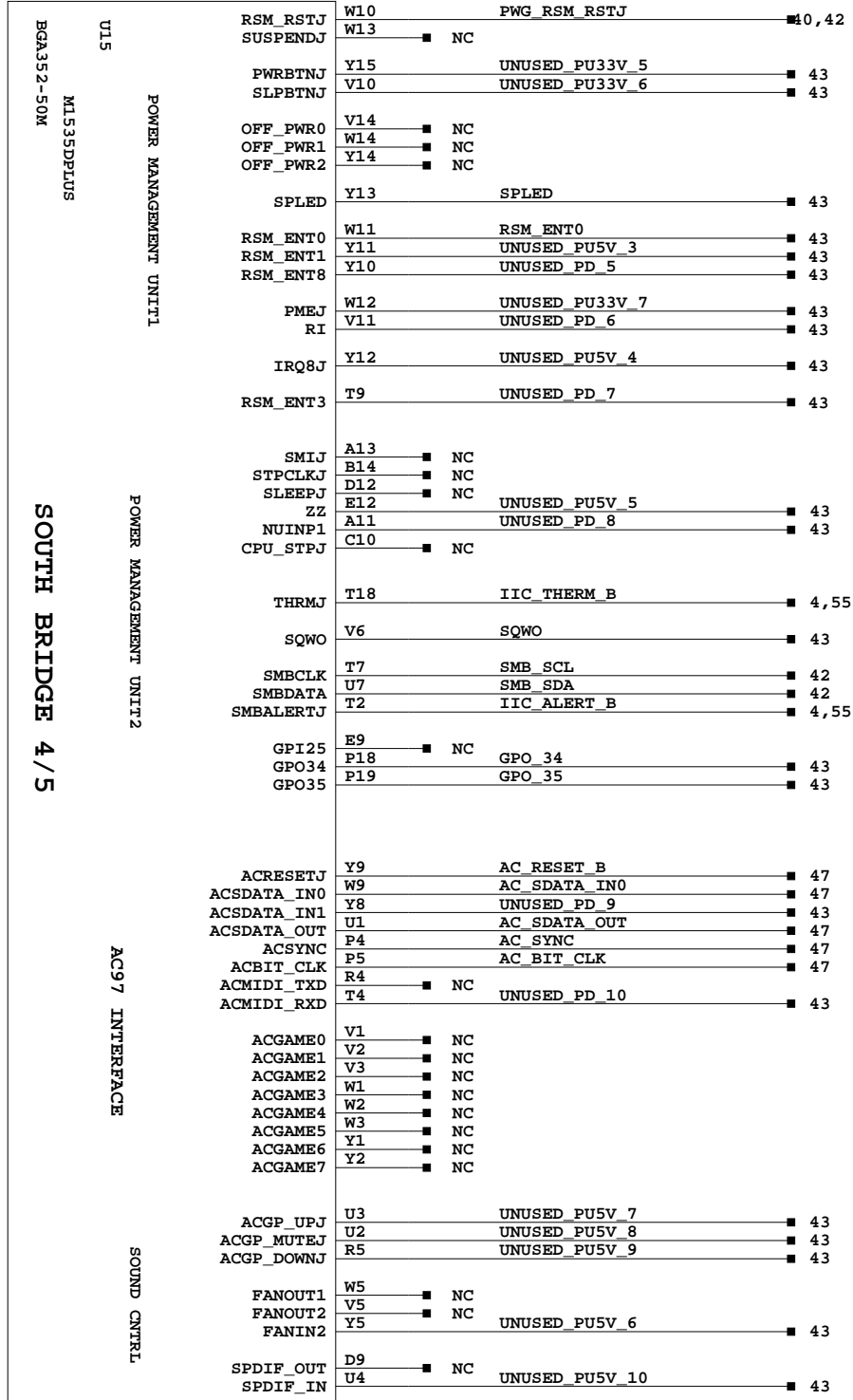
SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
PCI SOUTH BRIDGE, PART 2-3

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
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M1535D+

M1535D+



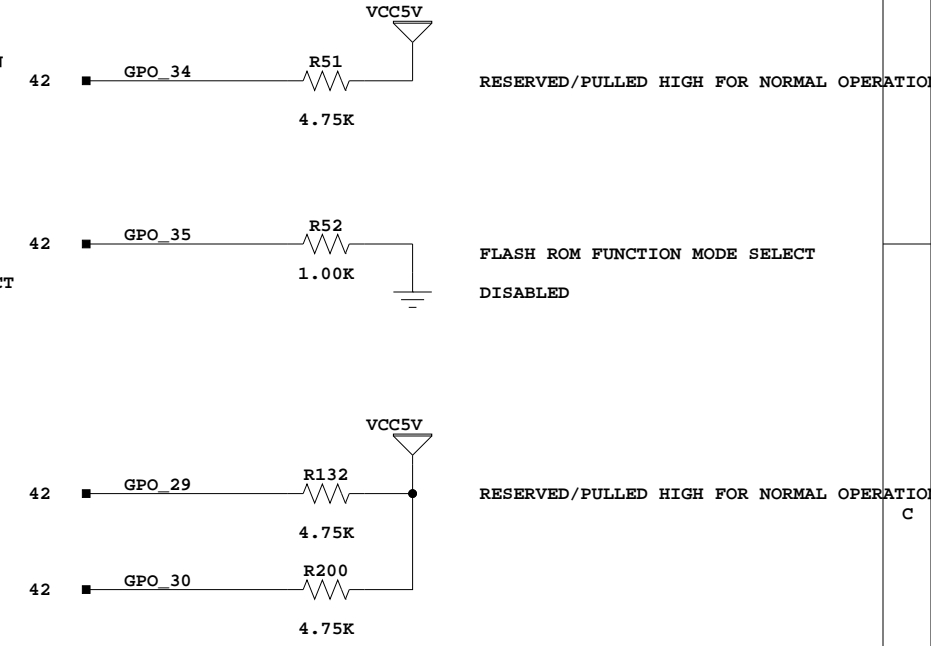
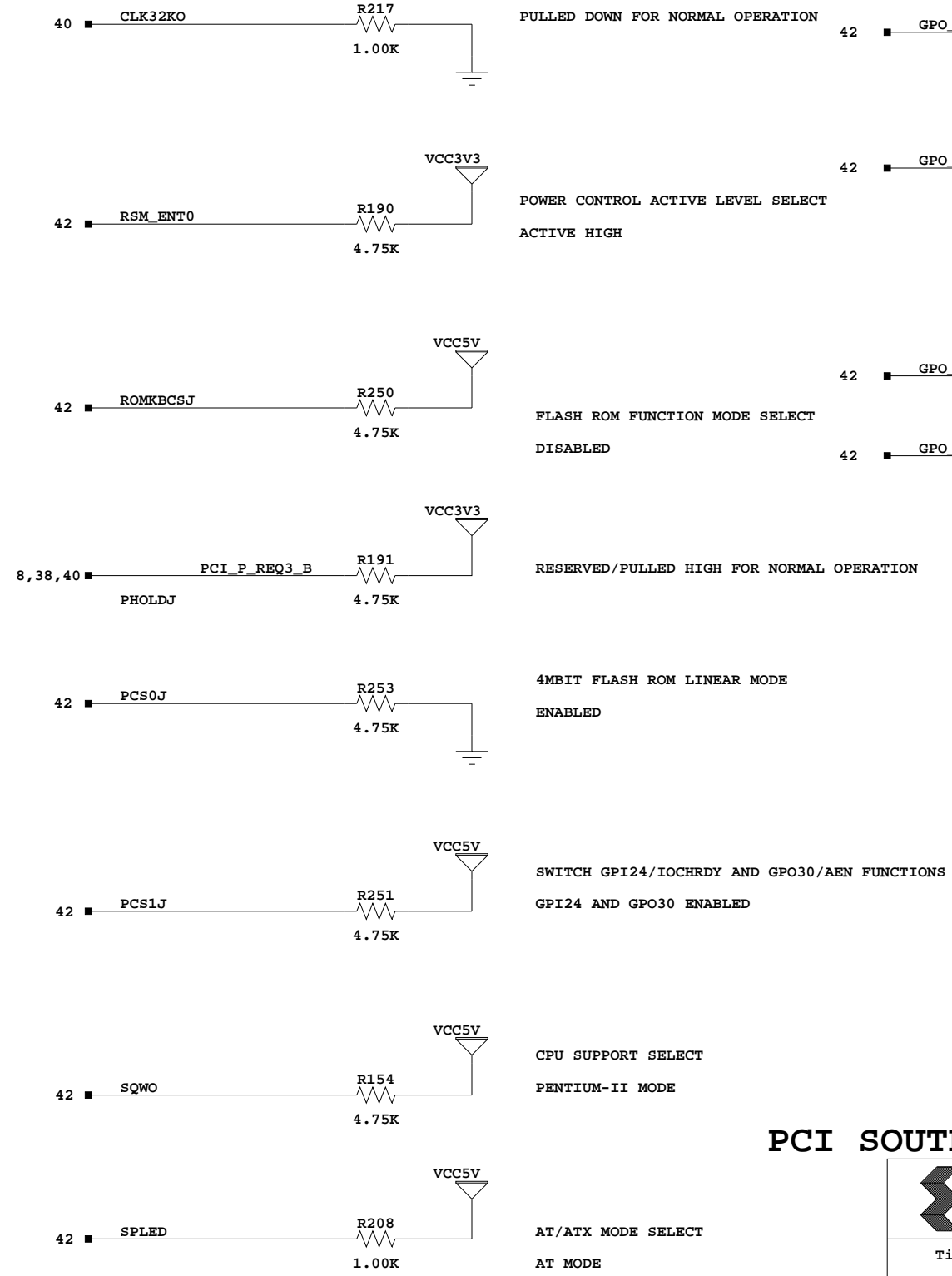
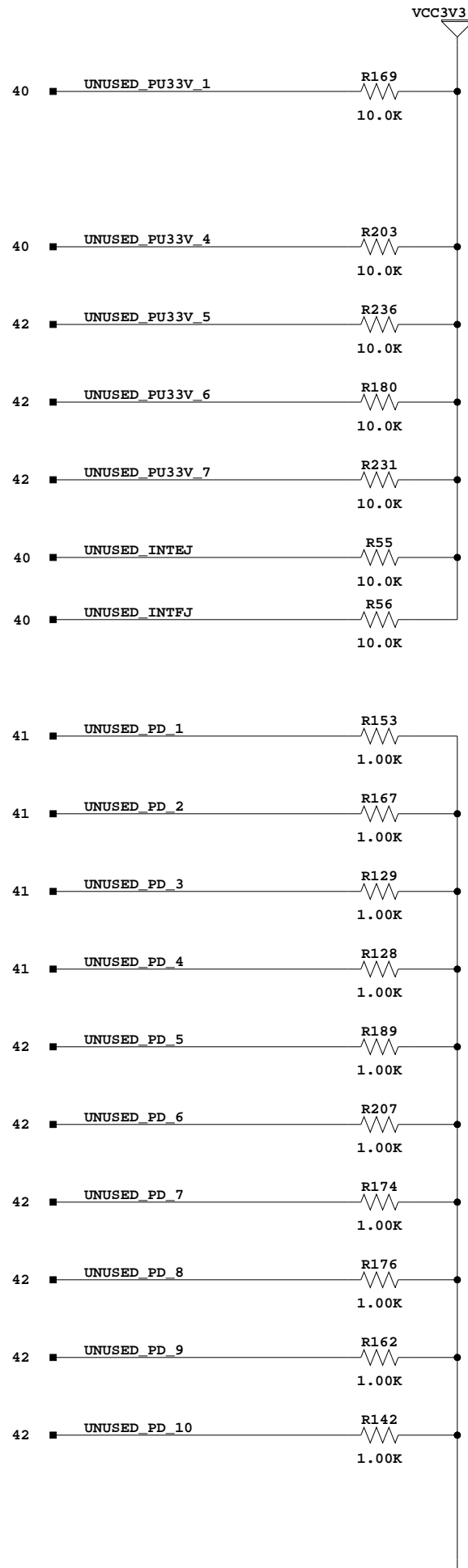
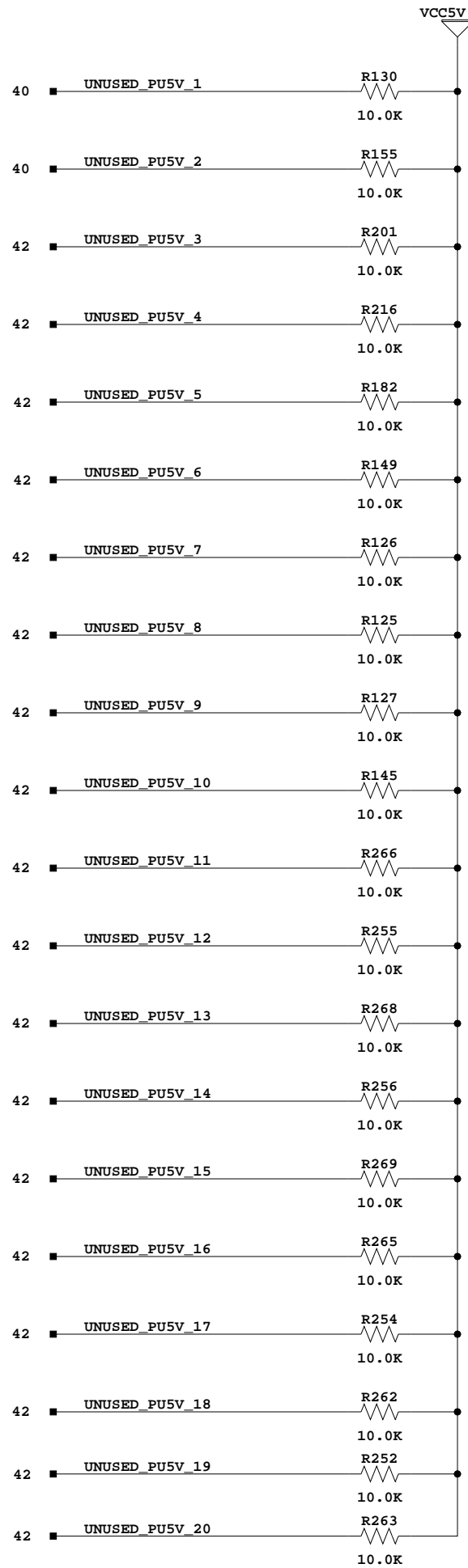
PCI SOUTH BRIDGE, PART 4-5



SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
PCI SOUTH BRIDGE, PART 4-5

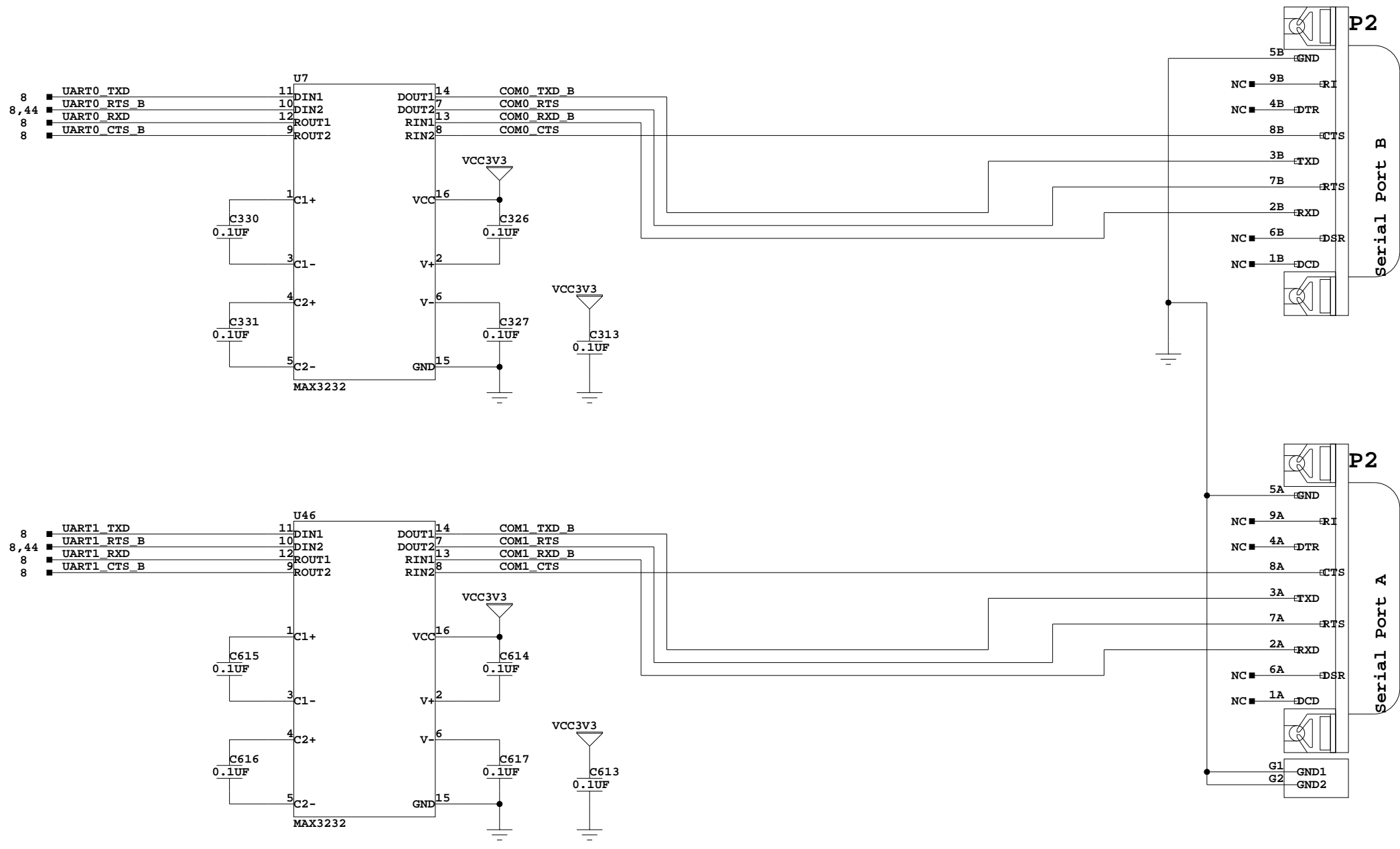
Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	42 of 70	Drawn By	BF



NOTE: AT MODE IS USED HERE TO DISABLE THE SOFTWARE FUNCTIONALITY OF THE SOUTH BRIDGE

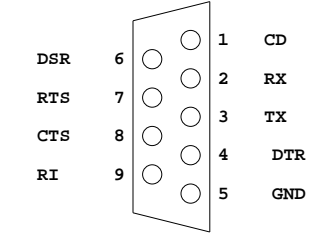
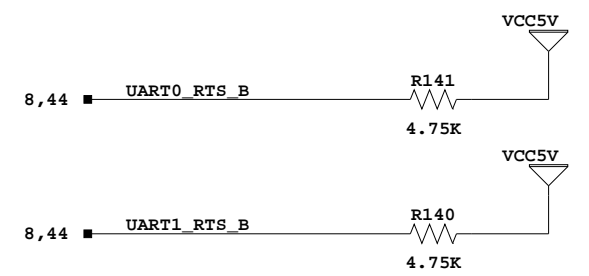
PCI SOUTH BRIDGE, CONFIG and UNUSED

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOM		
PCI SOUTH BRIDGE, UNUSED PIN RESISTORS		
Date:	7-10-2008_10:19	Ver: C
Sheet Size:	B	Rev: 01
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Silkscreen:  
"COM 1"

Silkscreen:  
"COM 2"



RS232 DTE PINOUT  
CONNECTS TO PC WITH  
F/F NULL MODEM CABLE.

LOOKING INTO DB9 PLUG

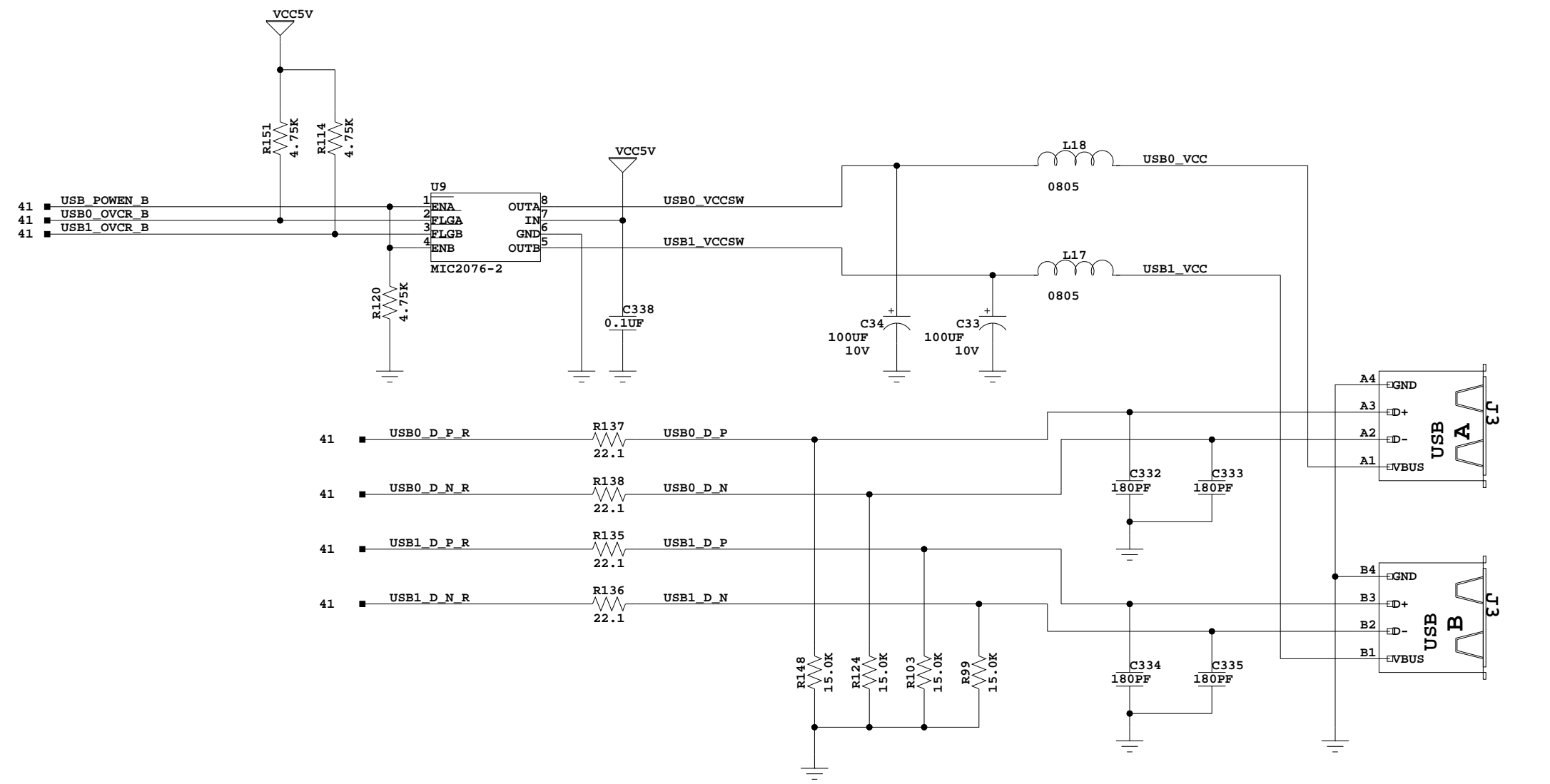
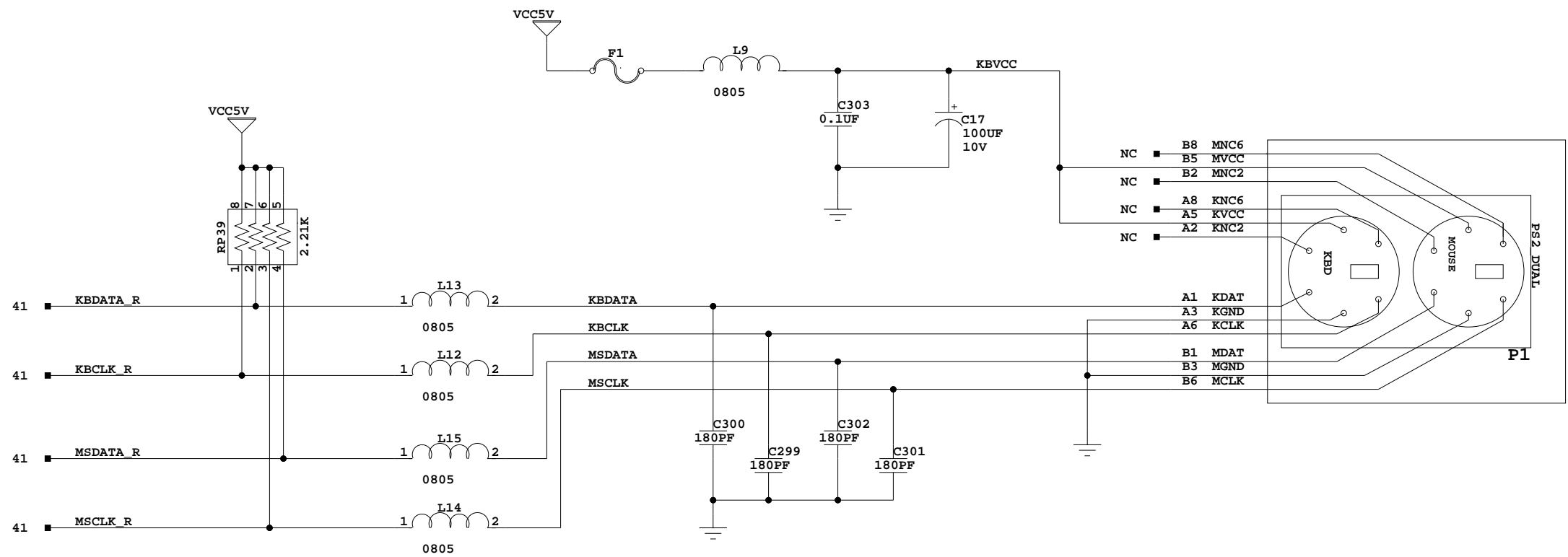
### RS232 SERIAL PORT INTERFACE



SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTRM  
RS232 SERIAL PORT INTERFACE

Date:	7-10-2008_10:19	Ver:	C
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### KBD/MOUSE AND USB INTERFACES



SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 KBD/MOUSE AND USB INTERFACES

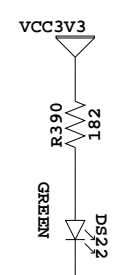
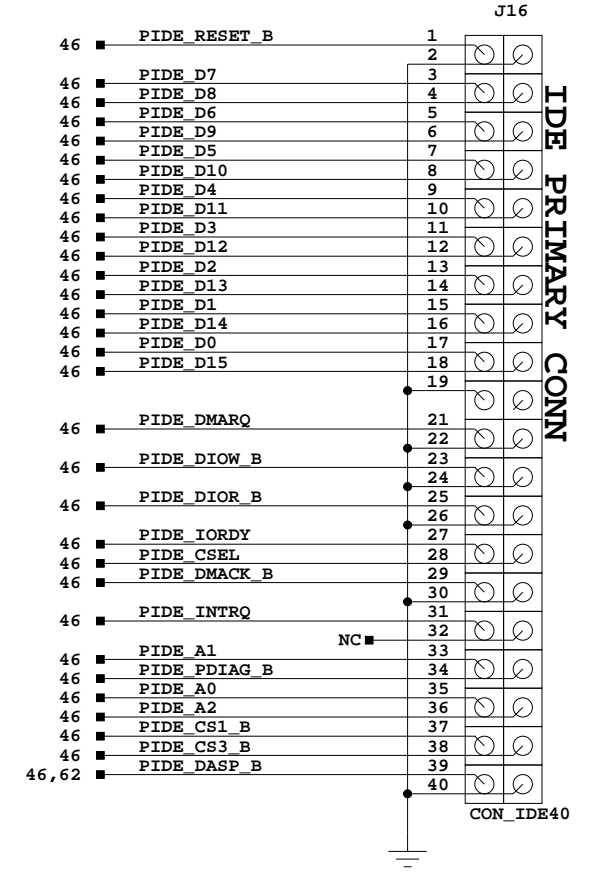
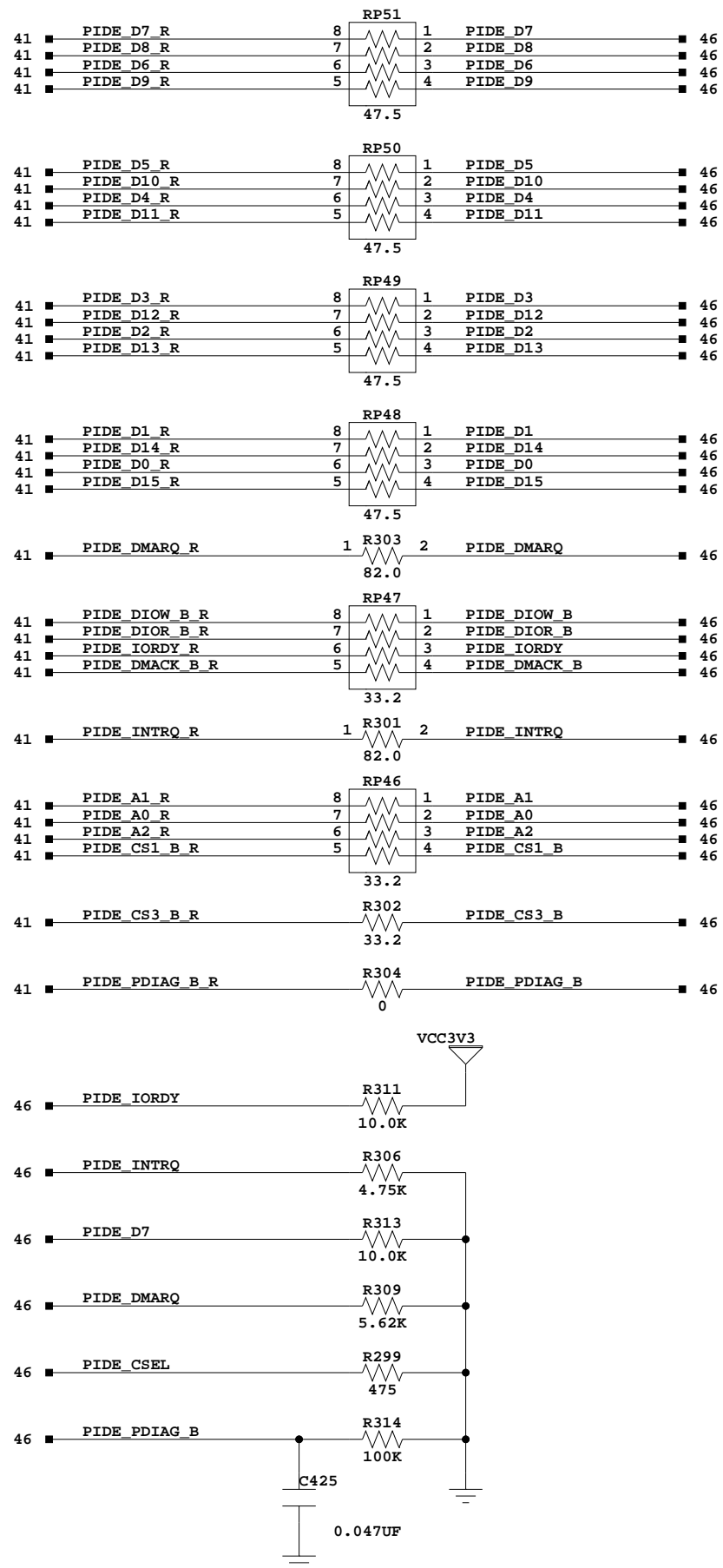
Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
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Pin 20 must be removed.  
Silkscreen:  
"IDE PRIMARY"

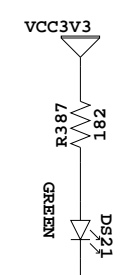
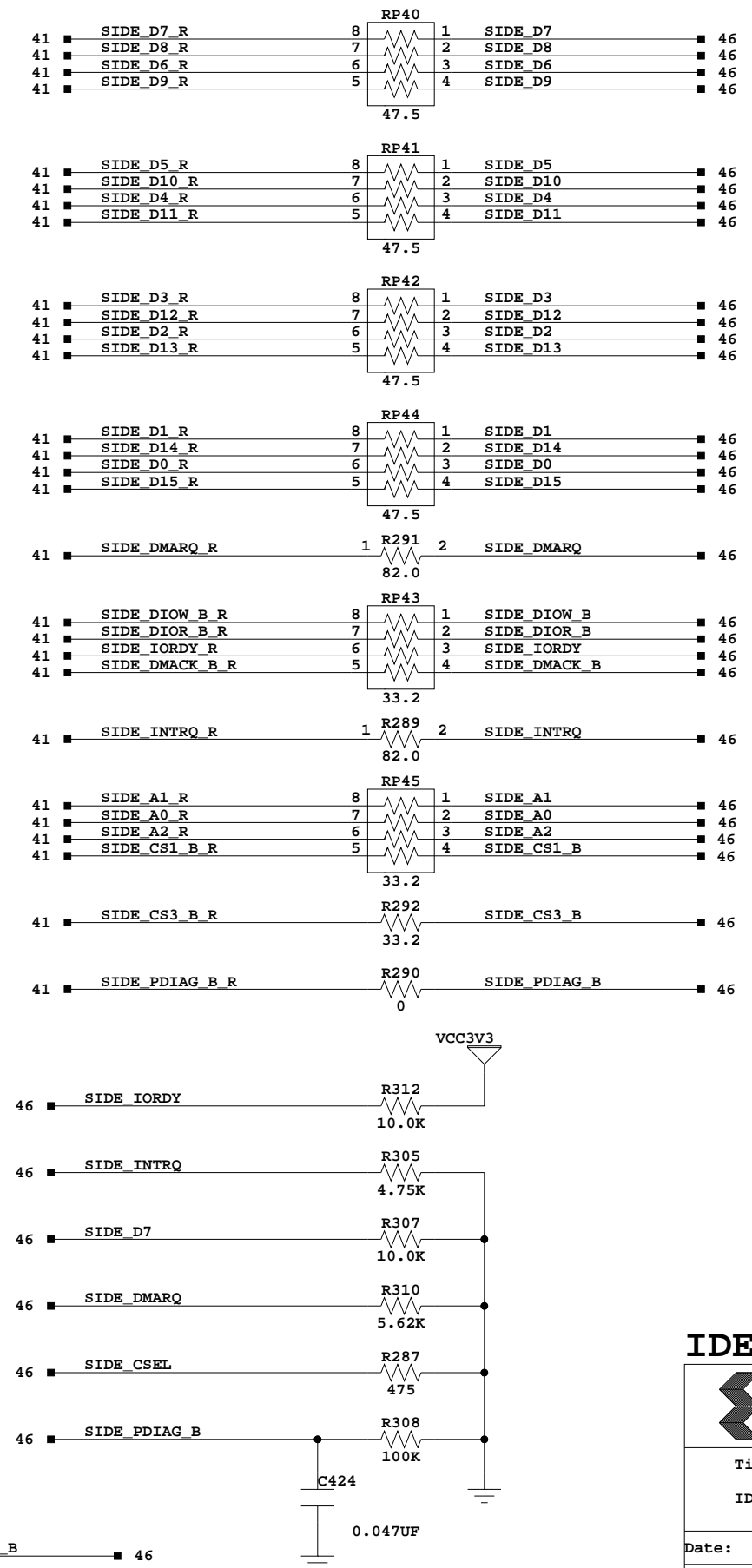
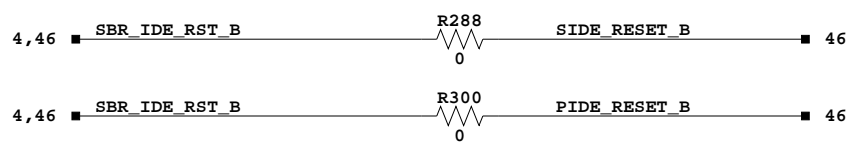
Mark Pin 1  
Pin20=Key  
J16

Pin 20 must be removed.  
Silkscreen:  
"IDE SECONDARY"

Mark Pin 1  
Pin20=Key  
J15



Silkscreen:  
"IDE P LED"



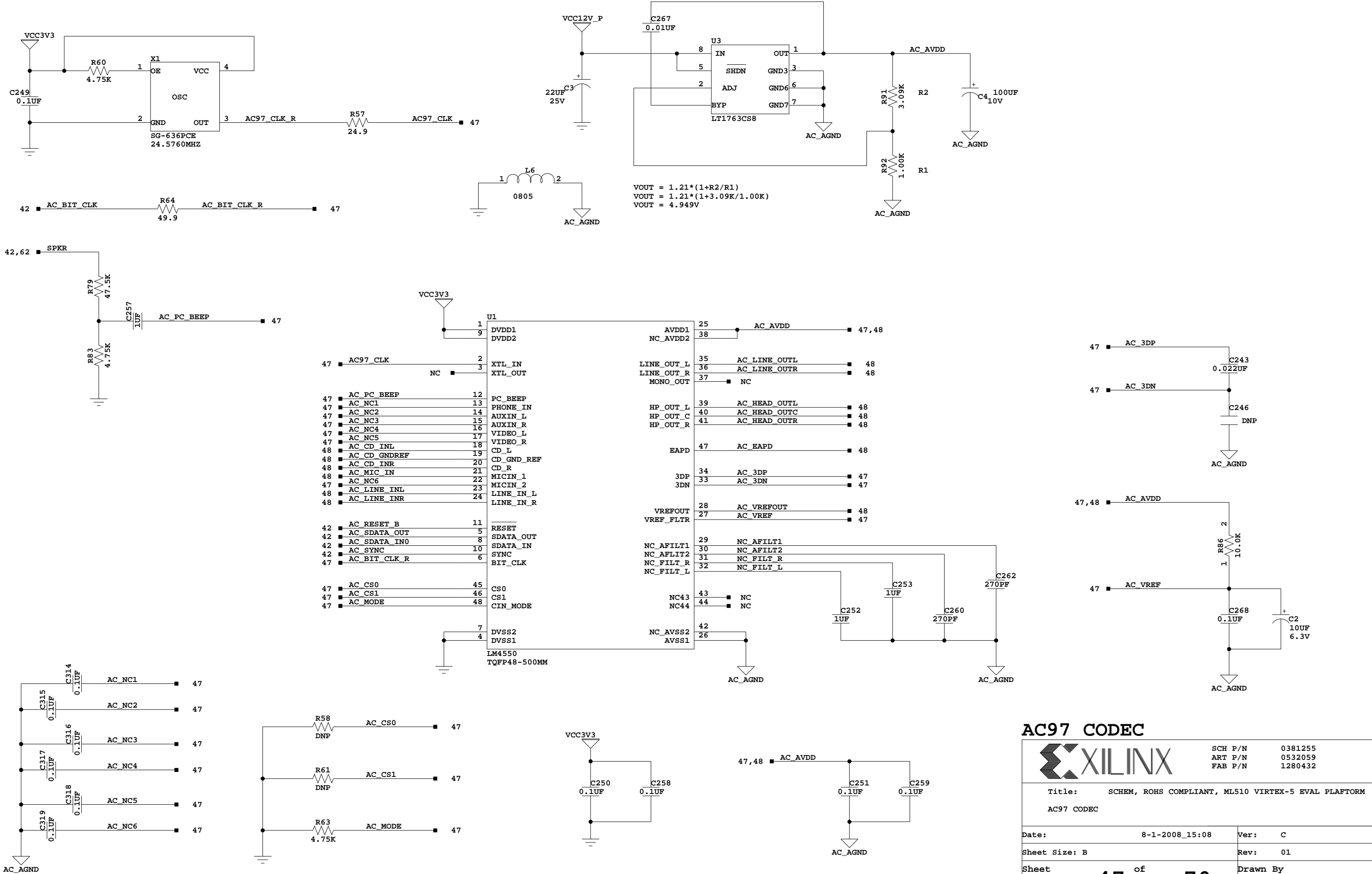
Silkscreen:  
"IDE S LED"

### IDE INTERFACES

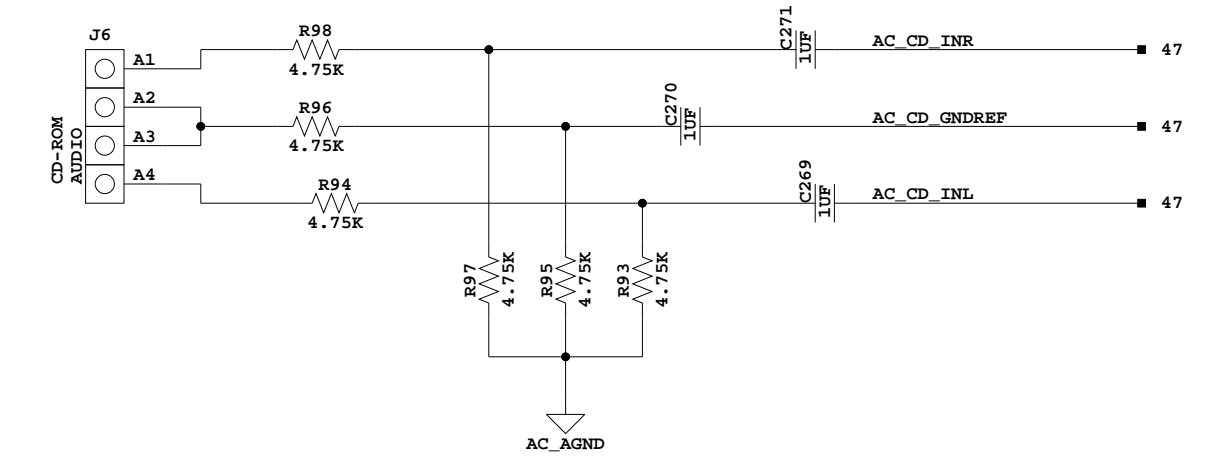
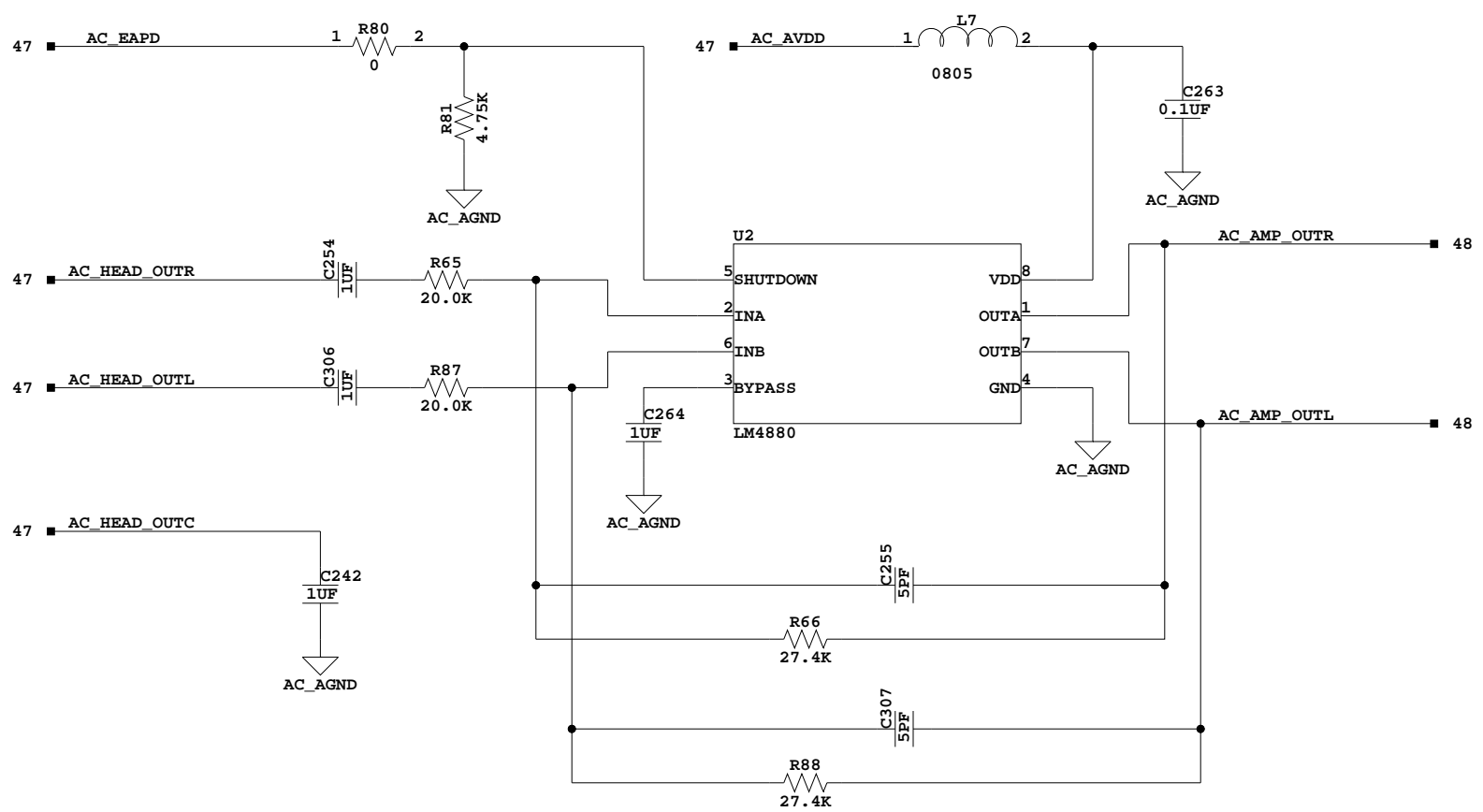
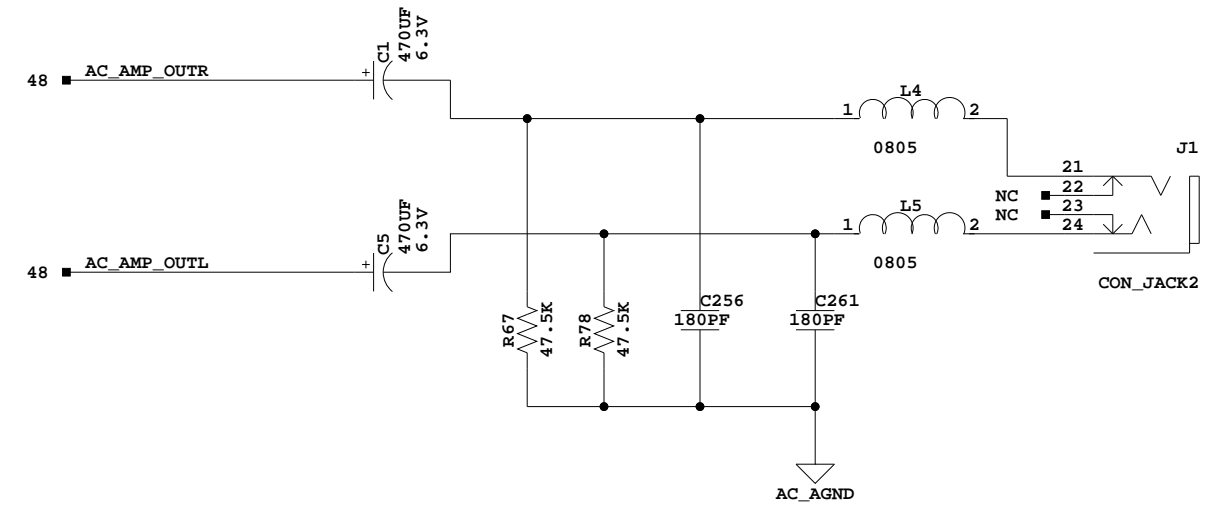
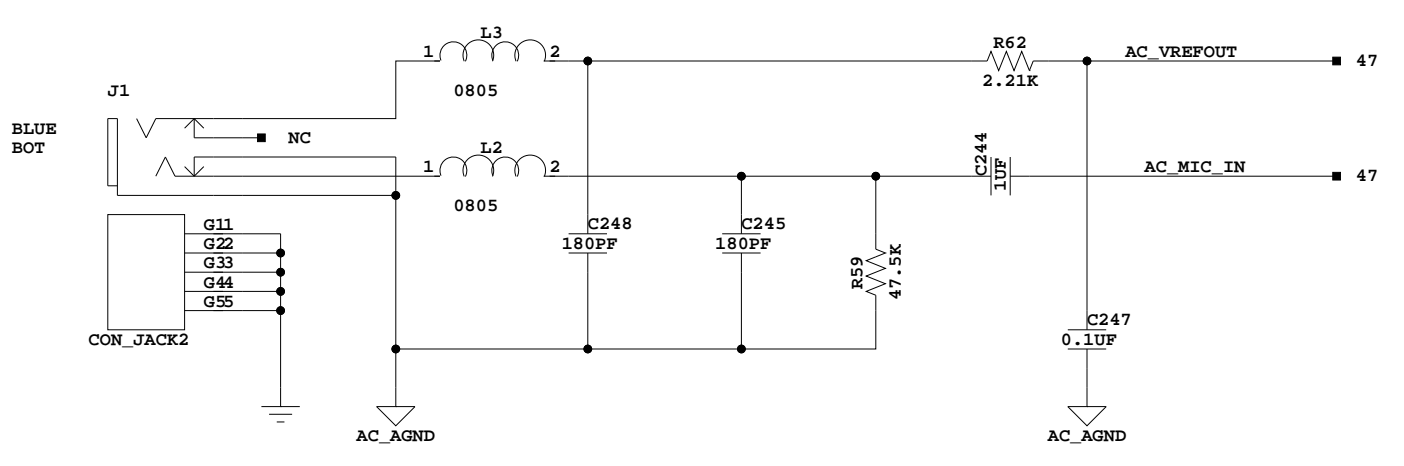
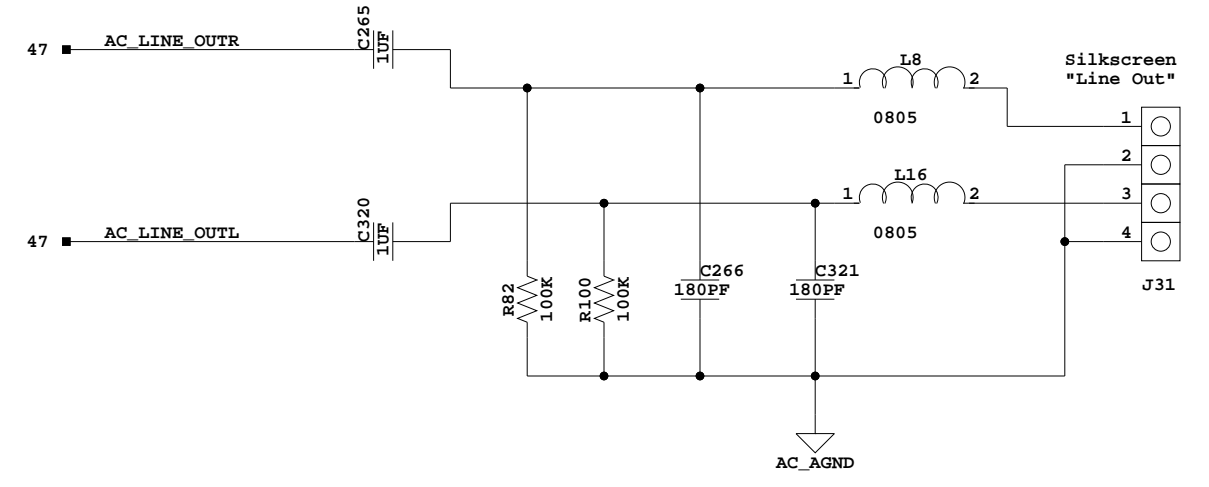
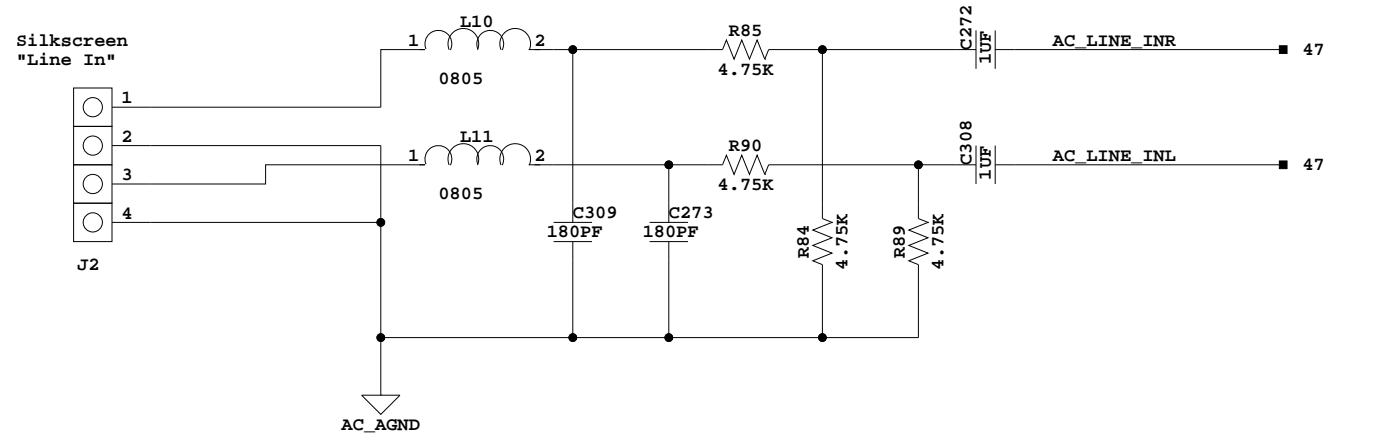


SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOM	
IDE INTERFACES	
Date: 7-10-2008_10:19	Ver: C
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AC97 CODEC		
		SCH P/N 0381255
		ART P/N 0532059
		FAB P/N 1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM		
AC97 CODEC		
Date: 8-1-2008_15:08	Ver: C	
Sheet Size: B	Rev: 01	
Sheet 47 of 70	Drawn By BF	



### AC97 CONNECTORS

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
AC97 CONNECTORS

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	48 of 70	Drawn By	BF

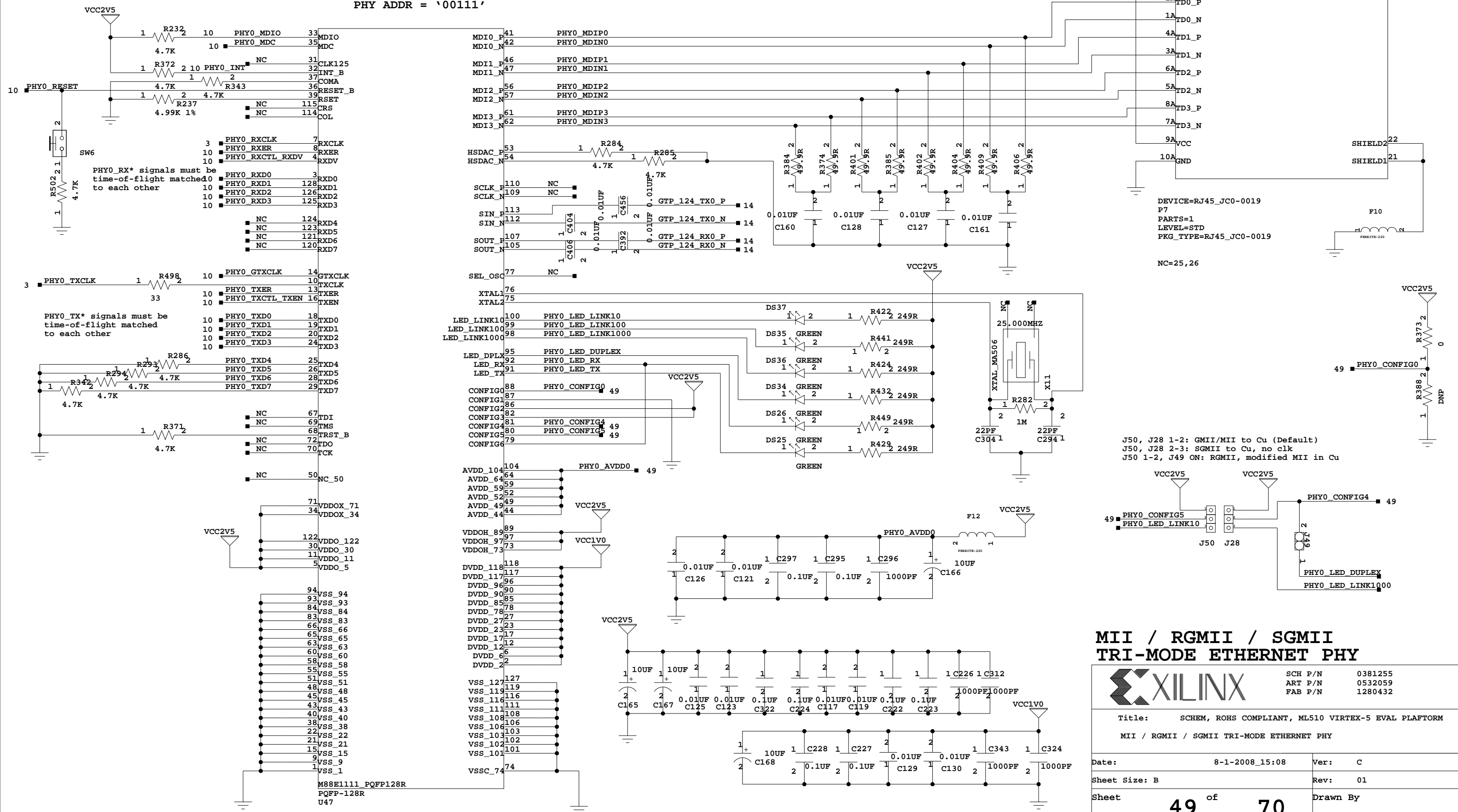


**SGMII:  
GTP 124\_0**

NOTE:  
PHY ADDR = '00111'

NOTE:  
BOTTOM SGMII

**10/100/1000  
RJ45 AND  
MAGNETICS**



DEVICE=RJ45\_JC0-0019  
P7  
PARTS=1  
LEVEL=STD  
PKG\_TYPE=RJ45\_JC0-0019  
NC=25,26

J50, J28 1-2: GMII/MII to Cu (Default)  
J50, J28 2-3: SGMII to Cu, no clk  
J50 1-2, J49 ON: RGMII, modified MII in Cu

**MII / RGMII / SGMII  
TRI-MODE ETHERNET PHY**

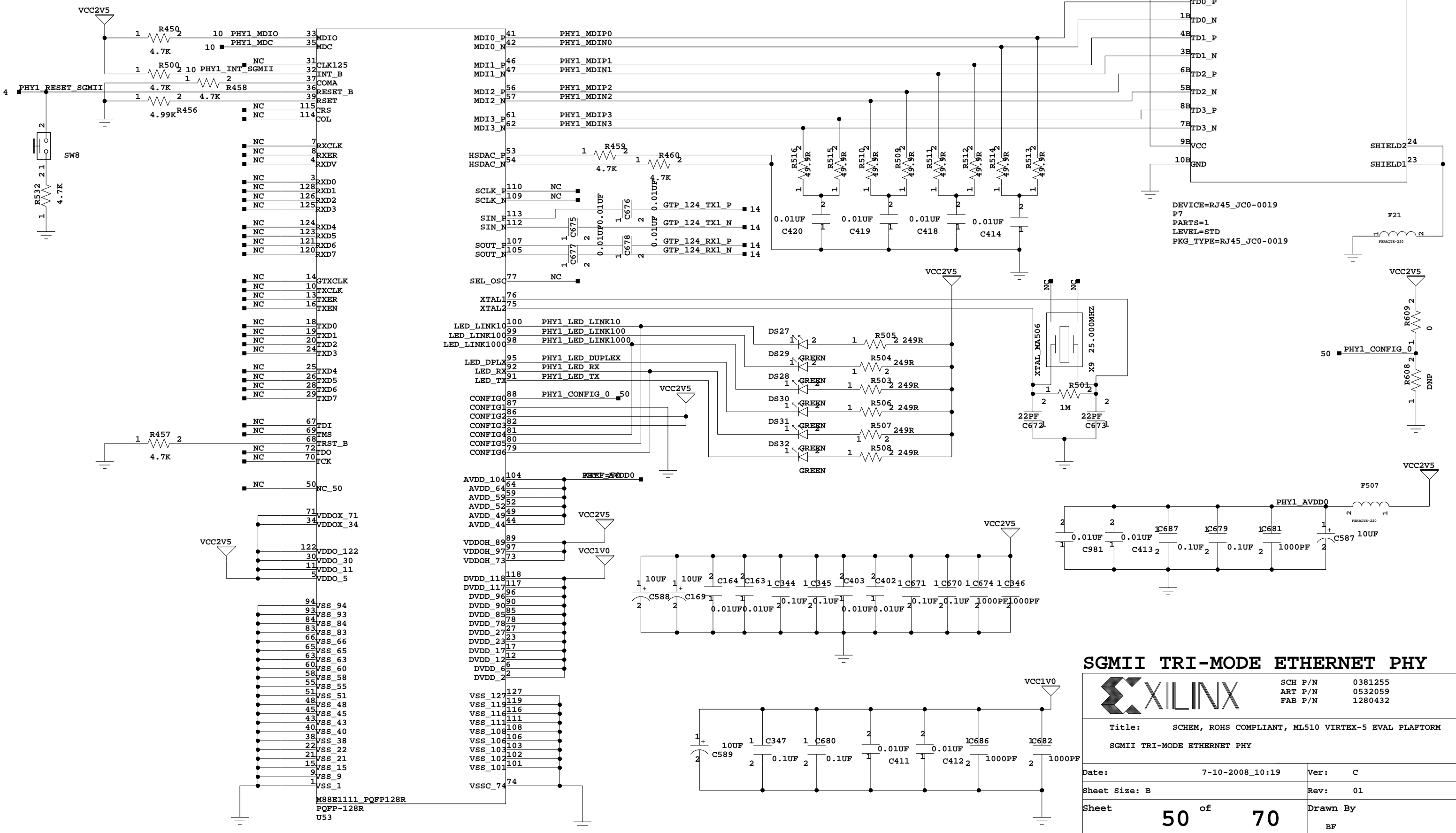
		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOM			
MII / RGMII / SGMII TRI-MODE ETHERNET PHY			
Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
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**SGMII:  
GTP 124\_1**

NOTE:  
PHY ADDR = '00111'

NOTE:  
BOTTOM SGMII

**10/100/1000  
RJ45 AND  
MAGNETICS**



DEVICE=RJ45\_JC0-0019  
P7  
PARTS=1  
LEVEL=STD  
PKG\_TYPE=RJ45\_JC0-0019

**SGMII TRI-MODE ETHERNET PHY**



SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
SGMII TRI-MODE ETHERNET PHY

Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
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# SATA Host 1

## GTP 120\_1



# SATA Host 2

## GTP 120\_0

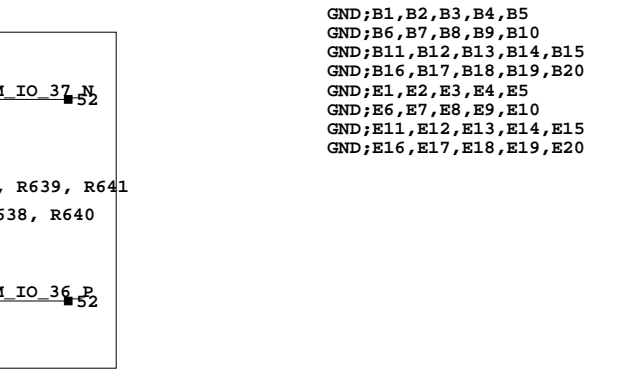
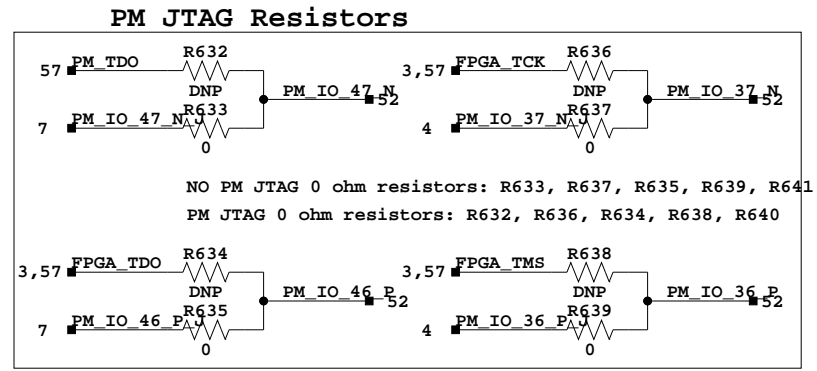
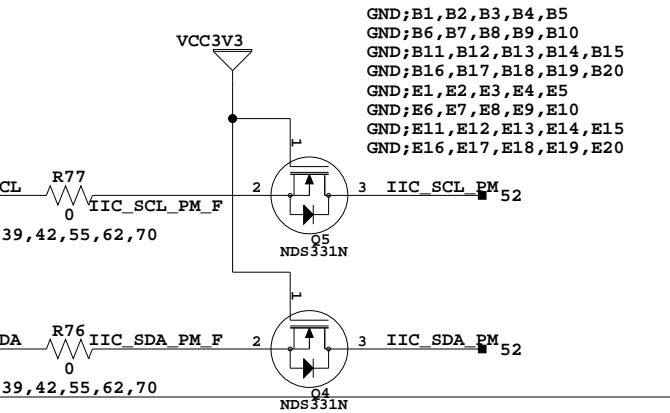
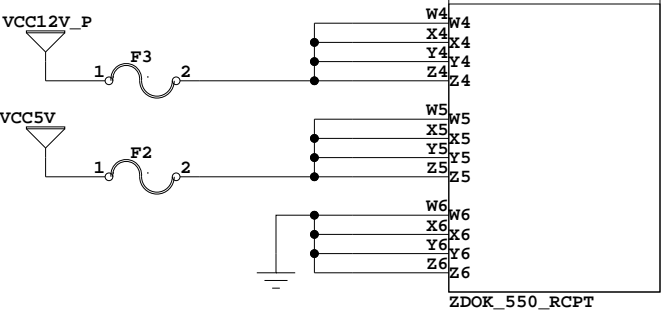
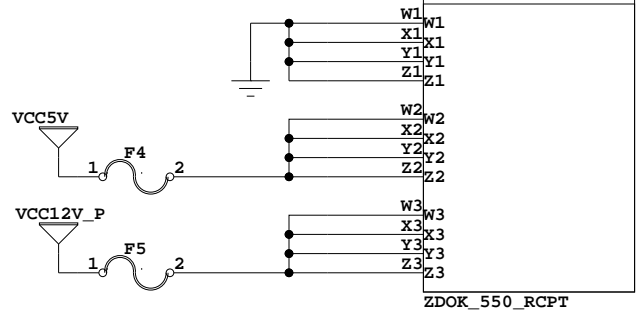
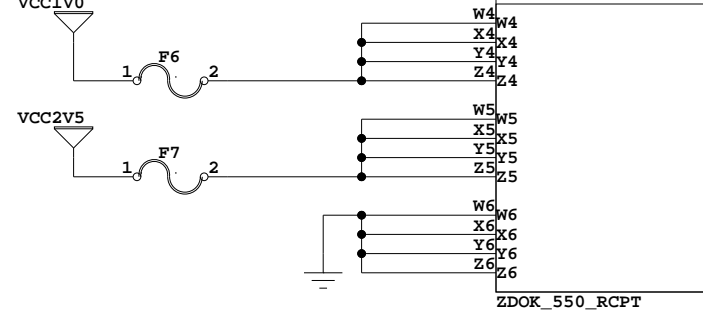
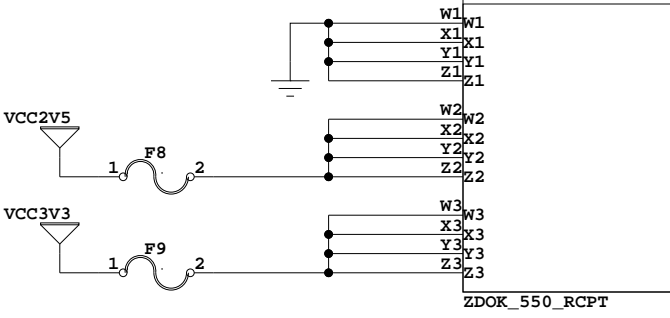
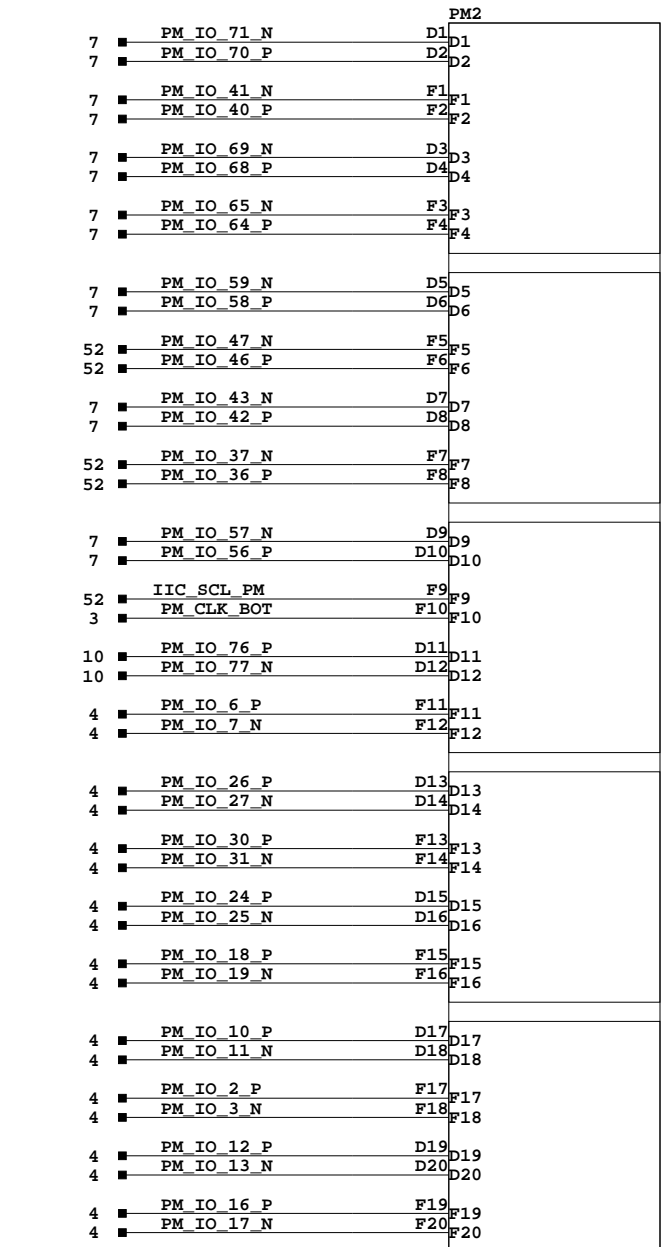
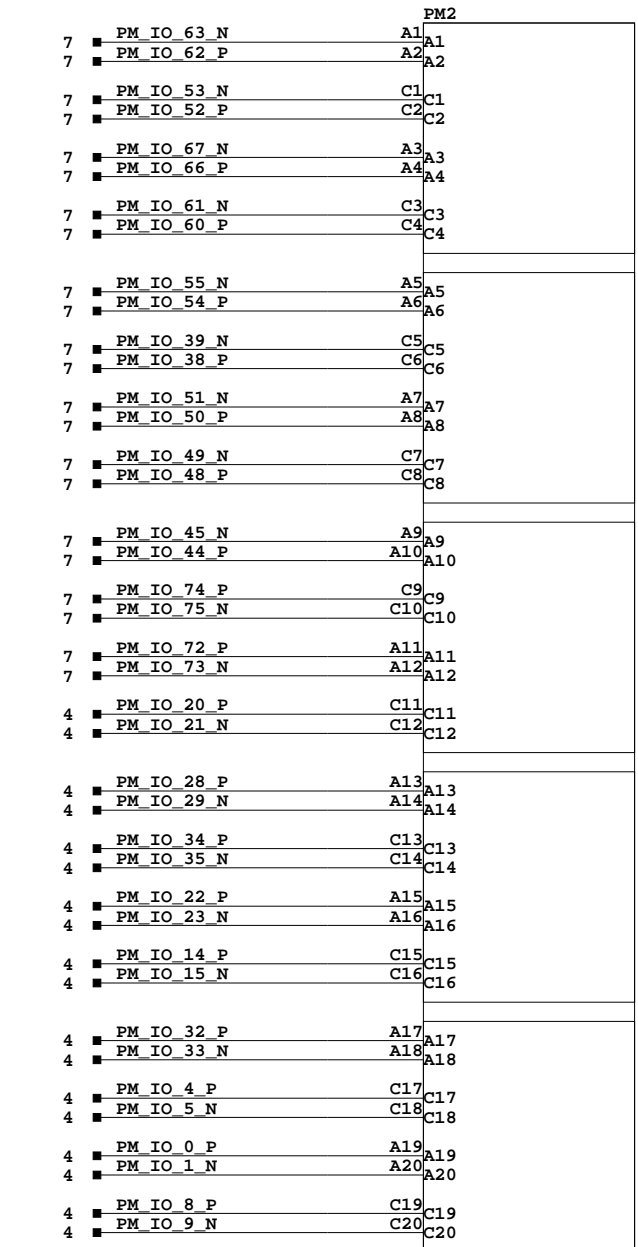
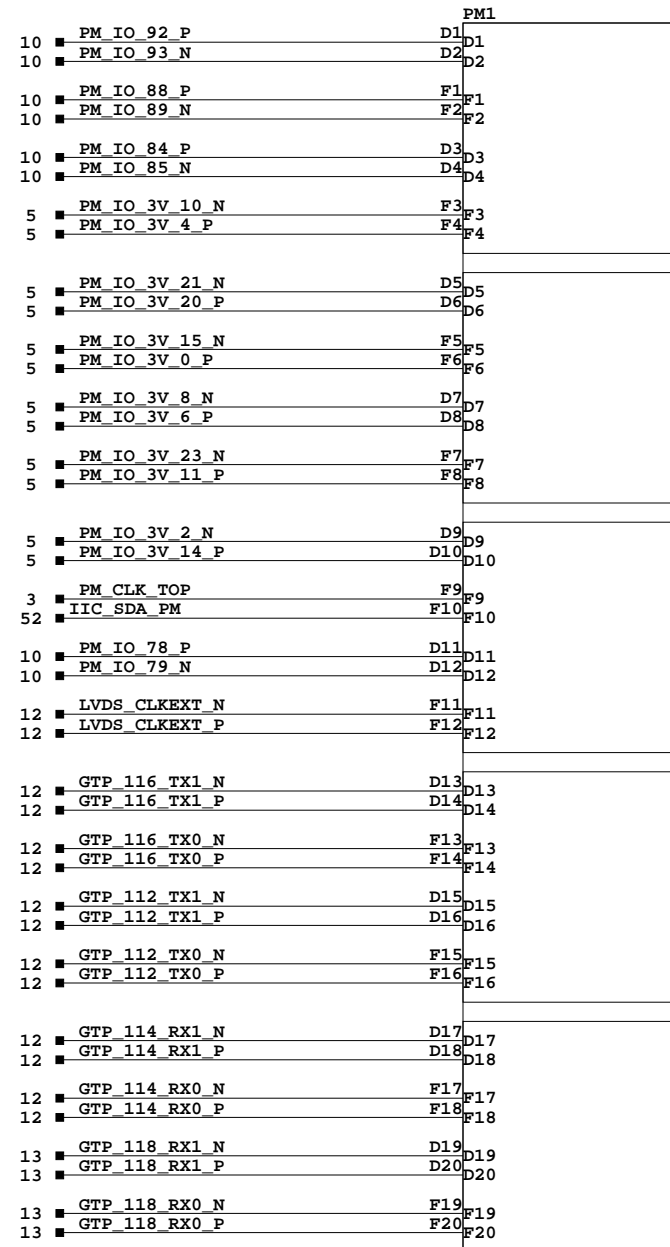
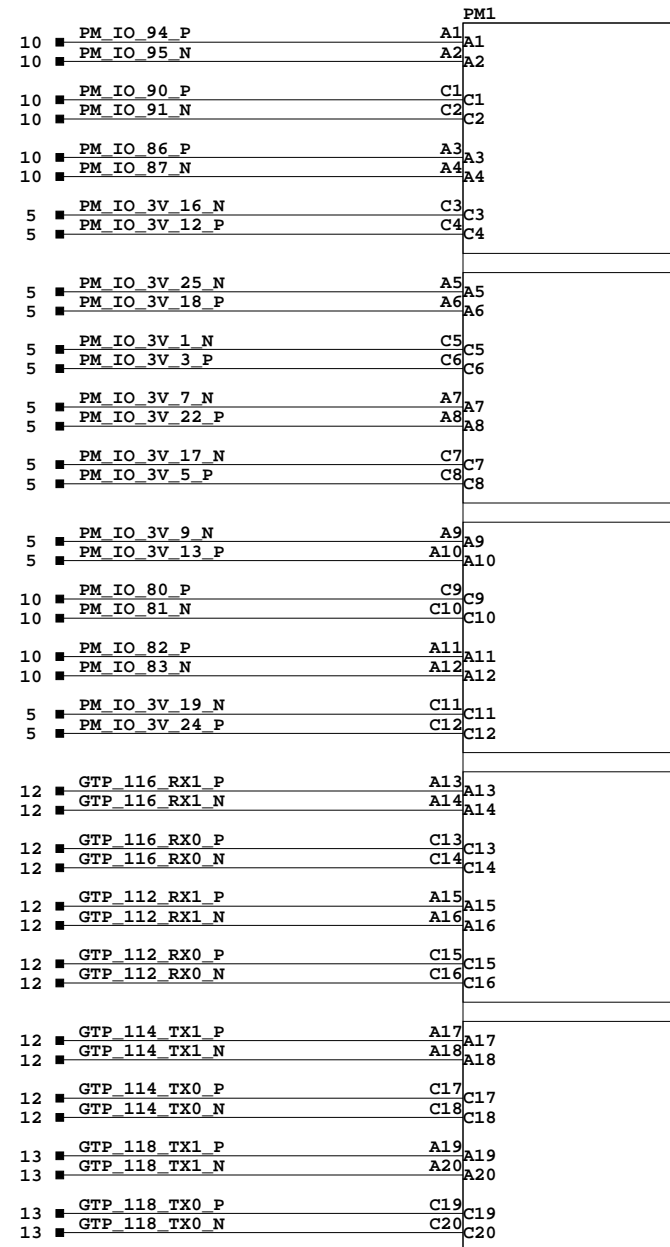


### SATA INTERFACE

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
SATA INTERFACE

Date:	7-10-2008_10:19	Ver:	C
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PERSONALITY MODULE CONNECTORS

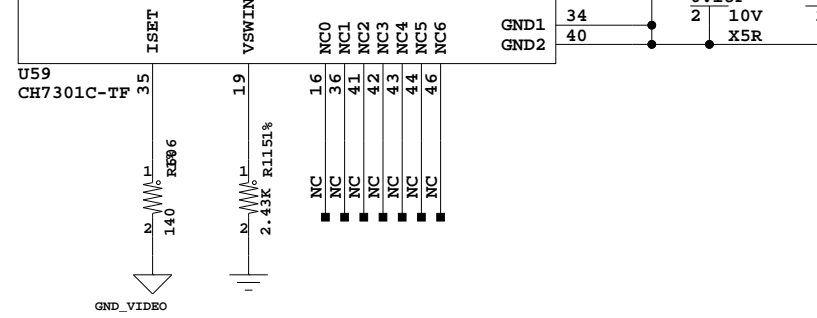
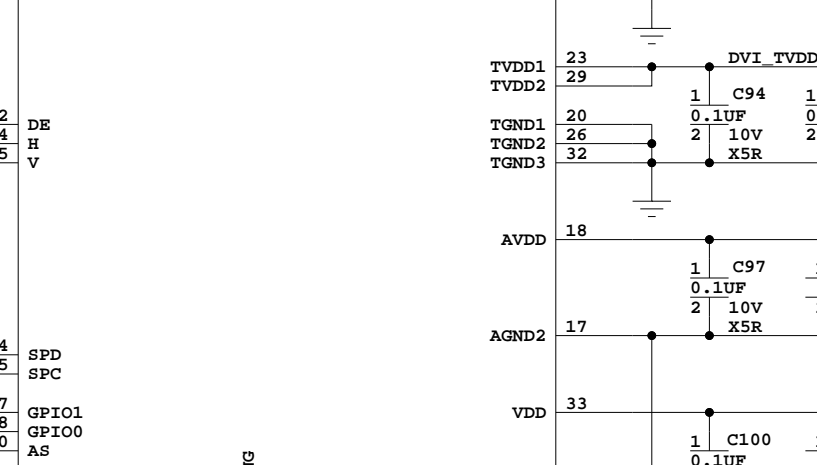
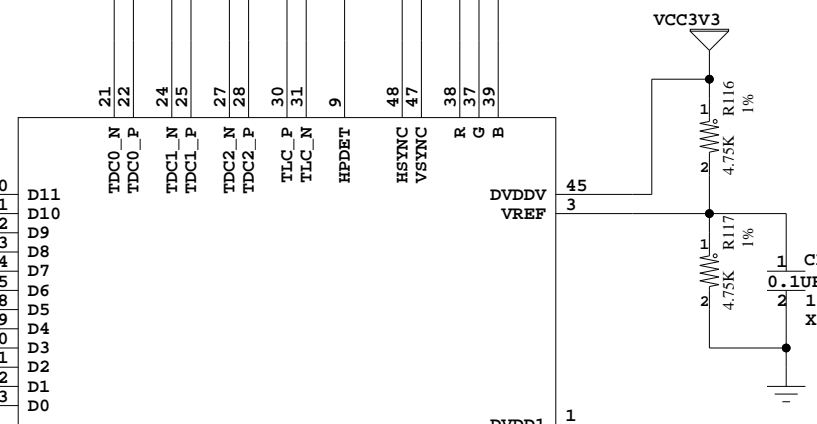
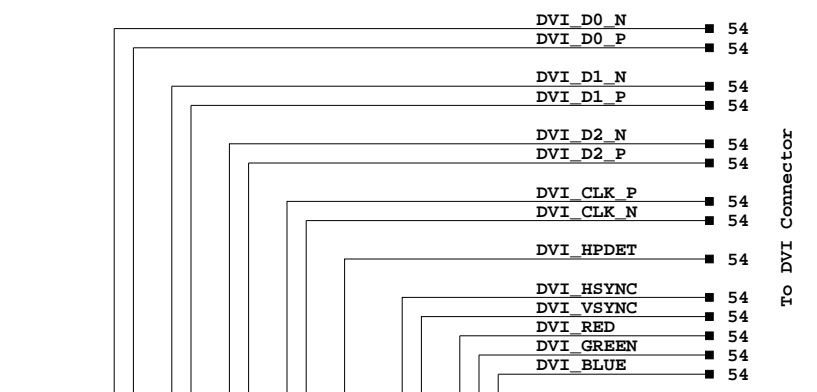
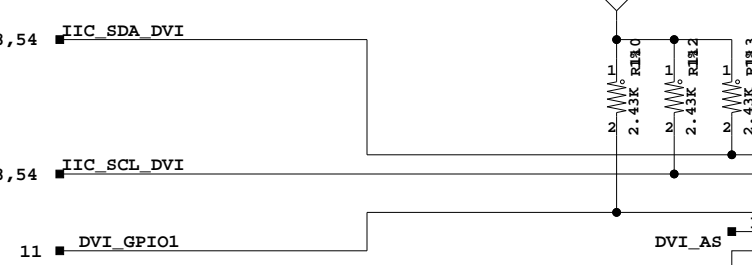
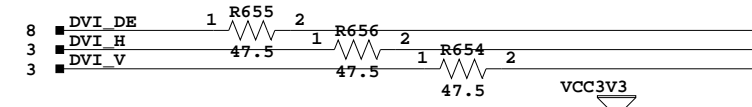
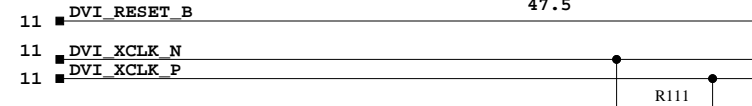
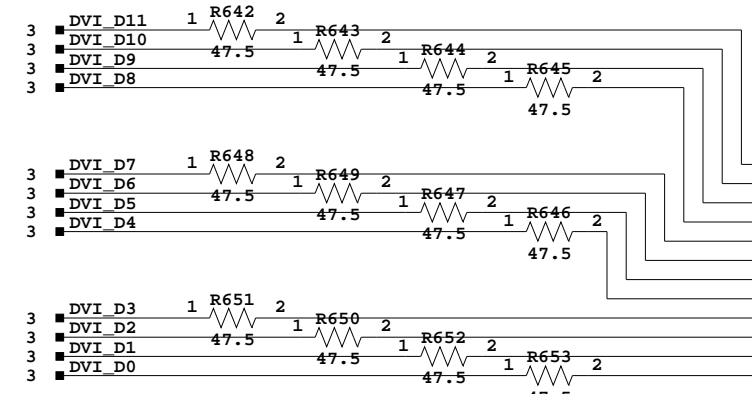


SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
PERSONALITY MODULE CONNECTORS

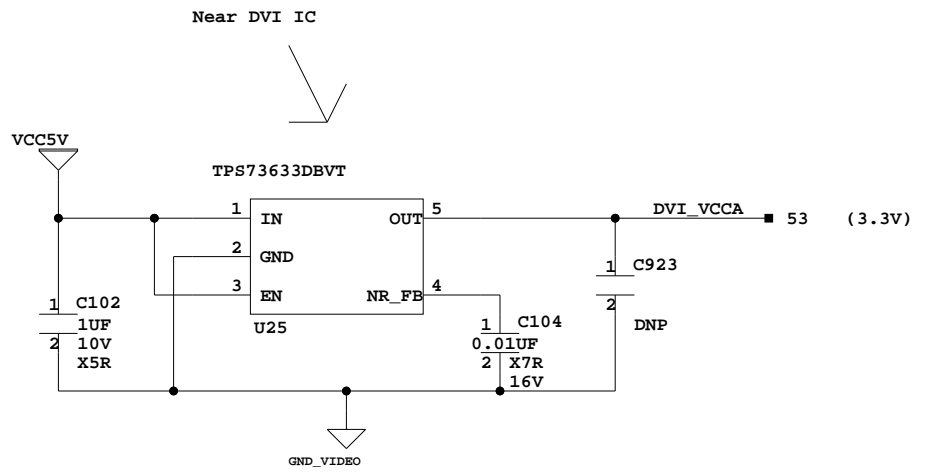
Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
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Place termination RPs near U37



IIC Address = 0x76

To DVI Connector



### DVI CODEC



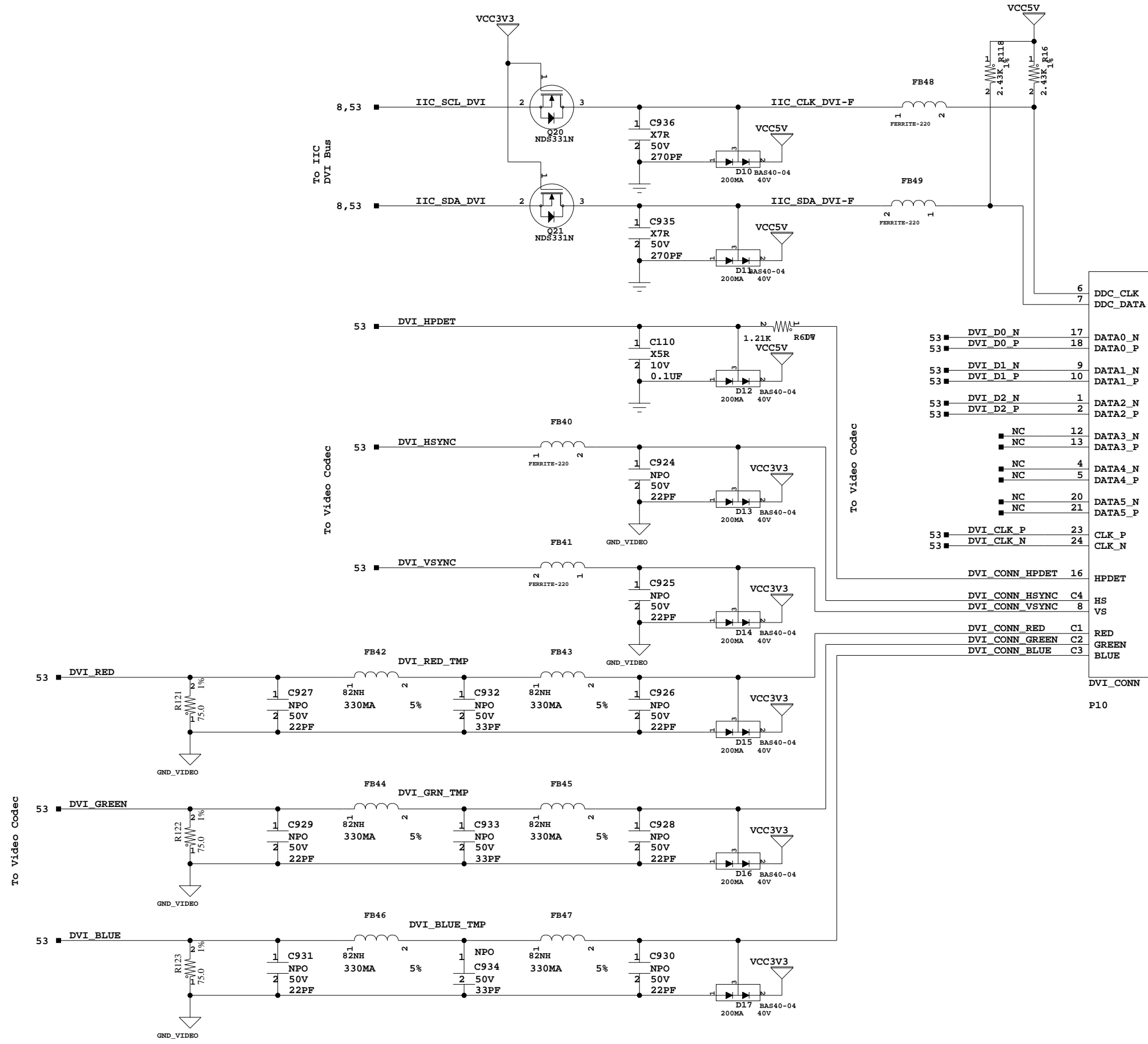
SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 DVI CODEC

Date: 8-1-2008\_15:08 Ver: C

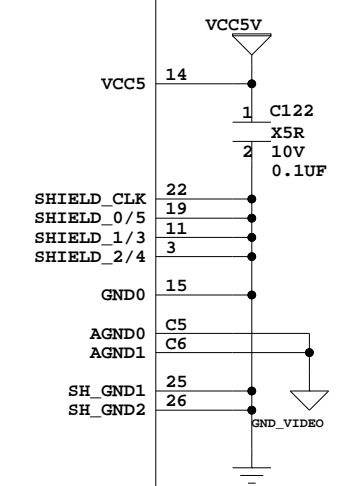
Sheet Size: B Rev: 01

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**DVI\_CONN**

6	DDC_CLK	17	DATA0_N
7	DDC_DATA	18	DATA0_P
53	DVI_D0_N	9	DATA1_N
53	DVI_D0_P	10	DATA1_P
53	DVI_D1_N	1	DATA2_N
53	DVI_D1_P	2	DATA2_P
NC	12	DATA3_N	
NC	13	DATA3_P	
NC	4	DATA4_N	
NC	5	DATA4_P	
NC	20	DATA5_N	
NC	21	DATA5_P	
53	DVI_CLK_P	23	CLK_P
53	DVI_CLK_N	24	CLK_N
	DVI_CONN_HPDET	16	HPDET
	DVI_CONN_HSYNC	C4	HS
	DVI_CONN_VSYNC	8	VS
	DVI_CONN_RED	C1	RED
	DVI_CONN_GREEN	C2	GREEN
	DVI_CONN_BLUE	C3	BLUE



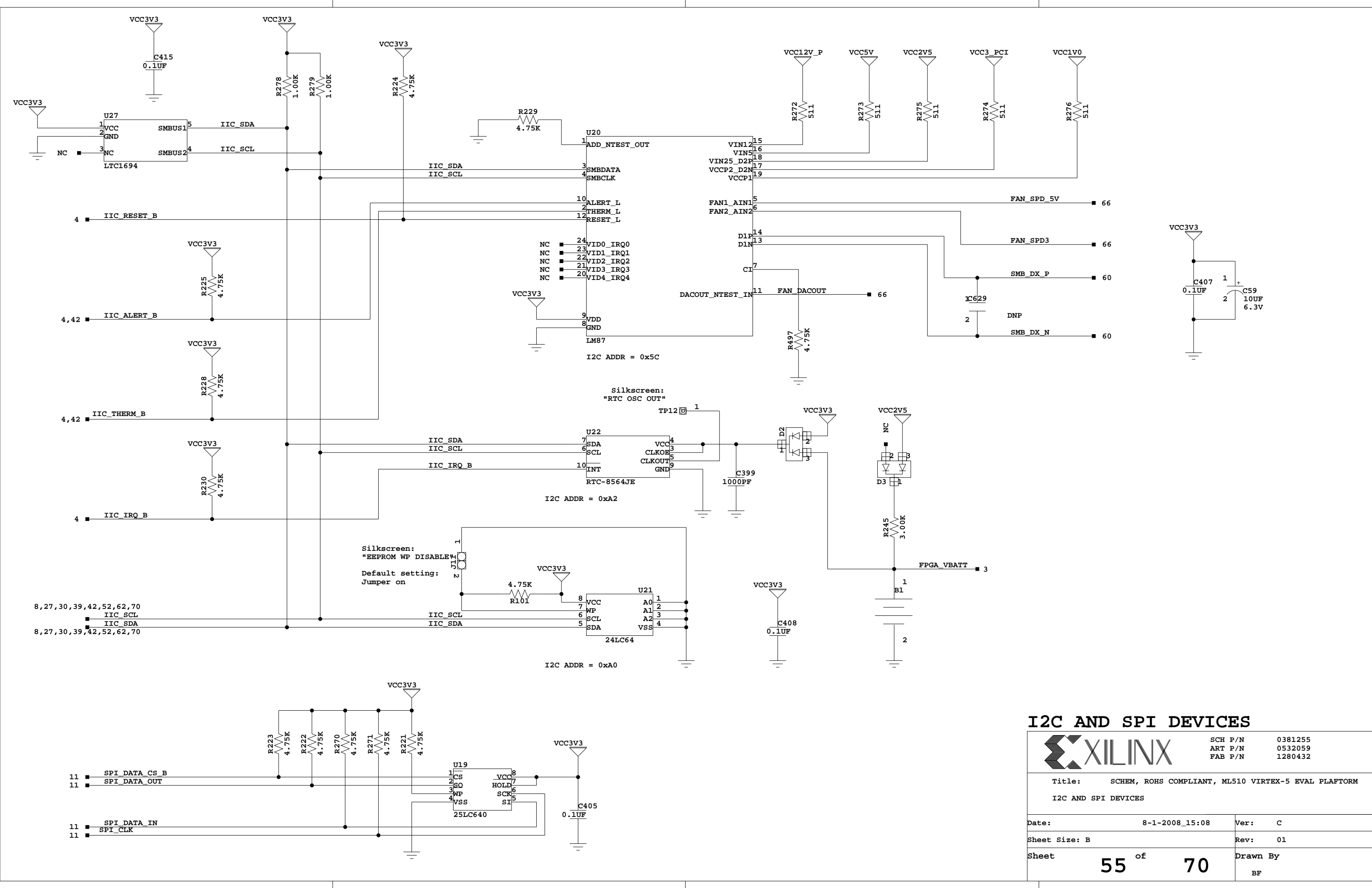
**DVI VIDEO CONNECTOR**




SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFRTORM  
 DVI VIDEO CONNECTOR

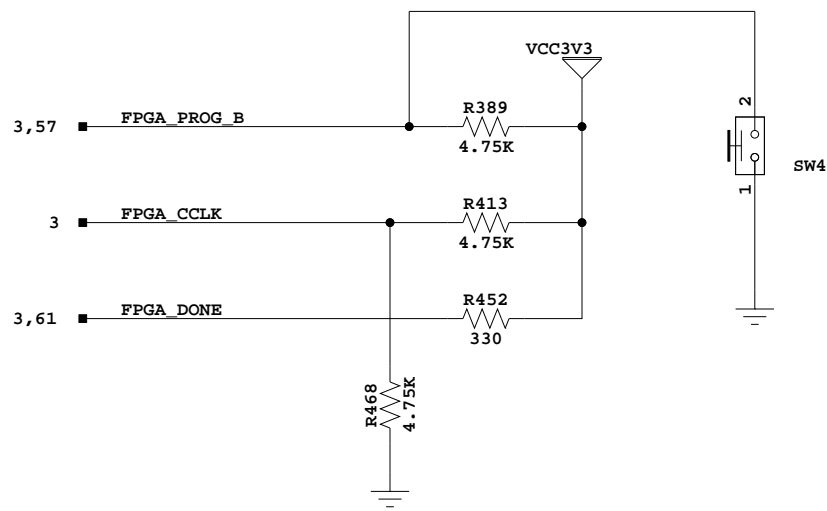
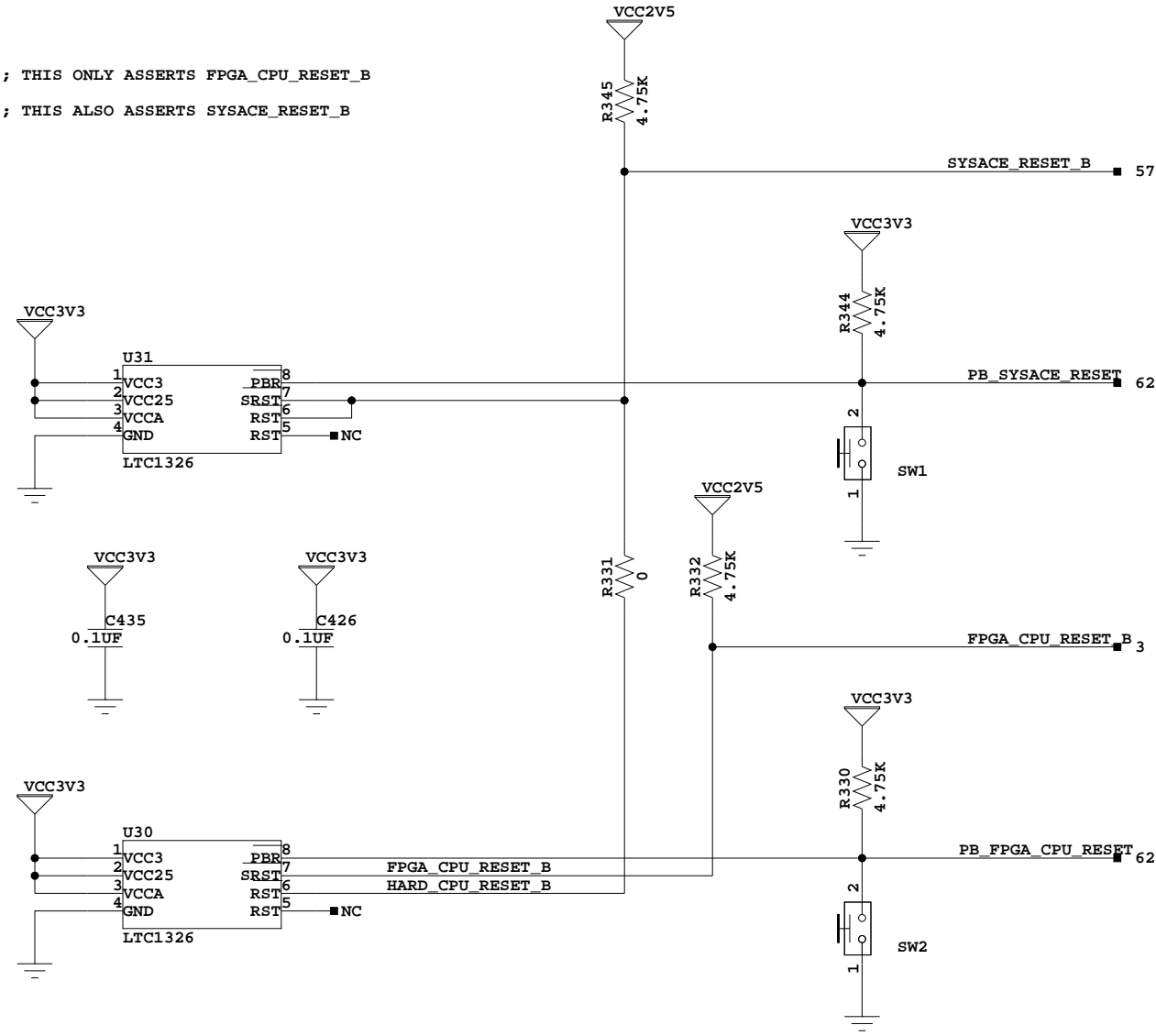
Date:	7-10-2008_10:19	Ver:	C
Sheet Size:	B	Rev:	01
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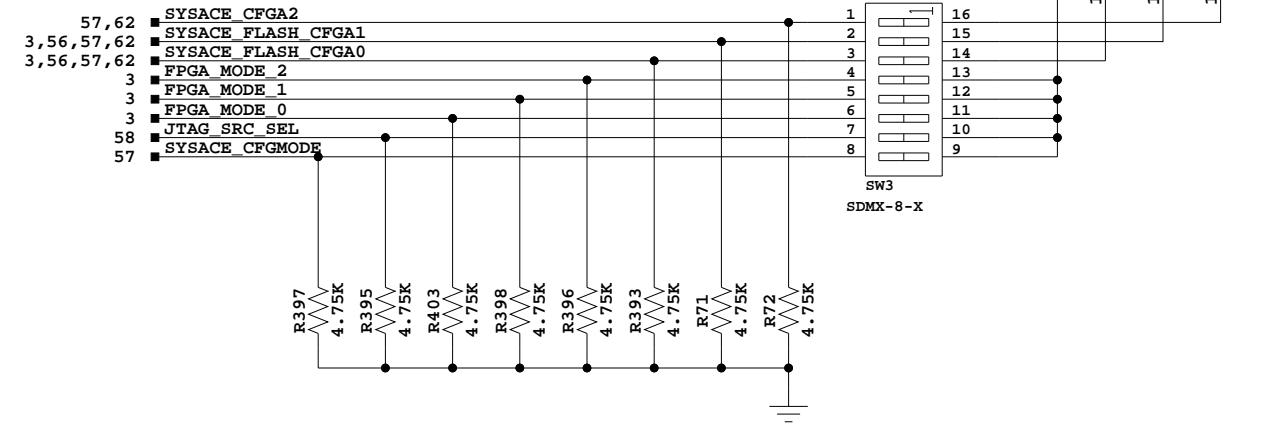
### I2C AND SPI DEVICES

		SCH P/N	0381255
		ART P/N	0532059
		FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM I2C AND SPI DEVICES			
Date:	8-1-2008_15:08	Ver:	C
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IF SW2 PRESSED < 2S; THIS ONLY ASSERTS FPGA\_CPU\_RESET\_B  
 IF SW2 PRESSED > 2S; THIS ALSO ASSERTS SYSACE\_RESET\_B

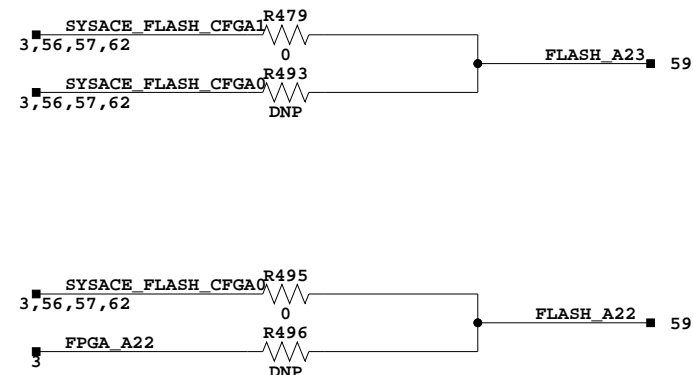


Strong pullups required because RS drives 0  
 During Fallback configuration mode



	FPGA (U37) BPI Addr Pin	Schematic Net Name	Net Connection After Jumpering	Parallel Flash (U43) Addr Pin	
4 x 64 Mbit Revisions	RS1 (U37.AK12)	SYSAC_FLASH_CFG1	FLASH_A23	R479-0ohm; R493-DNP	A24 (U43.26)
	RS0 (U37.AK13)	SYSAC_FLASH_CFG0	FLASH_A22	R495-0ohm; R496-DNP	A23 (U43.9)
	A22 (U37.AK14)	FPGA_A22	no connect		no connect
2 x 128 Mbit Revisions	RS1 (U37.AK12)	SYSAC_FLASH_CFG1	no connect	R479-DNP; R493-0ohm	no connect
	RS0 (U37.AK13)	SYSAC_FLASH_CFG0	FLASH_A23	R495-DNP; R496-0ohm	A24 (U43.26)
	A22 (U37.AK14)	FPGA_A22	FLASH_A22		A23 (U43.9)
Any Address Mode	A[21:0] (U37)	FLASH_A[21:0]	FLASH_A[21:0] N/A	A[22:1] (U43)	

Note: See the ML510 User Guide for more details about BPI Flash



## FPGA CONFIG, RESET, AND MISC I/O

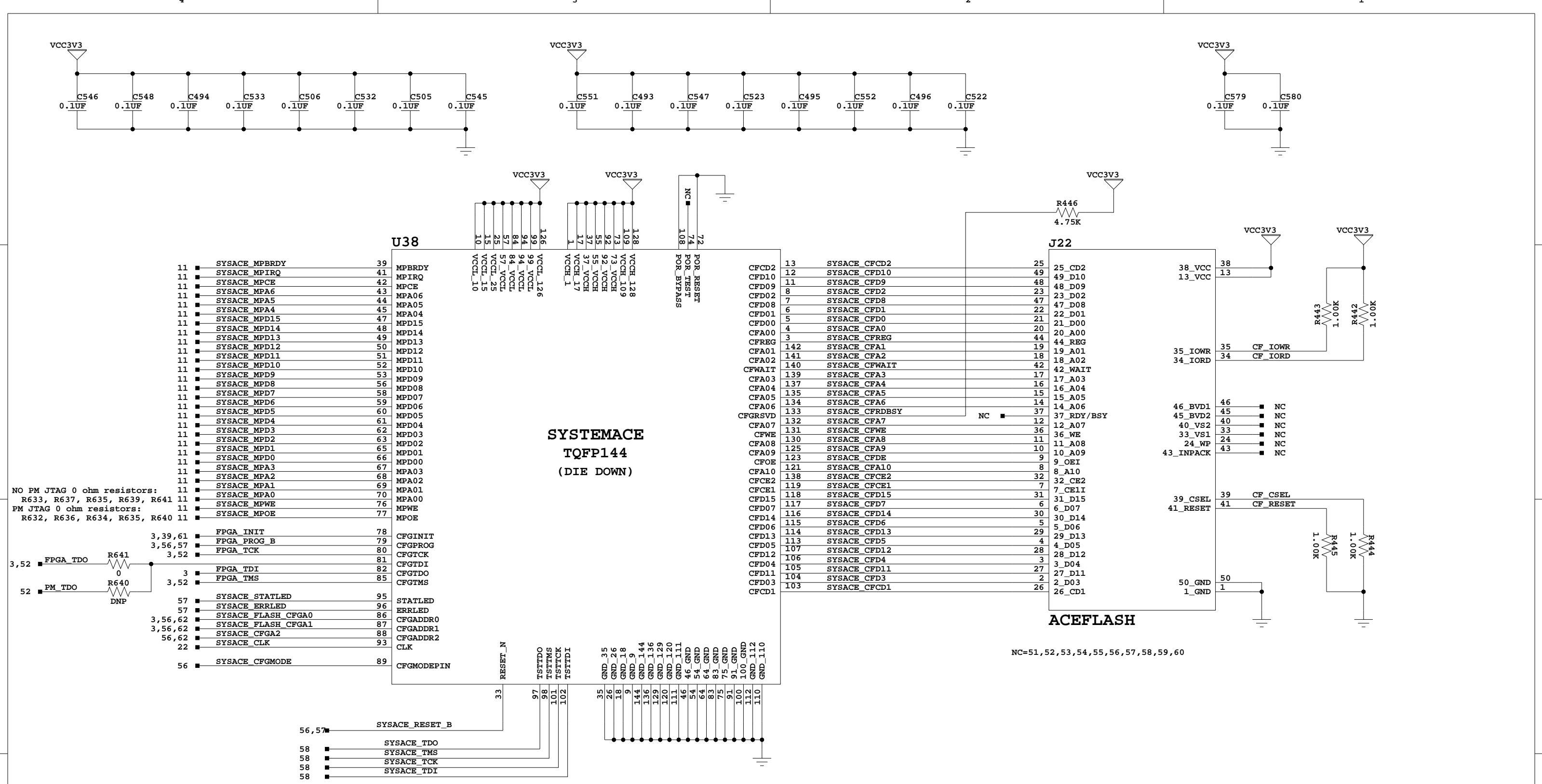


SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

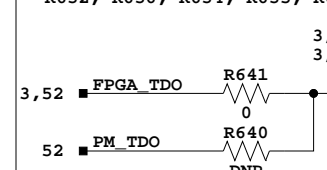
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 FPGA CONFIG, RESET, AND MISC I/O

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NO PM JTAG 0 ohm resistors:  
R633, R637, R635, R639, R641  
PM JTAG 0 ohm resistors:  
R632, R636, R634, R635, R640



# SYSTEM ACE AND COMPACT FLASH



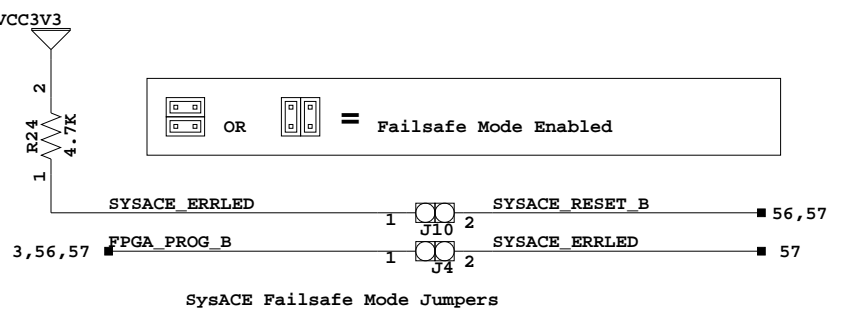
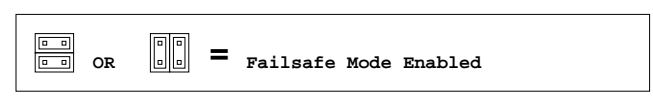
SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOM  
SYSTEM ACE AND COMPACT FLASH

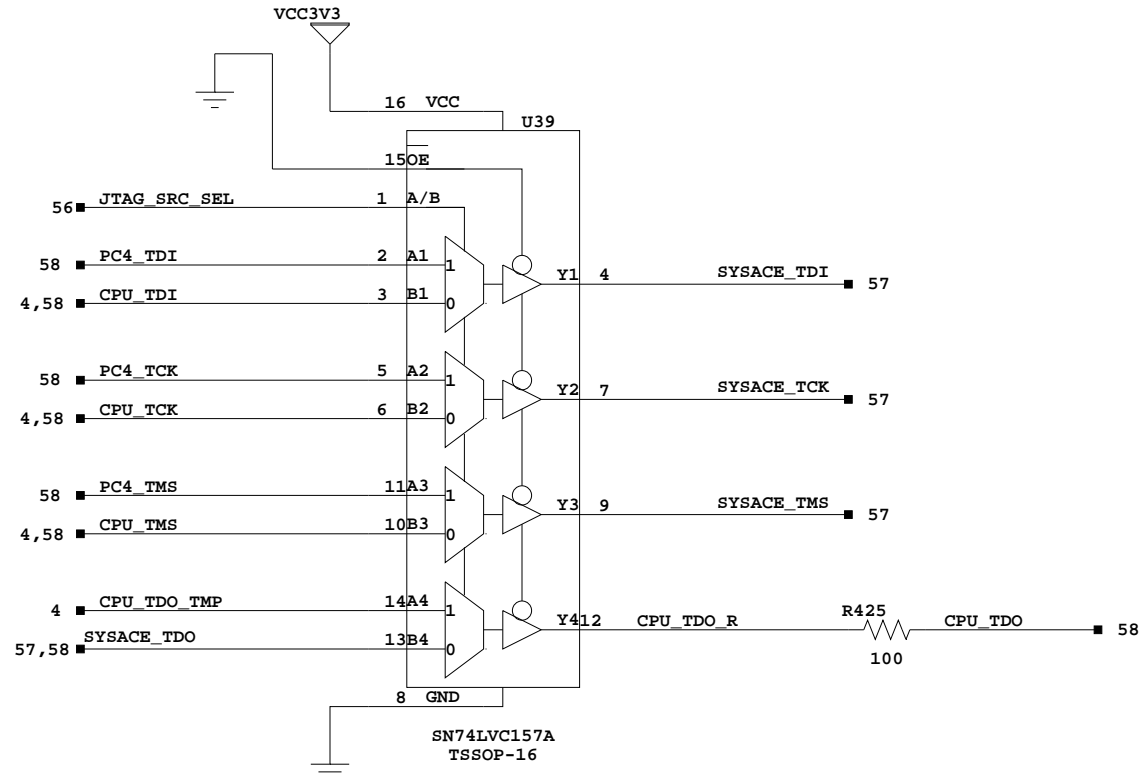
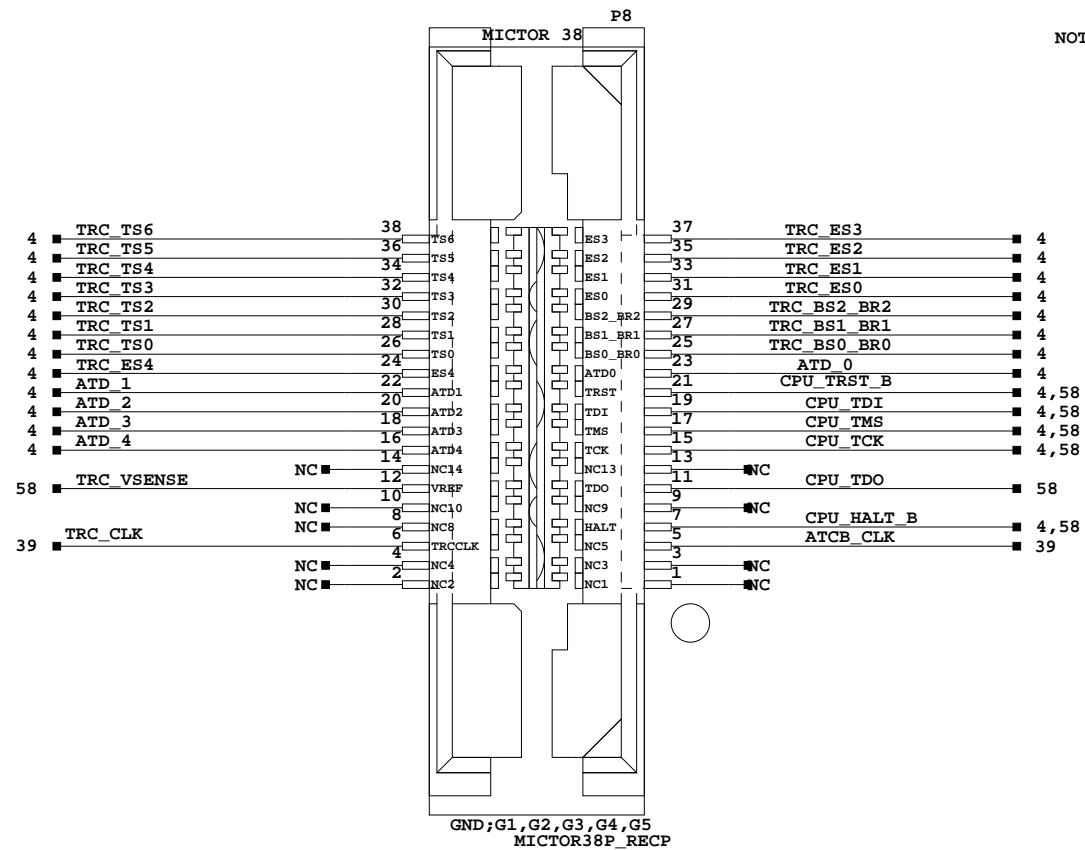
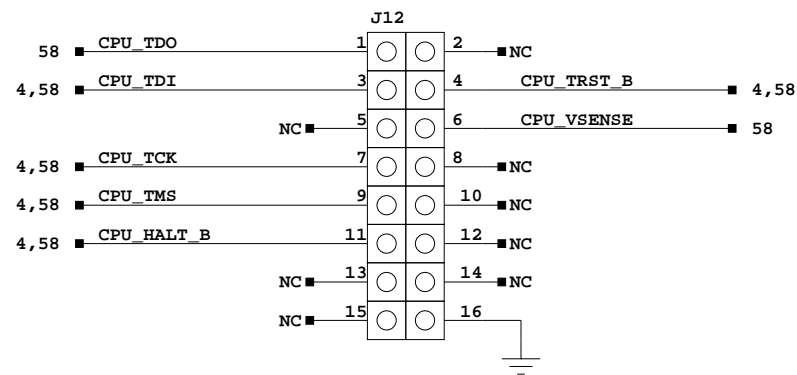
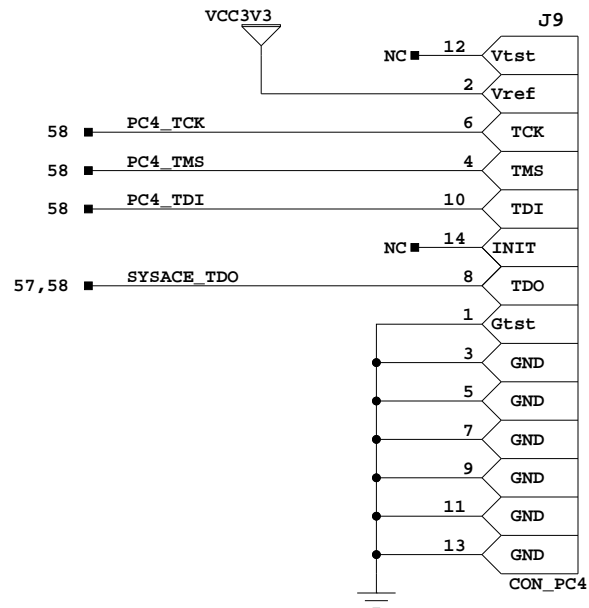
Date: 7-10-2008\_10:19 Ver: C

Sheet Size: B Rev: 01

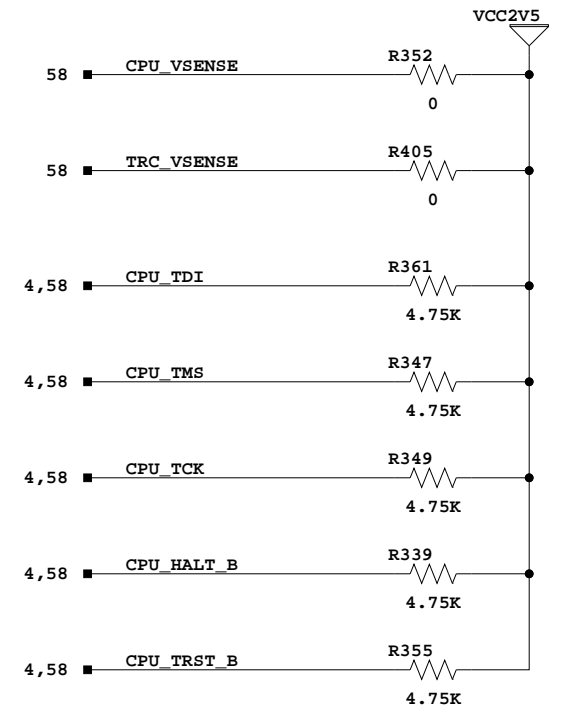
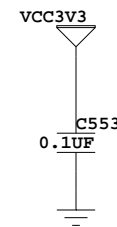
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SysACE Failsafe Mode Jumpers



NOTE: THIS MUX INTRODUCES AN IMPLICIT 2.5V TO 3.3V LEVEL-SHIFT FOR THE CPU JTAG SIGNALS. THE SERIES RESISTOR ON CPU\_TDO IS INTENDED TO PROVIDE PROTECTION FOR A 2.5V JTAG PROBE.



### JTAG, DEBUG, TRACE CONNECTORS

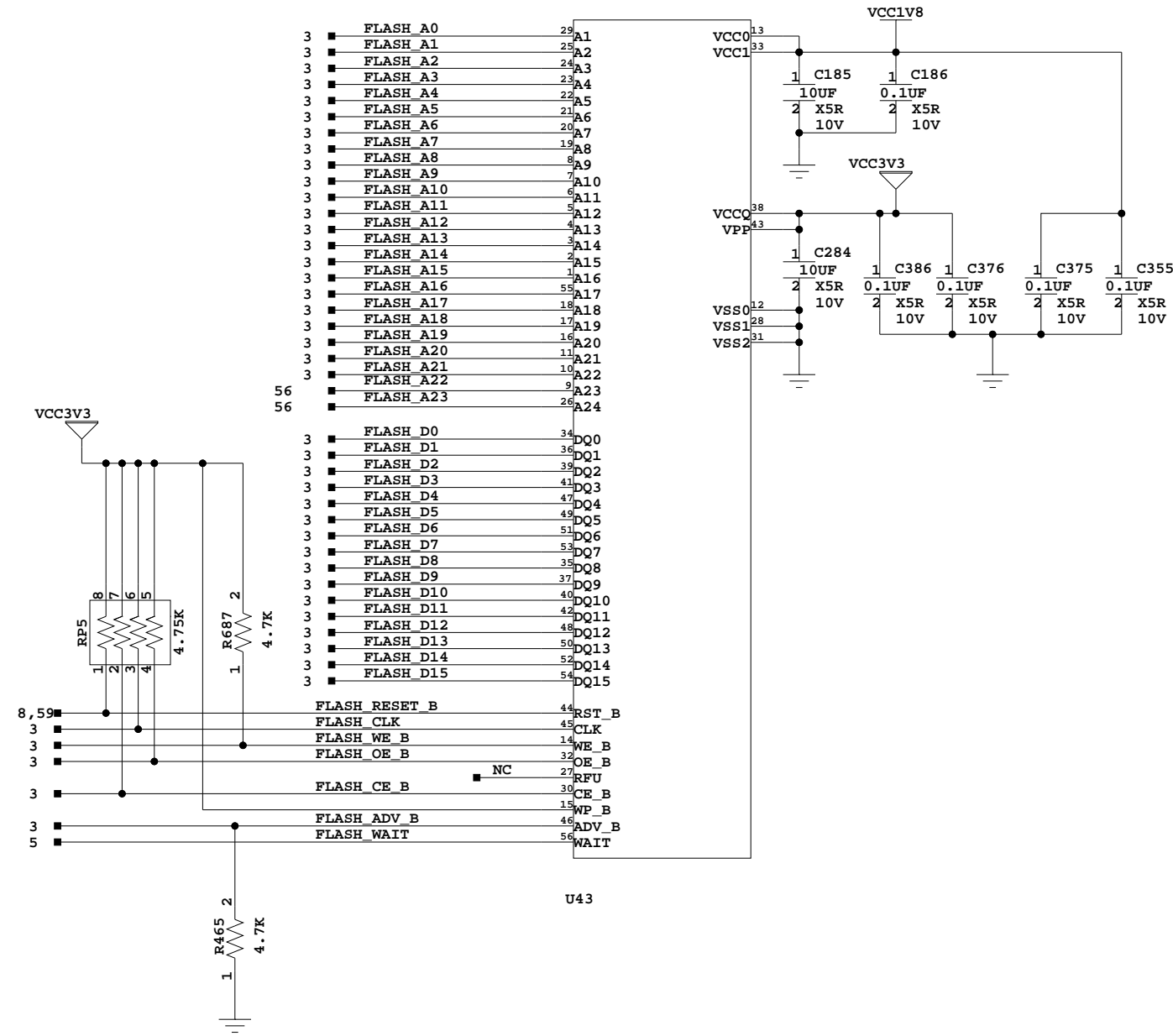


SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

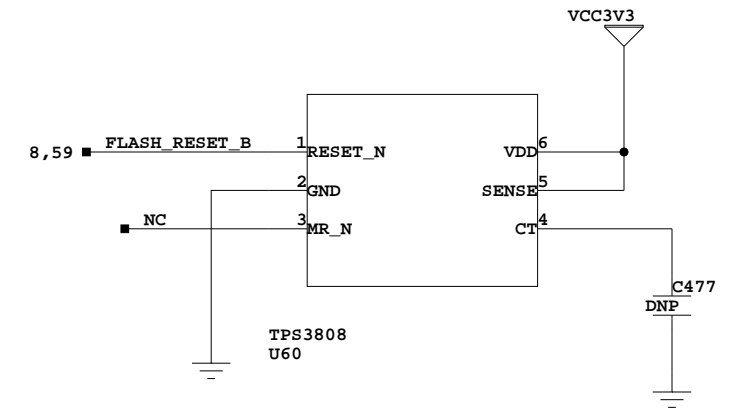
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
JTAG, DEBUG, TRACE CONNECTORS

Date:	7-10-2008_10:19	Ver:	C
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Silkscreen:  
"Strata FLASH"  
"256 MBit"



Programmable-Delay Supervisor Circuit



$$\langle \text{Cap Value in nF} \rangle = (((\langle \text{DELAY in S} \rangle) - (0.5 * 0.001)) * 175)$$

### SYNC. SRAM FLASH

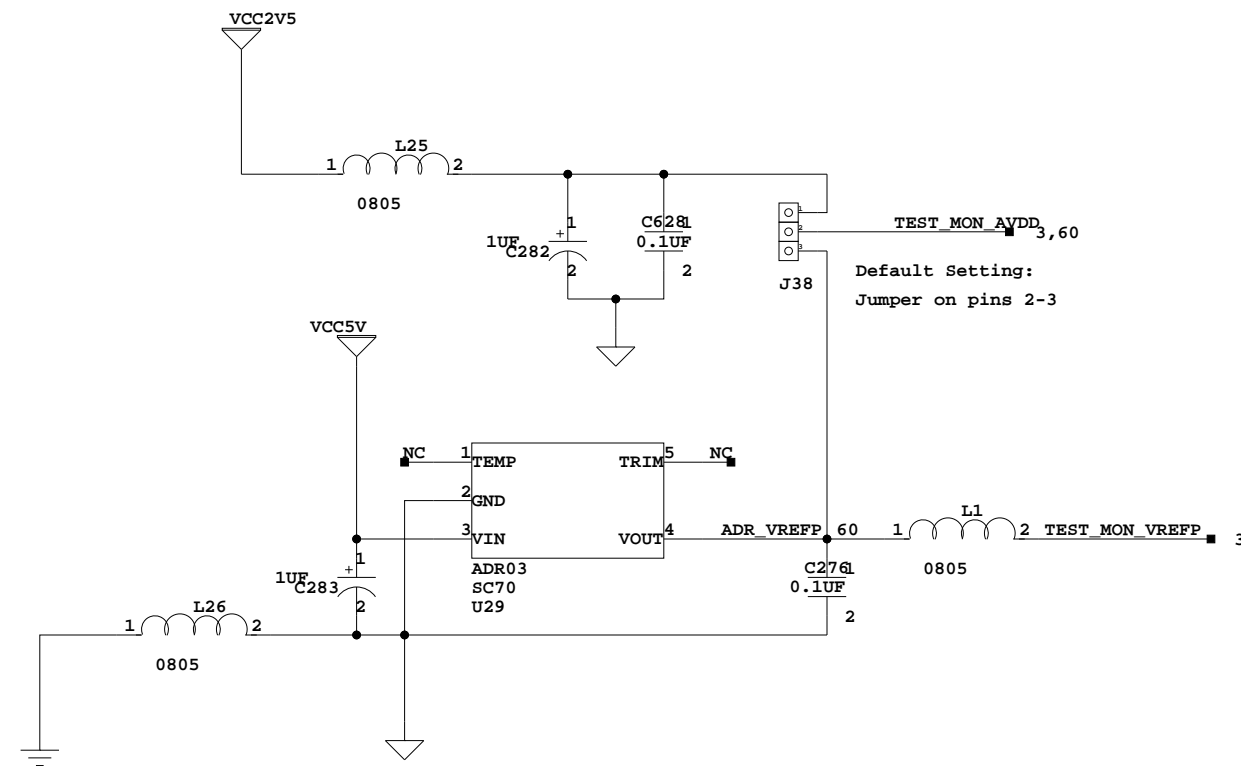


SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

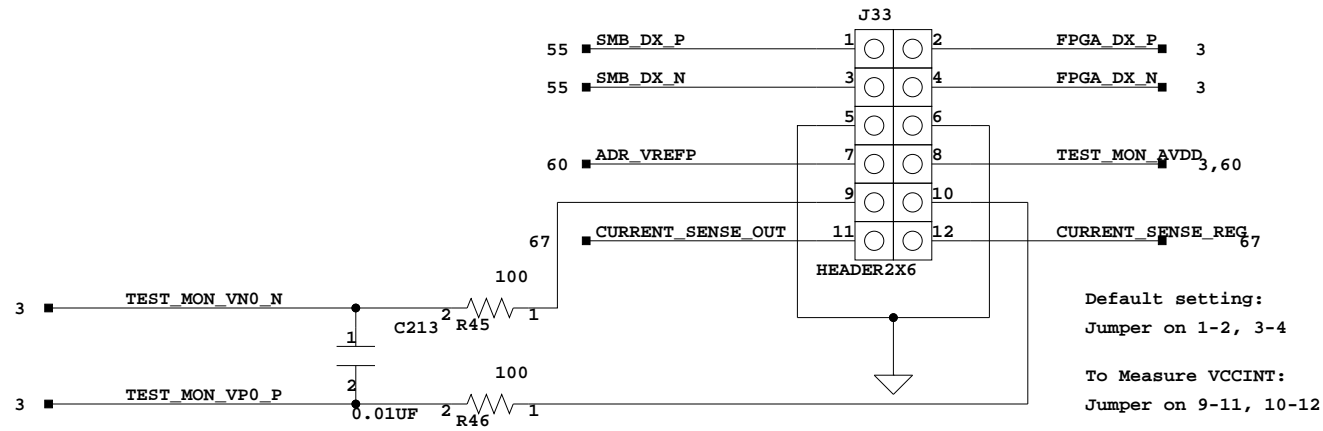
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM

SYNC. SRAM FLASH

Date:	8-1-2008_15:08	Ver:	C
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System Monitor Header for probing



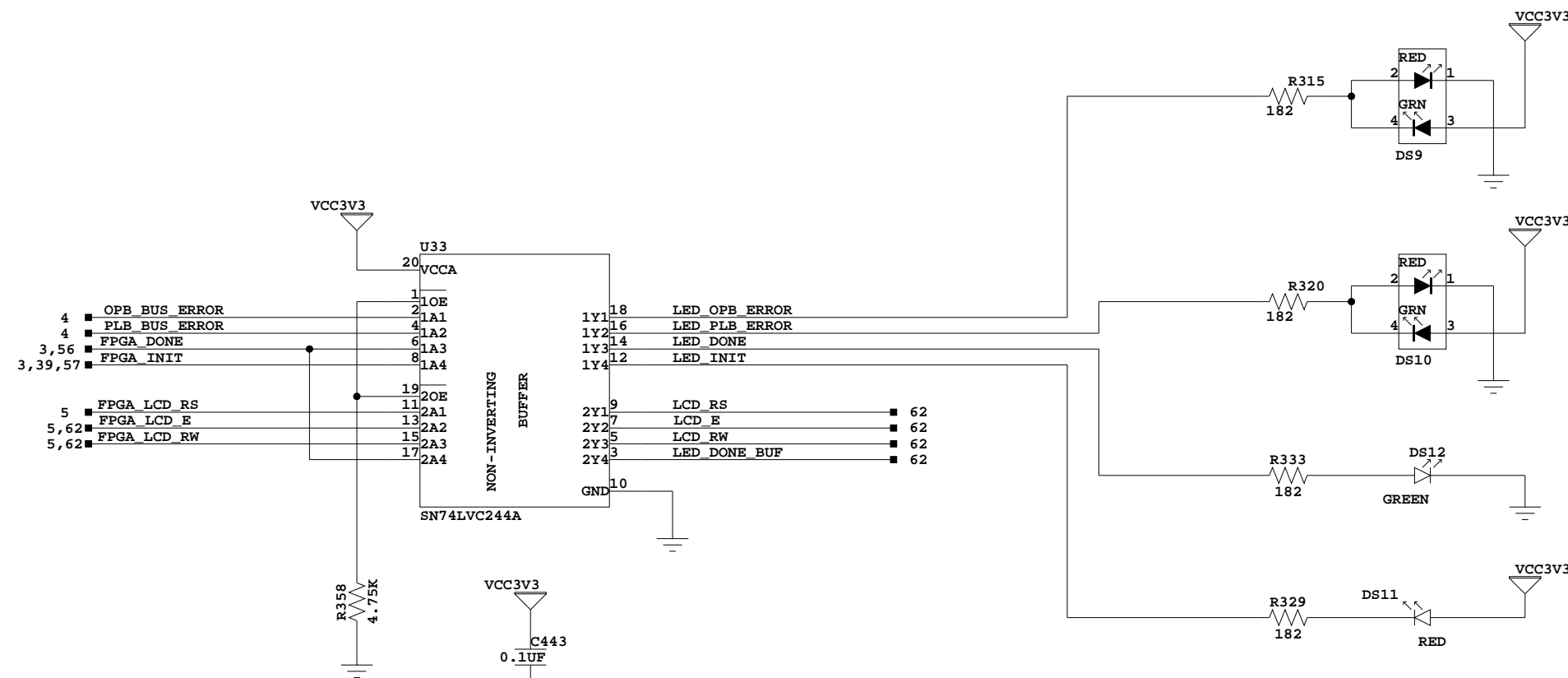
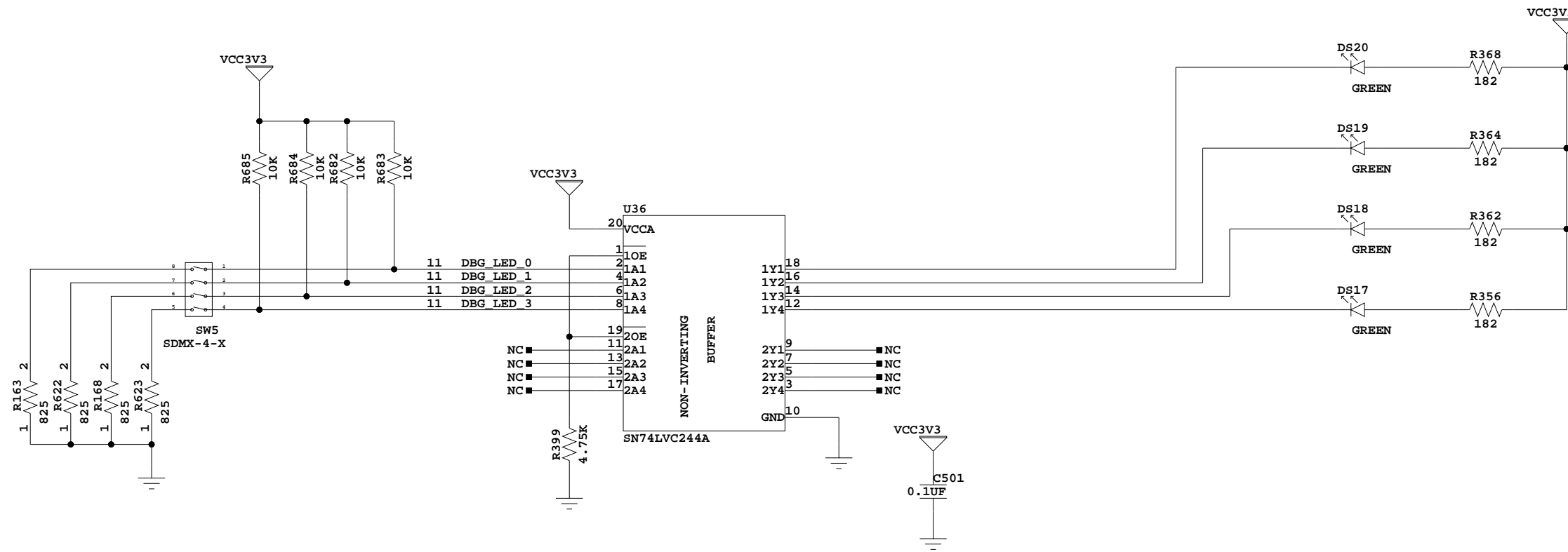
place 100 ohm resistors and 0.01 cap near FPGA

### SYSMON HEADER / AVDD VREFP SUPPLY

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
SYS MONITOR HEADER / FPGA AVDD VREFP SUPPLY

Date:	8-1-2008_15:09	Ver:	C
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**DEBUG AND STATUS LEDS**



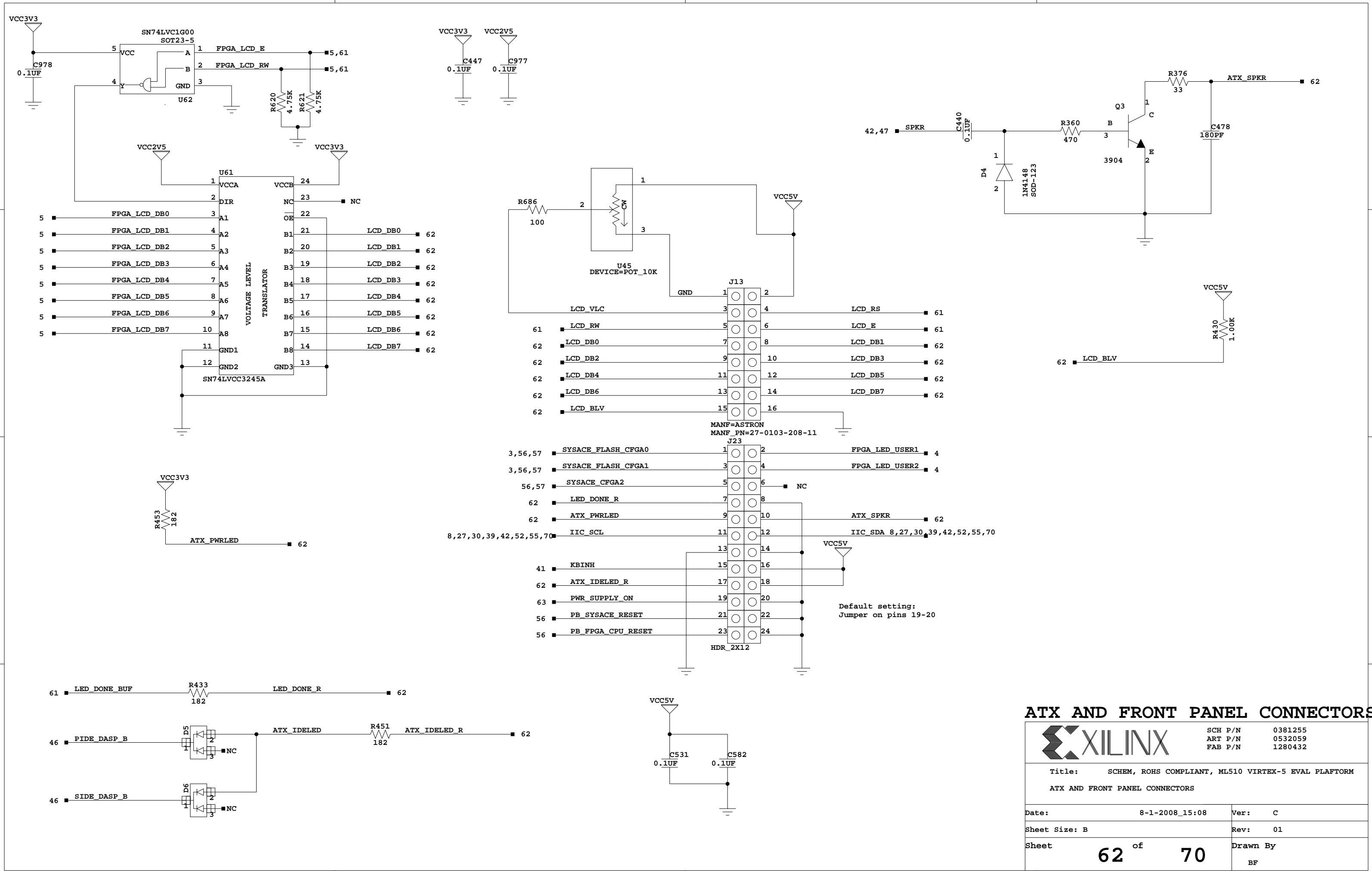
SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLATFOrm  
 DEBUG AND STATUS LEDS

Date: 8-1-2008\_15:08 Ver: C

Sheet Size: B Rev: 01

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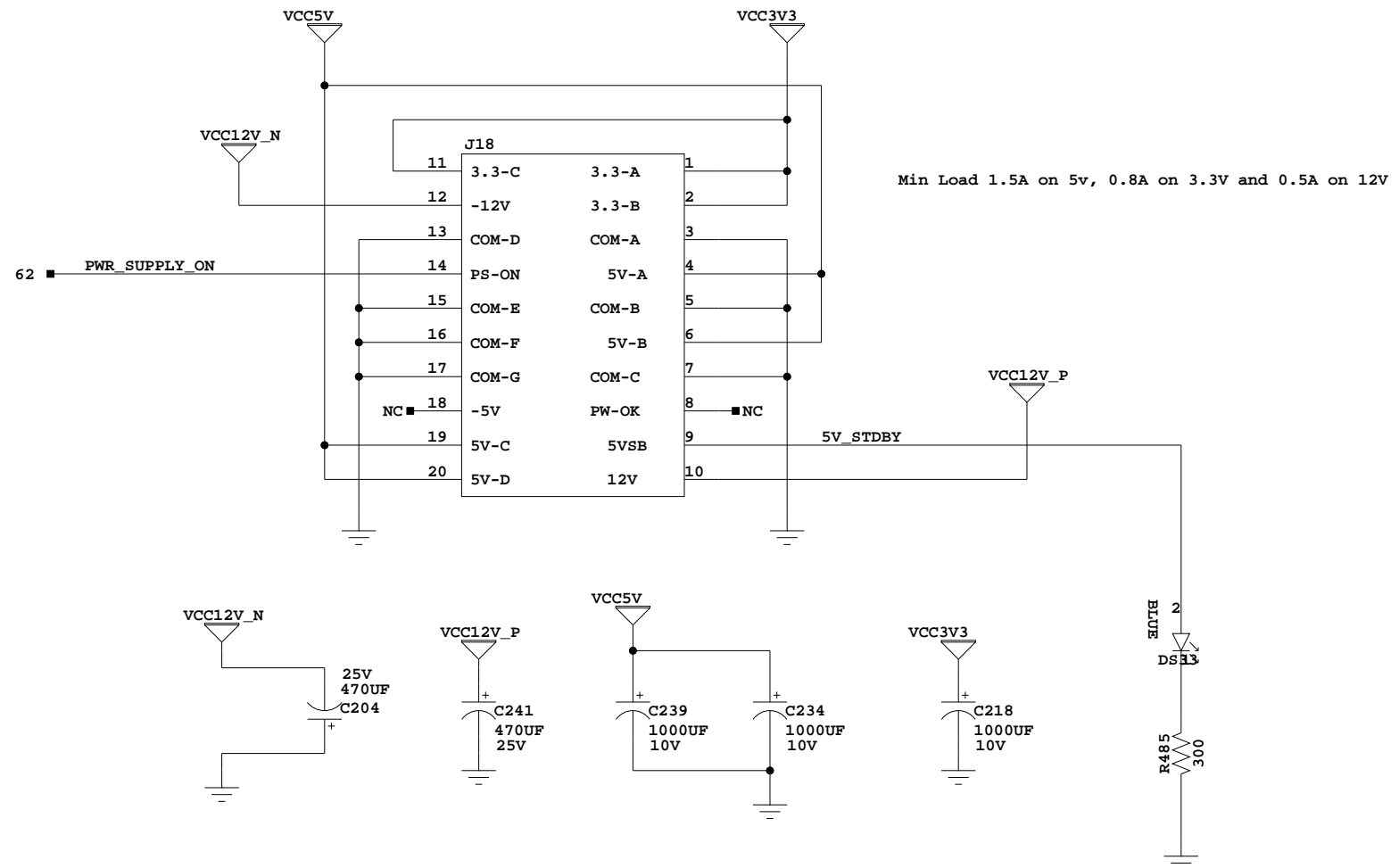
# ATX AND FRONT PANEL CONNECTORS



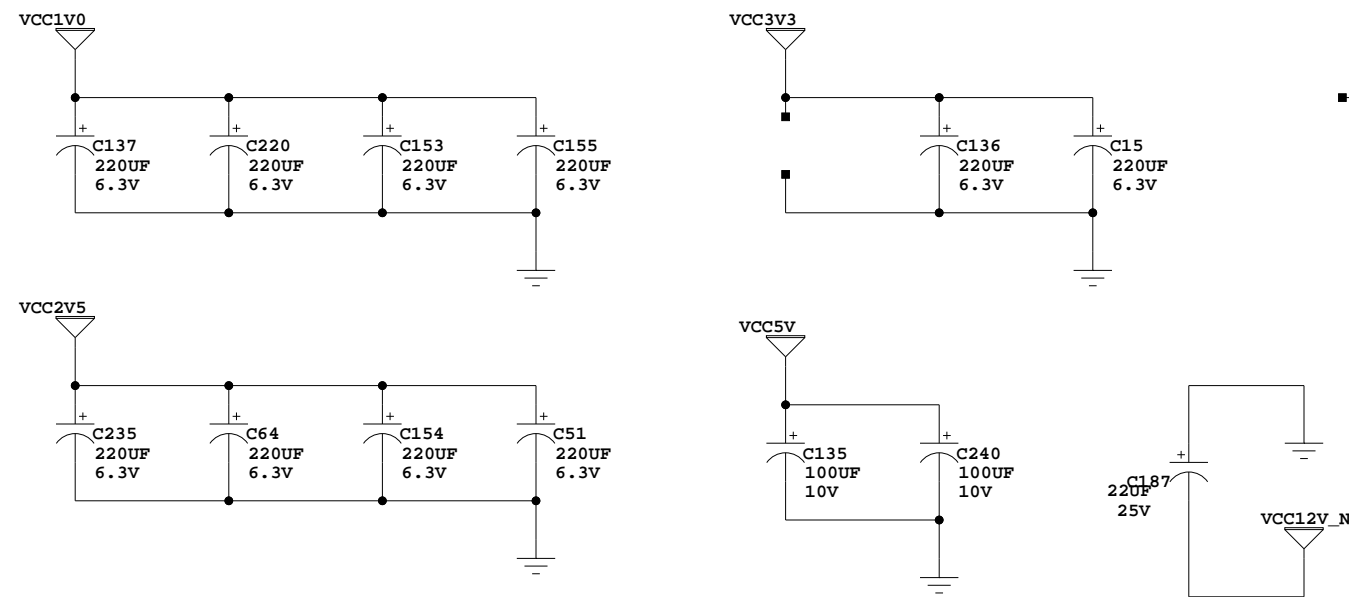
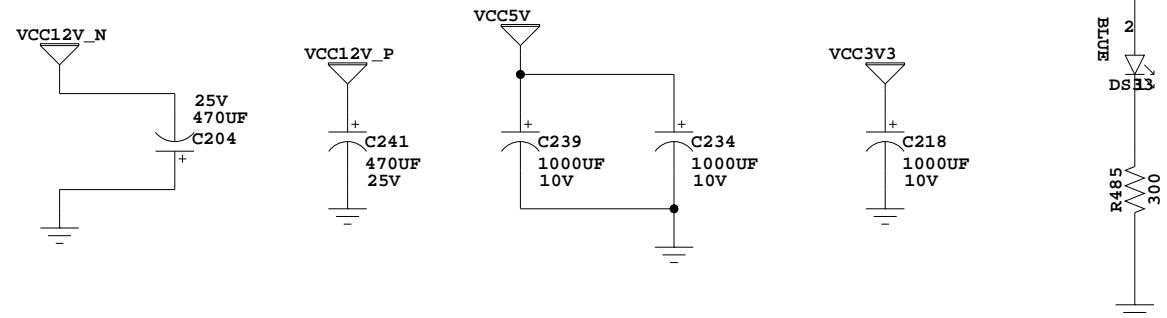
SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 ATX AND FRONT PANEL CONNECTORS

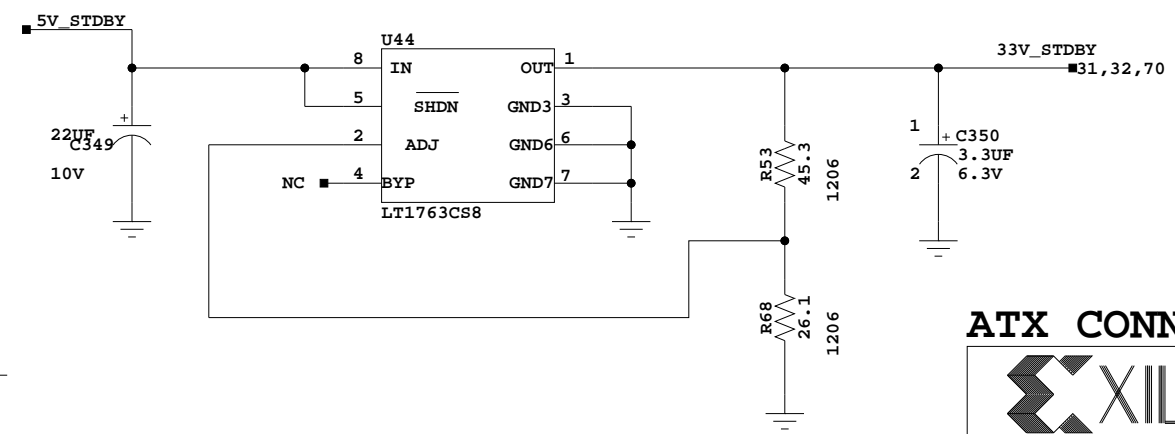
Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
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### ATX Power Connector



BULK CAPS DISTRIBUTED AROUND BOARD.

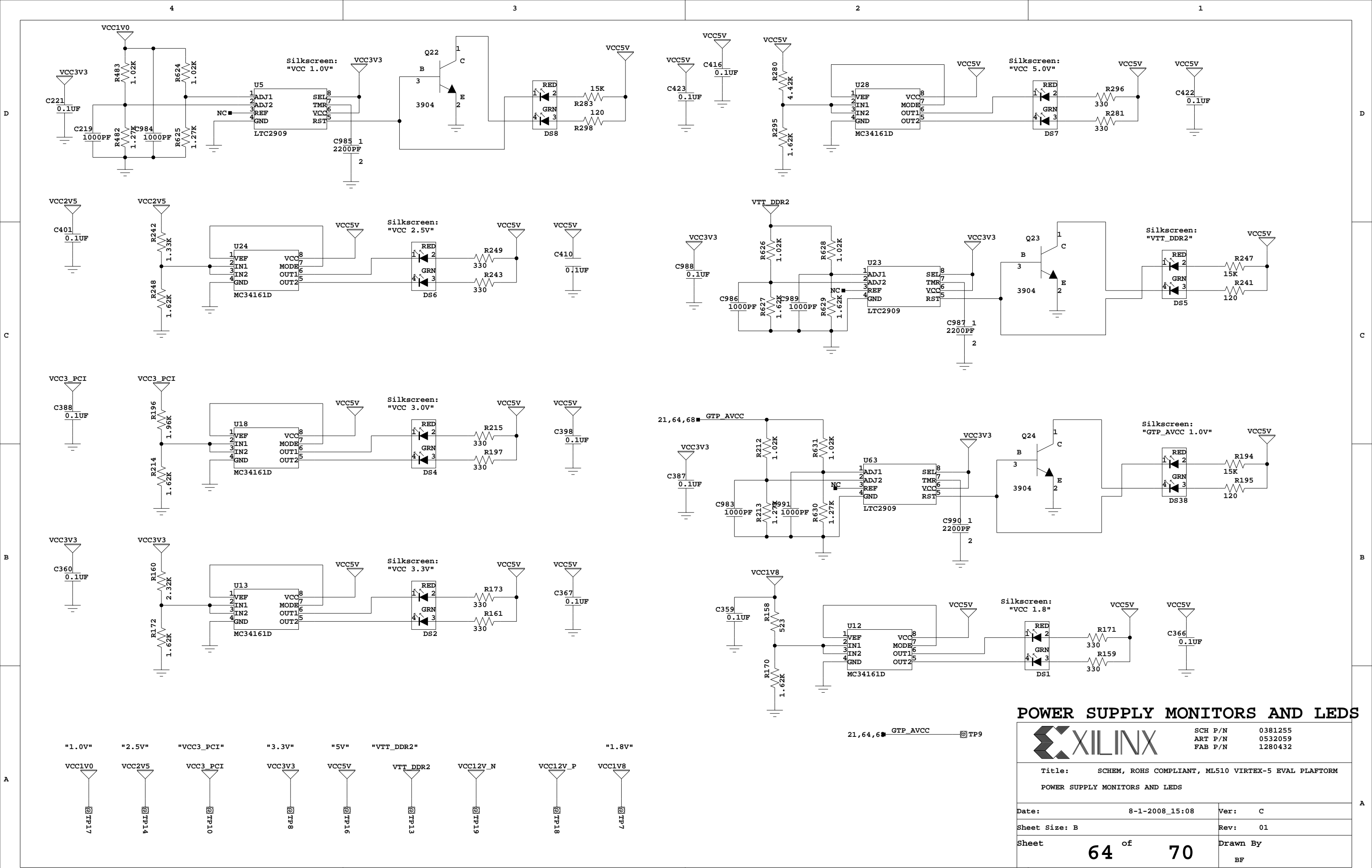


### ATX CONNECTOR, PWR TOGGLE

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 ATX CONNECTOR, PWR TOGGLE AND HEADER

Date:	8-1-2008_15:08	Ver:	C
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**POWER SUPPLY MONITORS AND LEDs**

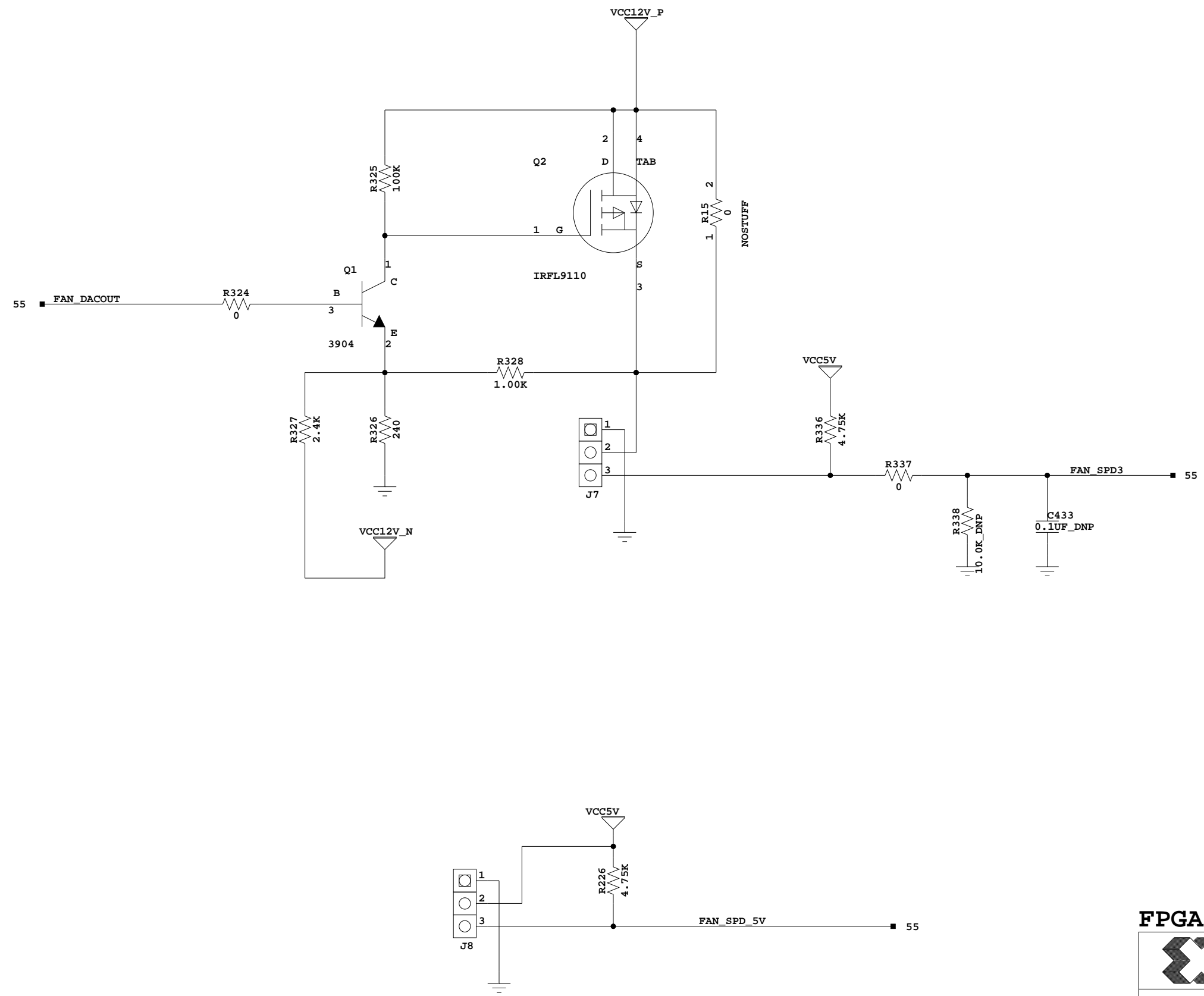
**XILINX** SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 POWER SUPPLY MONITORS AND LEDs

Date:	8-1-2008_15:08	Ver:	C
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### FPGA FAN SWITCH AND TACH

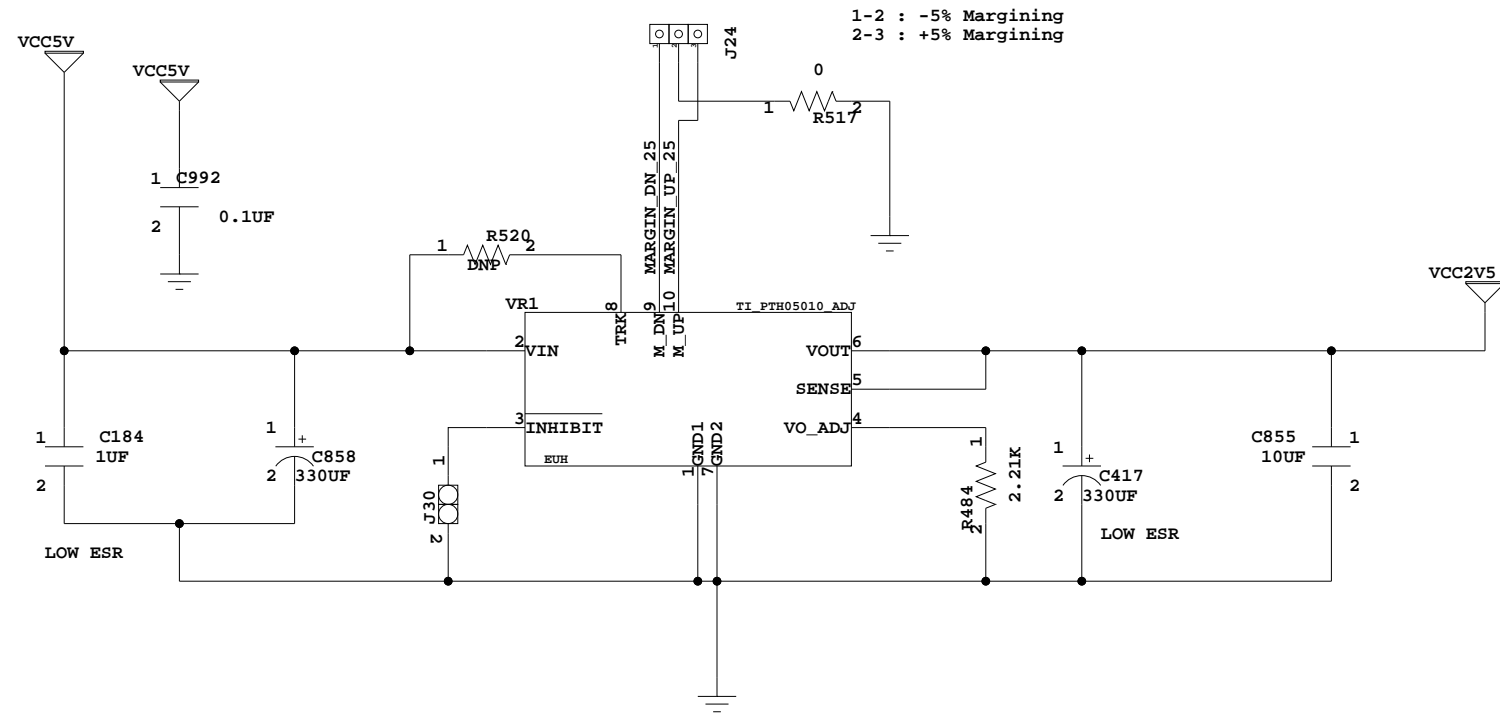


SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

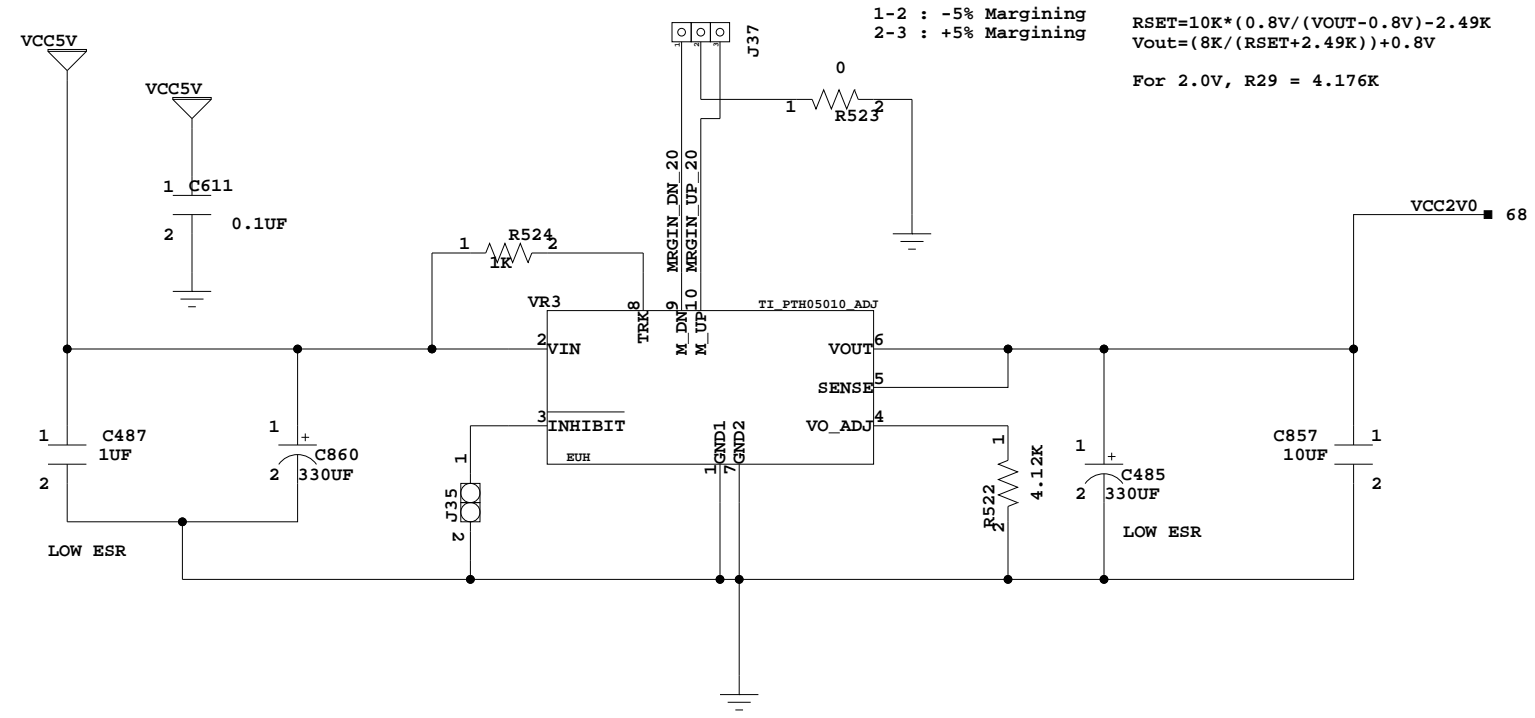
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 FPGA FAN SWITCH AND TACH

Date:	8-1-2008_15:08	Ver:	C
Sheet Size:	B	Rev:	01
Sheet	66 of 70	Drawn By	BF

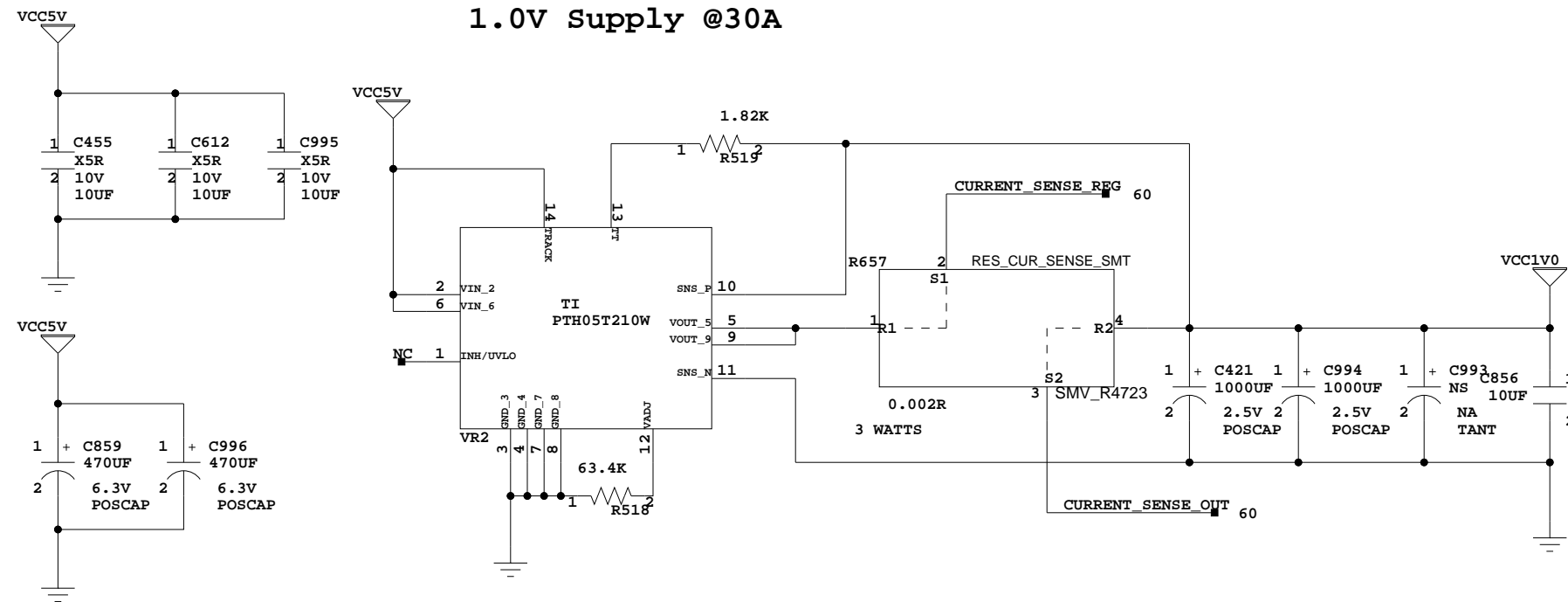
### 2.5V Supply @15A



### 2.0V Supply @15A



### 1.0V Supply @30A



## FPGA CORE AND IO VOLTAGE

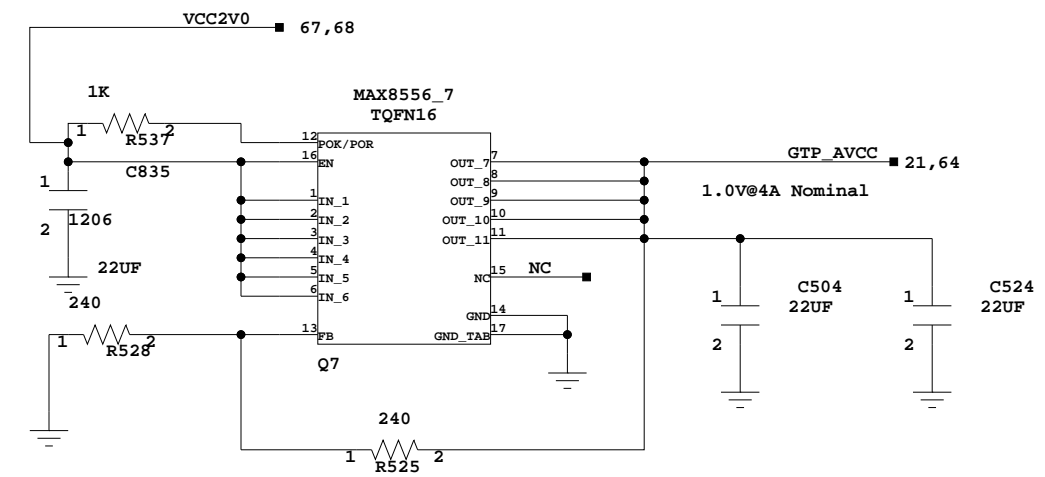
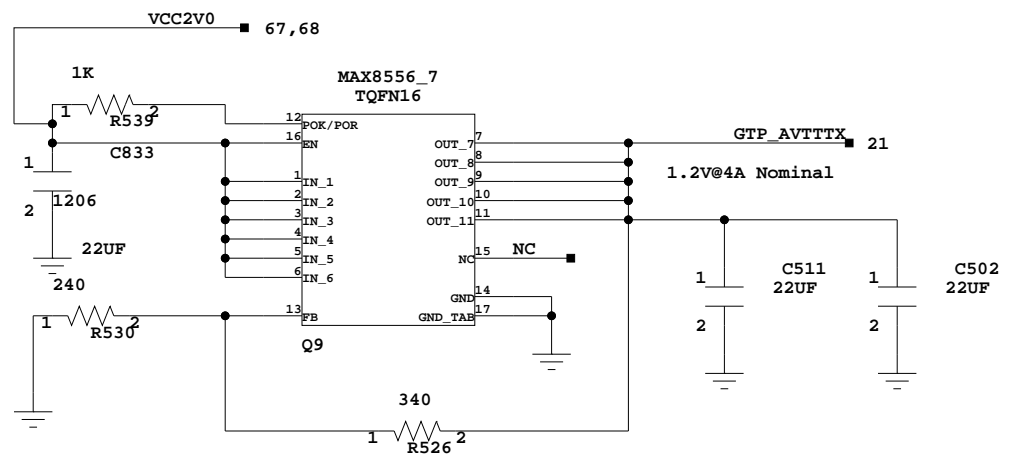
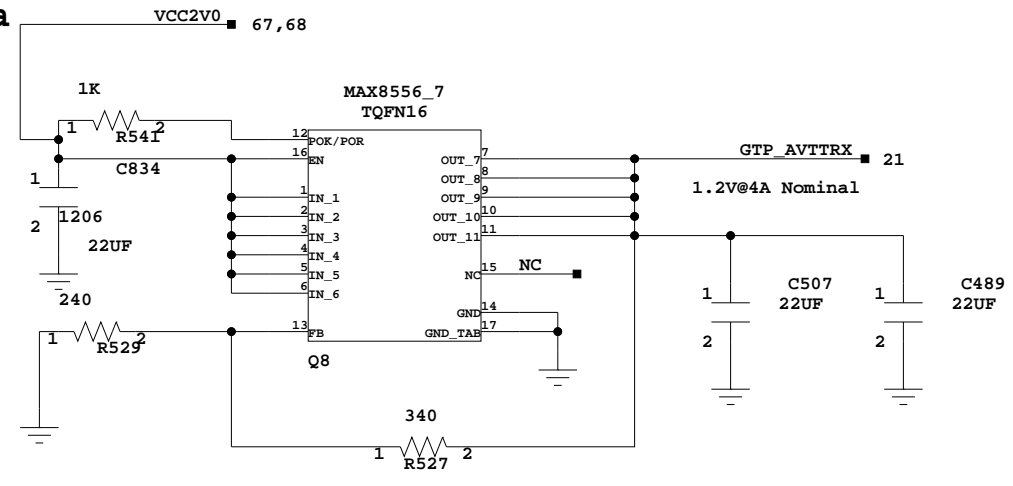
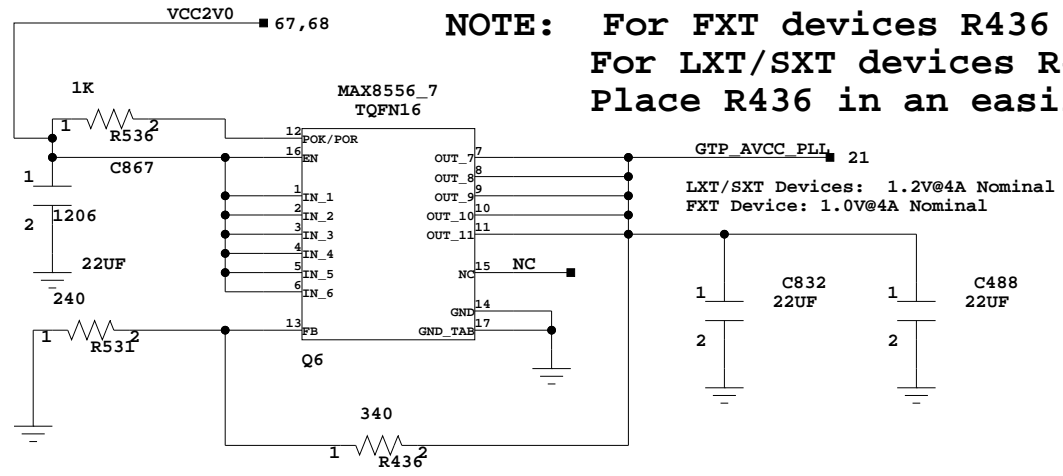


SCH P/N 0381255  
ART P/N 0532059  
FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFTRM  
FPGA CORE AND IO VOLTAGE

Date:	8-1-2008_15:08	Ver:	C
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**NOTE: For FXT devices R436 must be 240 ohms  
 For LXT/SXT devices R436 should be 340 ohms  
 Place R436 in an easily accessible area**



$$R2 = R1 * \left\{ \left( \frac{V_{out}}{0.5} \right) - 1 \right\}$$

**GTP POWER SUPPLIES**



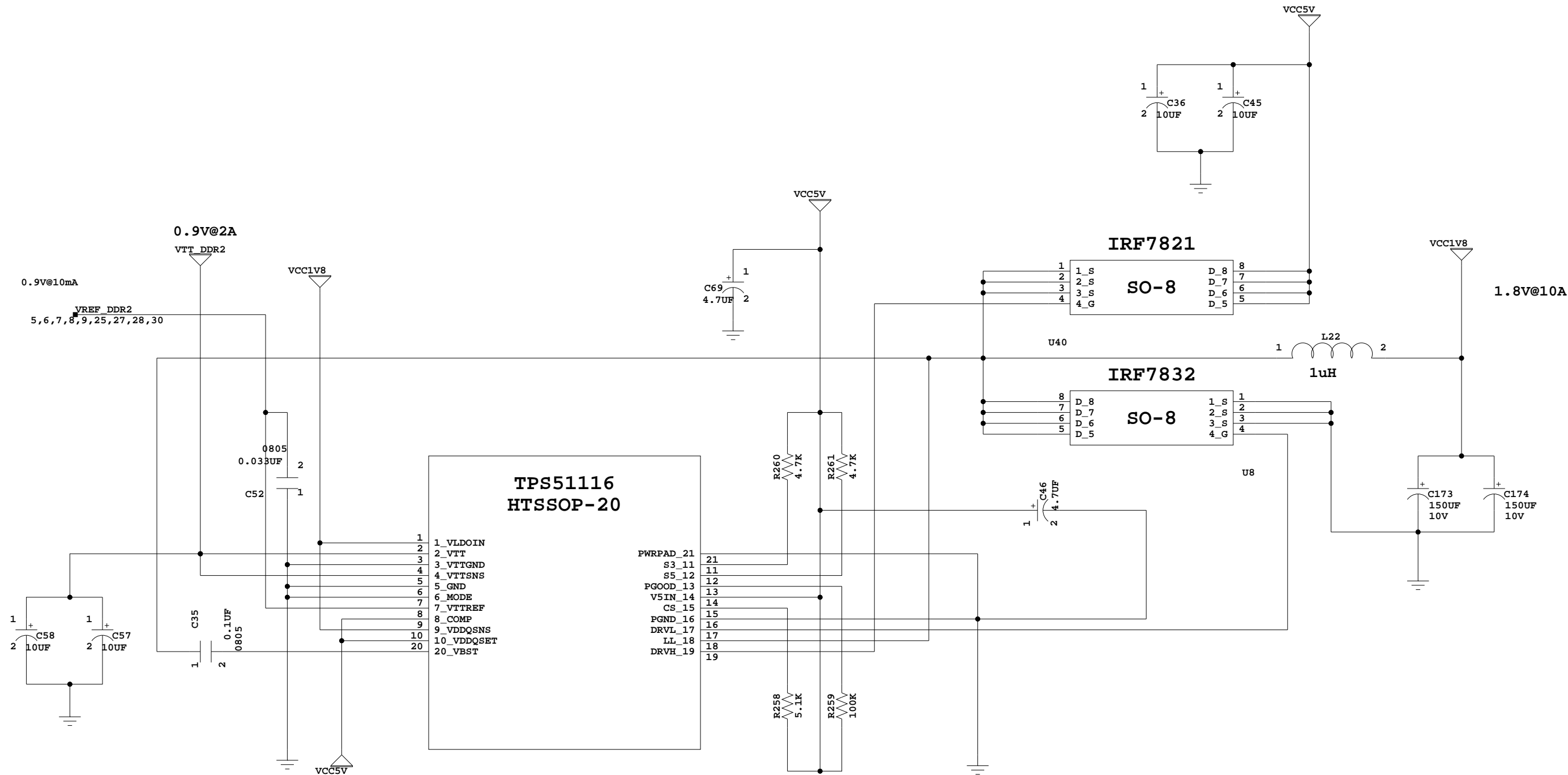
SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM  
 GTP POWER SUPPLIES


Date: 8-1-2008\_15:08 Ver: C

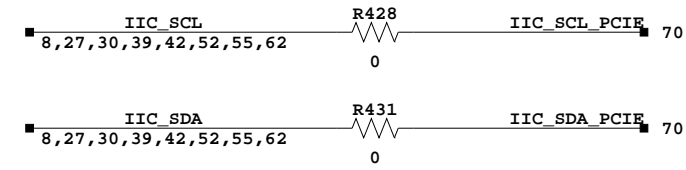
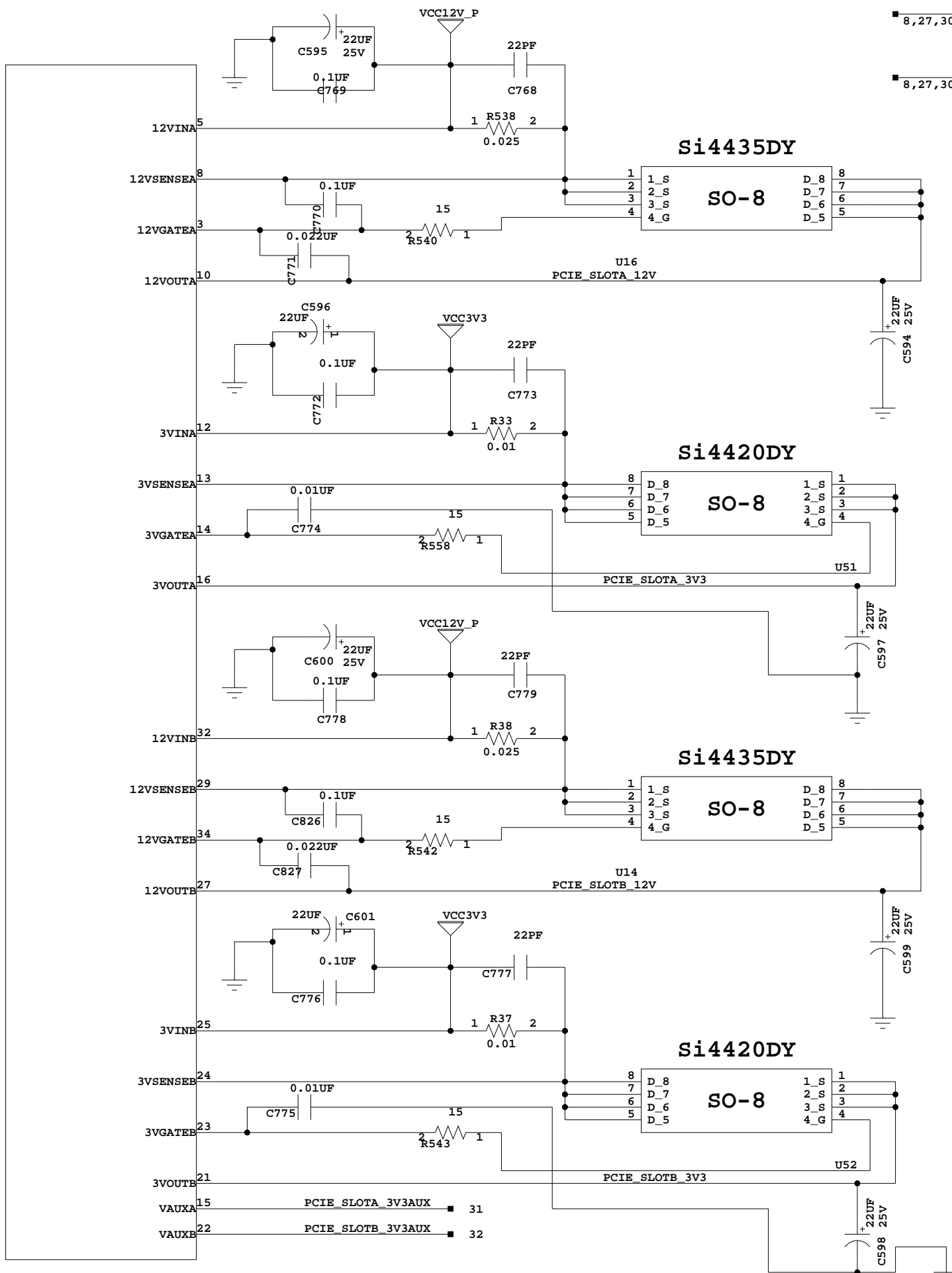
Sheet Size: B Rev: 01

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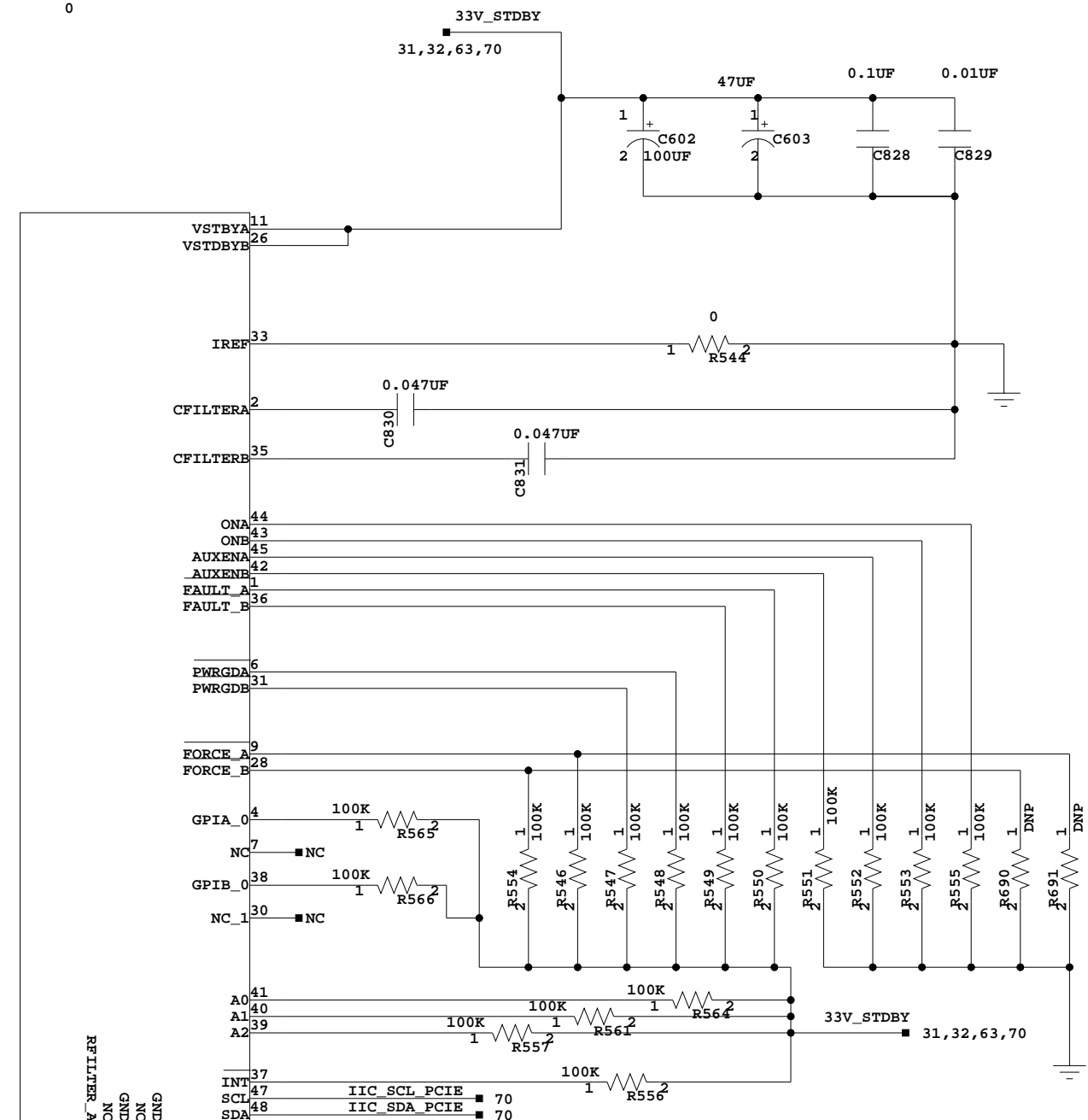


### DDR2 POWER SUPPLY

	SCH P/N	0381255
	ART P/N	0532059
	FAB P/N	1280432
Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM DDR2 POWER SUPPLY		
Date:	8-1-2008_15:08	Ver: C
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I2C ADDR = 0x8E  
 Make sure IIC Address is set correctly



### PCI-E PWR MGMT CONTROLLER



SCH P/N 0381255  
 ART P/N 0532059  
 FAB P/N 1280432

Title: SCHEM, ROHS COMPLIANT, ML510 VIRTEX-5 EVAL PLAFORM PCI-E PWR MGMT CONTROLLER	
Date: 8-1-2008_15:08	Ver: C
Sheet Size: B	Rev: 01
Sheet 70 of 70	Drawn By BF