Spartan-3 PCIe Starter Board

Avnet Engineering Services

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05/03/07

REVISION 2.1

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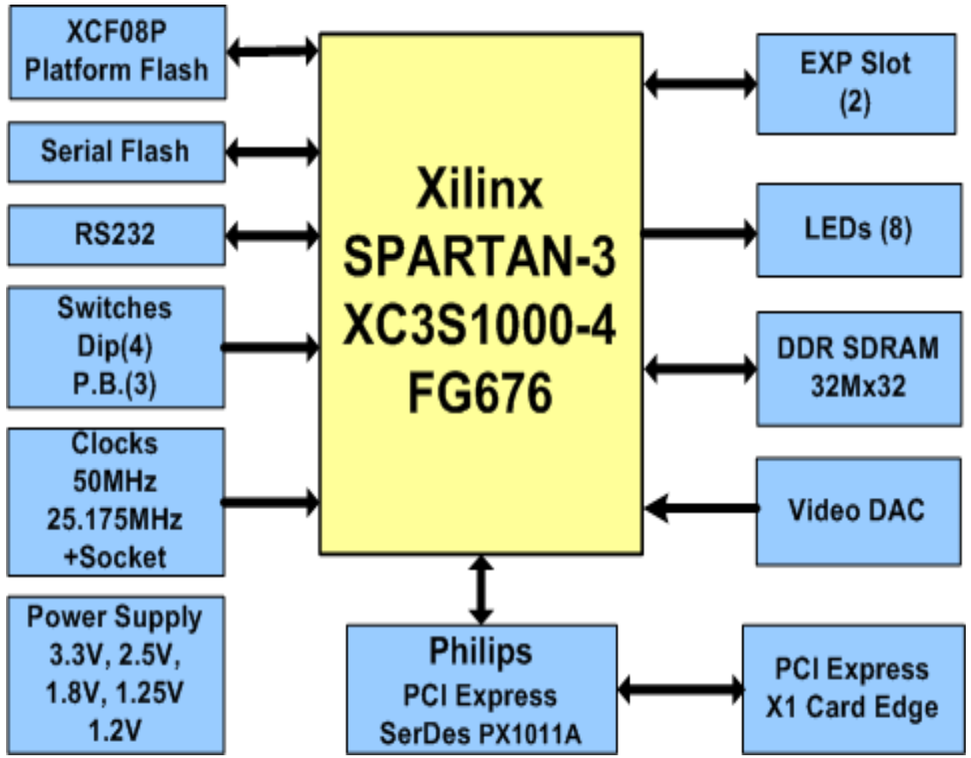
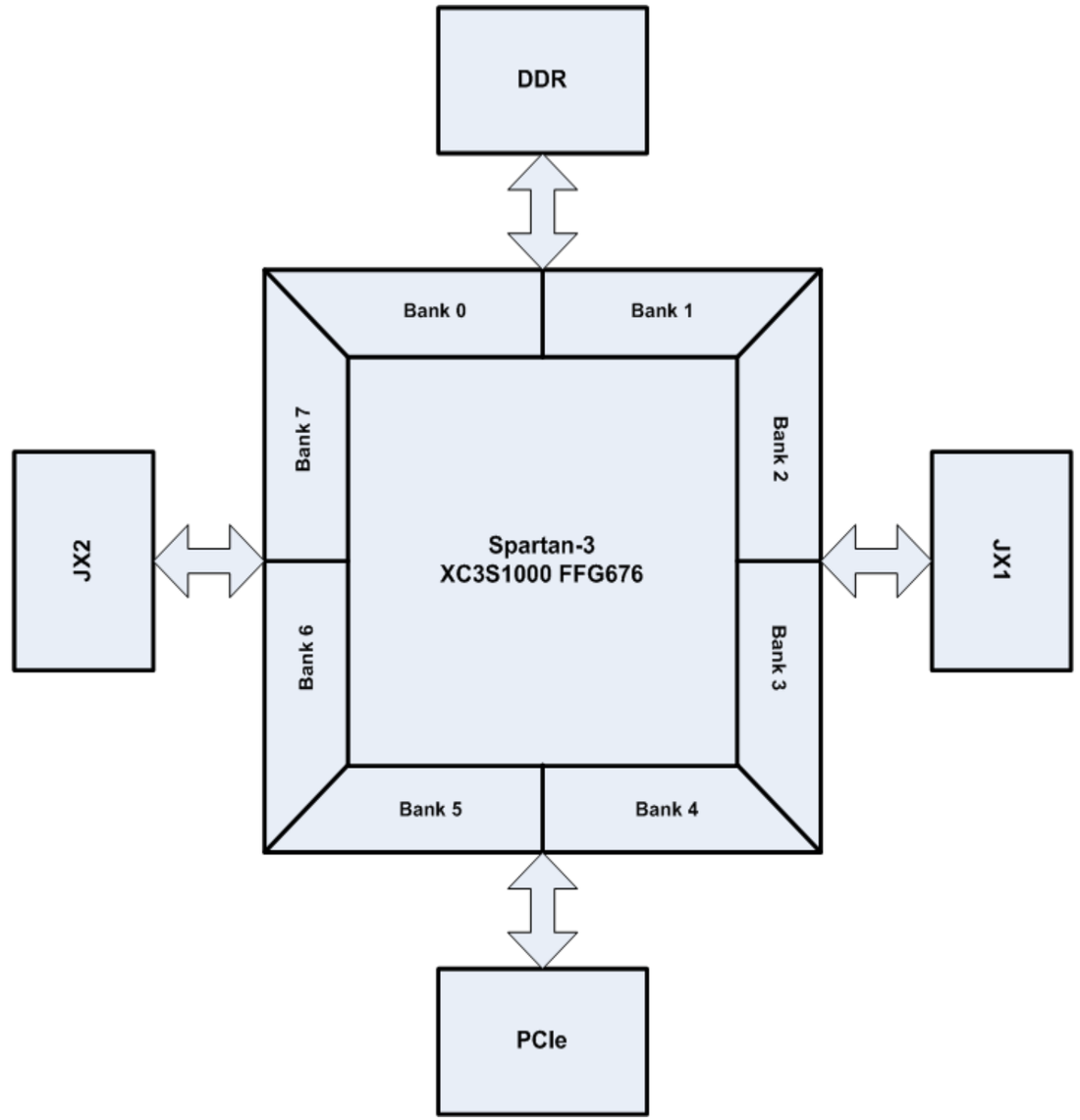
Title: Spartan-3 PCIe Starter Board		Cover sheet	
Size: B	Document Number: AES-SP3-PCIE-SCH		Rev: 2.1
Date: Thursday, May 03, 2007	Sheet 1 of 13		





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Title: Spartan-3 PCIe Starter Board	Block Diagram	
Size: B	Document Number: AES-SP3-PCIE-SCH	Rev: 2.1
Date: Thursday, May 03, 2007	Sheet 2 of 13	

10 DDR_A[0:13]

RP3 24R0: DDR_A0 A0, DDR_A1 A1, DDR_A2 A2, DDR_A3 A3
RP43 24R0: DDR_A7 A7, DDR_A4 A4, DDR_A6 A6, DDR_A5 A5
RP12 24R0: DDR_A10 A10, DDR_A8 A8, DDR_A9 A9, DDR_A11 A11
RP38 24R0: DDR_A13 A13, DDR_A12 A12, 10 DDR_BA0 BA0, 10 DDR_BA1 BA1
RP32 24R0: 10 DDR_CAS# CAS#, 10 DDR_WE# WE#, 10 DDR_CS# CS#, 10 DDR_RAS# RAS#
RP11 24R0: 10 DDR_CKE CKE, 10 DDR_CK0# CK0#, 10 DDR_CK0 CK0
RP15 24R0: 10 DDR_CK1# CK1#, 10 DDR_CK1 CK1
RP7 24R0: 10 DDR_DM3 DM3, 10 DDR_DM2 DM2, 10 DDR_DM1 DM1, 10 DDR_DM0 DM0

10 DDR_D[0:31]

DDR_D0, DDR_D1, DDR_D2, DDR_D3, DDR_D4, DDR_D5, DDR_D6, DDR_D7, DDR_D8, DDR_D9, DDR_D10, DDR_D11, DDR_D12, DDR_D13, DDR_D14, DDR_D15, DDR_D16, DDR_D17, DDR_D18, DDR_D19, DDR_D20, DDR_D21, DDR_D22, DDR_D23, DDR_D24, DDR_D25, DDR_D26, DDR_D27, DDR_D28, DDR_D29, DDR_D30, DDR_D31

Place R25 close to U18.C10. Total length of U18.C10 to R25 to U18.D10 is 2X the routed DDR Clock length (DDR_CK0, DDR_CK1).

+2.5V, R23 49R9, R22 49R9, +1.25V_REF, +1.25V_TT, R24 49R9, R25 24R0 (Cntrl0_Rst_DQS_Div_In → Cntrl0_Rst_DQS_Div_Out)

U18A — XC3S1000_FG676

10 DDR_DQS0	E5	IO_L01N_0/VRP_0	
10 DDR_DQS1	D5	IO_L01P_0/VRN_0	
DDR_D4	A3	IO_0_No_Pair_0	
	A5	IO_0_No_Pair_1	
DDR_D0	A6	IO_0_No_Pair_2	
DDR_D22	C4	IO_0_No_Pair_3	
DDR_D24	C12	IO_0_No_Pair_5	
LED1	E13	IO_0_No_Pair_6	
DDR_D18	H11	IO_0_No_Pair_7	
	H12	IO_0_No_Pair_8	
	B3	IO_0_No_Pair_9/VREF_0	
	F7	IO_0_No_Pair_10/VREF_0	
	G10	IO_0_No_Pair_11/VREF_0	
DDR_D1	B4	IO_L05N_0	
	A4	IO_L05P_0/VREF_0	
DDR_D2	C5	IO_L06N_0	
DDR_D3	B5	IO_L06P_0	
DDR_D5	F6	IO_L07N_0	
DM0	D6	IO_L07P_0	
DDR_D6	C6	IO_L08N_0	
DDR_D7	B6	IO_L08P_0	
CK0#	E7	IO_L09N_0	
CK0	D7	IO_L09P_0	
DDR_D8	B7	IO_L10N_0	
DDR_D9	A7	IO_L10P_0	
DDR_D10	B8	IO_L15N_0	
DDR_D11	A8	IO_L15P_0	
DDR_D12	G9	IO_L16N_0	
DDR_D13	F9	IO_L16P_0	
DDR_D14	E10	IO_L19N_0	
DDR_D15	E10	IO_L19P_0	
	D10	IO_L22N_0	
	C10	IO_L22P_0	
10 DDR_DQS2	G11	IO_L24N_0	
SW4	F11	IO_L24P_0	
DDR_D16	E11	IO_L25N_0	
DDR_D17	D11	IO_L25P_0	
DDR_D19	G12	IO_L27N_0	
DM1	H13	IO_L27P_0	
DDR_D20	F12	IO_L28N_0	
DDR_D21	E12	IO_L28P_0	
DDR_D23	B12	IO_L29N_0	
DM2	A12	IO_L29P_0	
10 DDR_DQS3	G13	IO_L30N_0	
A13	F13	IO_L30P_0	
DDR_D25	D13	IO_L31N_0	
	C13	IO_L31P_0/VREF_0	
4,5,6 NC_NET	G8	IO_L11N_0	
4,5,6 NC_NET	F8	IO_L11P_0	
4,5,6 NC_NET	E8	IO_L12N_0	
4,5,6 NC_NET	D8	IO_L12P_0	
4,5,6 NC_NET	C8	IO_0_No_Pair_4	
4,5,6 NC_NET	F9	IO_L17N_0	
4,5,6 NC_NET	D9	IO_L17P_0	
4,5,6 NC_NET	C9	IO_L18N_0	
4,5,6 NC_NET	B9	IO_L18P_0	
4,5,6 NC_NET	B10	IO_L23N_0	
4,5,6 NC_NET	A10	IO_L23P_0	
4,5,6 NC_NET	B11	IO_L26N_0	
4,5,6 NC_NET	A11	IO_L26P_0/VREF_0	
	B13	IO_L32N_0/GCLK7	
	A13	IO_L32P_0/GCLK6	

add for 1500 & 2000

bank0 bank1

IO_L32N_1/GCLK5	B14	
IO_L32P_1/GCLK4	C14	
IO_1_No_Pair_0	A14	DDR_D26
IO_1_No_Pair_1	A22	LED5
IO_1_No_Pair_2	A23	LED6
IO_1_No_Pair_3	D16	LED7
IO_1_No_Pair_4	E18	LED8
IO_1_No_Pair_5	F14	DDR_D28
IO_1_No_Pair_6	F20	SW1
IO_1_No_Pair_7	G19	SW2
IO_1_No_Pair_8/VREF_1	C15	
IO_1_No_Pair_9/VREF_1	C17	
IO_L04N_1	B23	SW3
IO_L04P_1	C23	LED3
IO_L05N_1	F21	
IO_L05P_1	F22	
IO_L06N_1/VREF_1	C22	LED2
IO_L06P_1	C21	WE#
IO_L07N_1	D21	CAS#
IO_L07P_1	A21	RAS#
IO_L08N_1	B21	CS#
IO_L08P_1		
IO_L09N_1	D20	CKE
IO_L09P_1	E20	BA0
IO_L10N_1/VREF_1	A20	
IO_L10P_1	B20	DDR_CK_FB 5
IO_L15N_1	A19	BA1
IO_L15P_1	B19	A0
IO_L16N_1	F18	A1
IO_L16P_1	G18	A2
IO_L19N_1	E17	A3
IO_L19P_1	G17	A4
IO_L22N_1	D17	A5
IO_L22P_1	E17	A6
IO_L24N_1	G16	A7
IO_L24P_1	H16	A8
IO_L25N_1	E16	A9
IO_L25P_1	F16	A10
IO_L27N_1	G15	A11
IO_L27P_1	H15	A12
IO_L28N_1	E15	CK1#
IO_L28P_1	F15	CK1
IO_L29N_1	A15	DDR_D30
IO_L29P_1	B15	DDR_D31
IO_L30N_1	G14	DDR_D29
IO_L30P_1	H14	DM3
IO_L31N_1/VREF_1	D14	
IO_L31P_1	E14	DDR_D27
IO_L11N_1	E19	NC_NET 4,5,6
IO_L11P_1	F19	NC_NET 4,5,6
IO_L12N_1	C19	NC_NET 4,5,6
IO_L12P_1	D19	NC_NET 4,5,6
IO_1_No_Pair_10/VREF_1	D18	
IO_L18N_1	B18	NC_NET 4,5,6
IO_L18P_1	C18	NC_NET 4,5,6
IO_L23N_1	A17	NC_NET 4,5,6
IO_L23P_1	B17	NC_NET 4,5,6
IO_L26N_1	A16	NC_NET 4,5,6
IO_L26P_1	B16	NC_NET 4,5,6
IO_L01N_1/VRP_1	D22	
IO_L01P_1/VRN_1	E22	

+2.5V, R28 49R9, R27 49R9

+3.3V, U20, C169 0.1uF, 50MHz, U19 NC7SV126, C159 0.1uF, R35 33R0

6 JX1_SE_CLK_IN, U12 SN74CB3T1G125, 0.1uF C109, +2.5V, R31 33R0

+2.5V, 0.1uF C94, U40 NC7SV126, R73 33R0, R37 33R0, R74 4.75K

U10 OSC_8PIN: OUT, OSC, VCC, ENABLE, GND; +3.3V, C100 0.1uF

+2.5V, 0.1uF C179, U23 NC7SV126, R38 4.75K

U26 DNI: VCC, OUT EN, GND; +3.3V, C189 0.1uF

D2 ERROR, R4 100, +2.5V, R7 4.75K, SW4 FPGA Reset, C4 0.1uF

+2.5V, R11 1K, R10 1K, R9 1K, R8 1K, SW5 SW DIP-4/SM, SW1–SW4, RP27 10K

4 LED4

D3 LED1 — R60 100
D4 LED2 — R61 100
D5 LED3 — R62 100
D6 LED4 — R63 100
D7 LED5 — R64 100
D8 LED6 — R65 100
D9 LED7 — R66 100
D10 LED8 — R67 100

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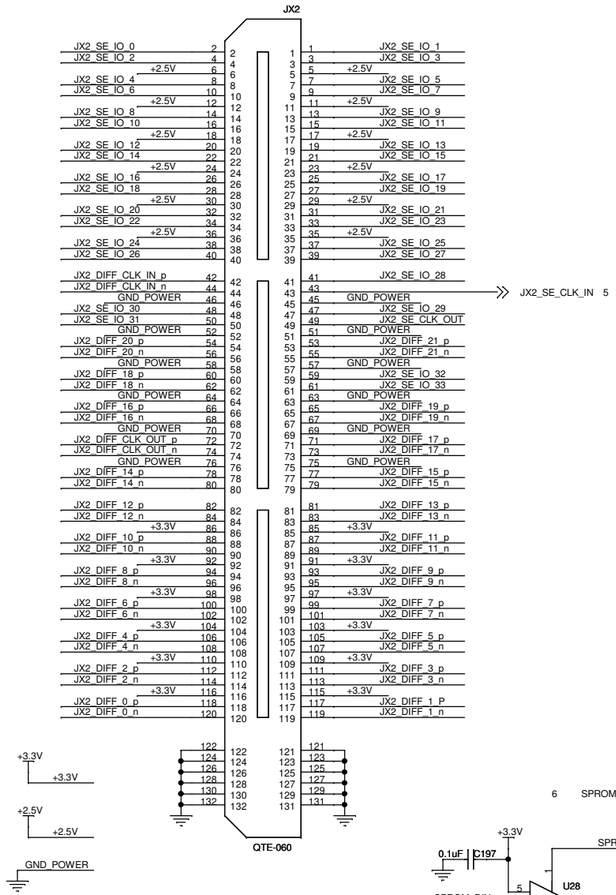
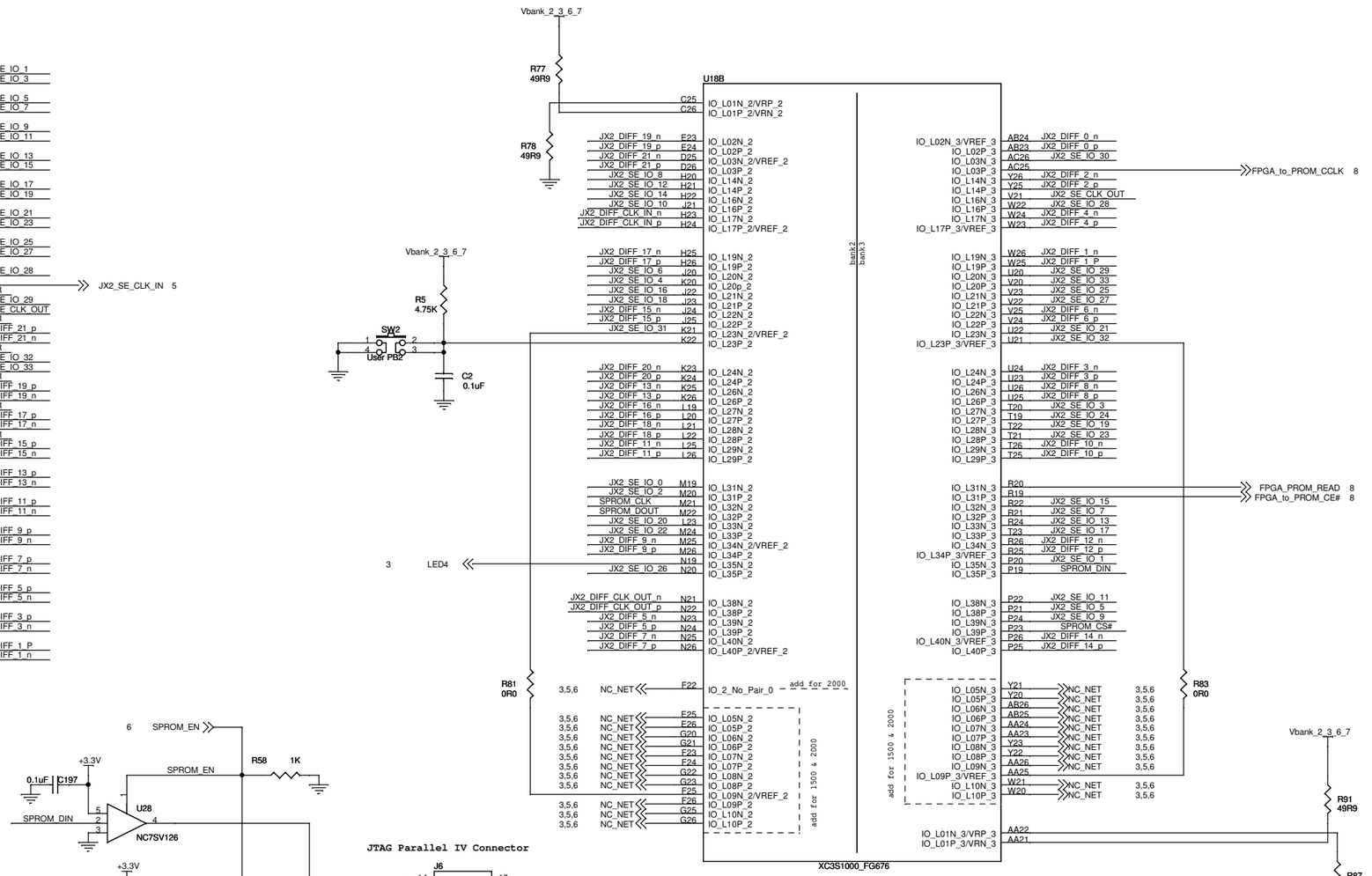
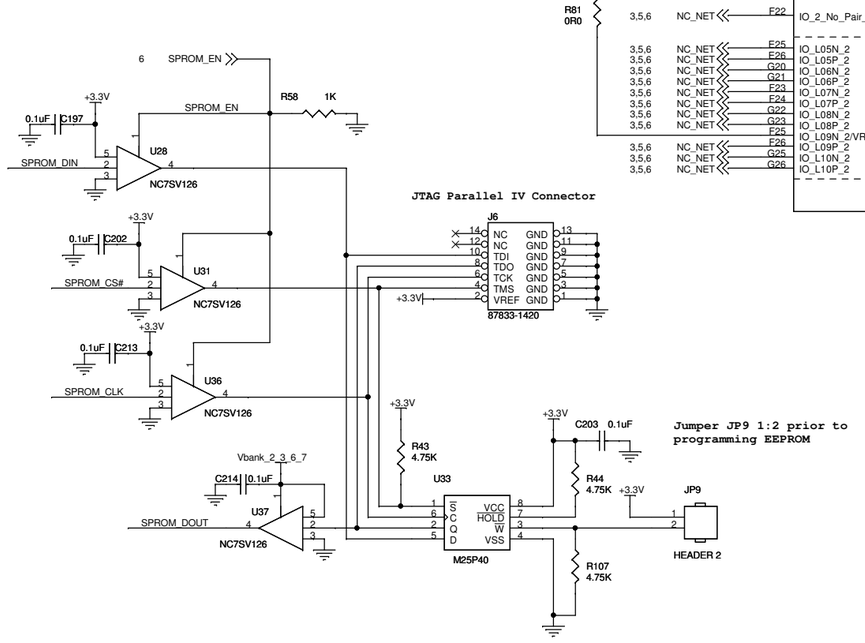
Title	Spartan-3 PCIe Starter Board	FPGA Banks 0 & 1
Size C	Document Number AES-SP3-PCIE-SCH	Rev 2.1
Date: Thursday, May 03, 2007	Sheet 3 of 13	







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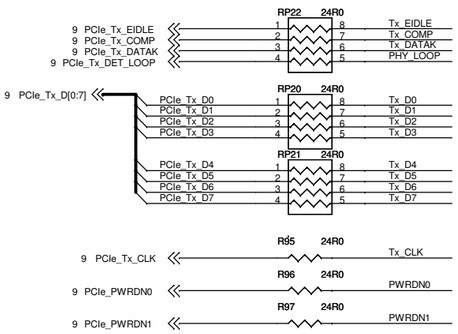
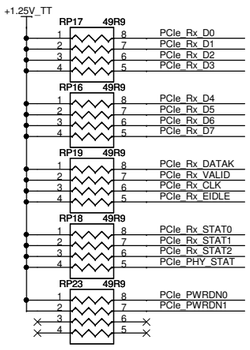
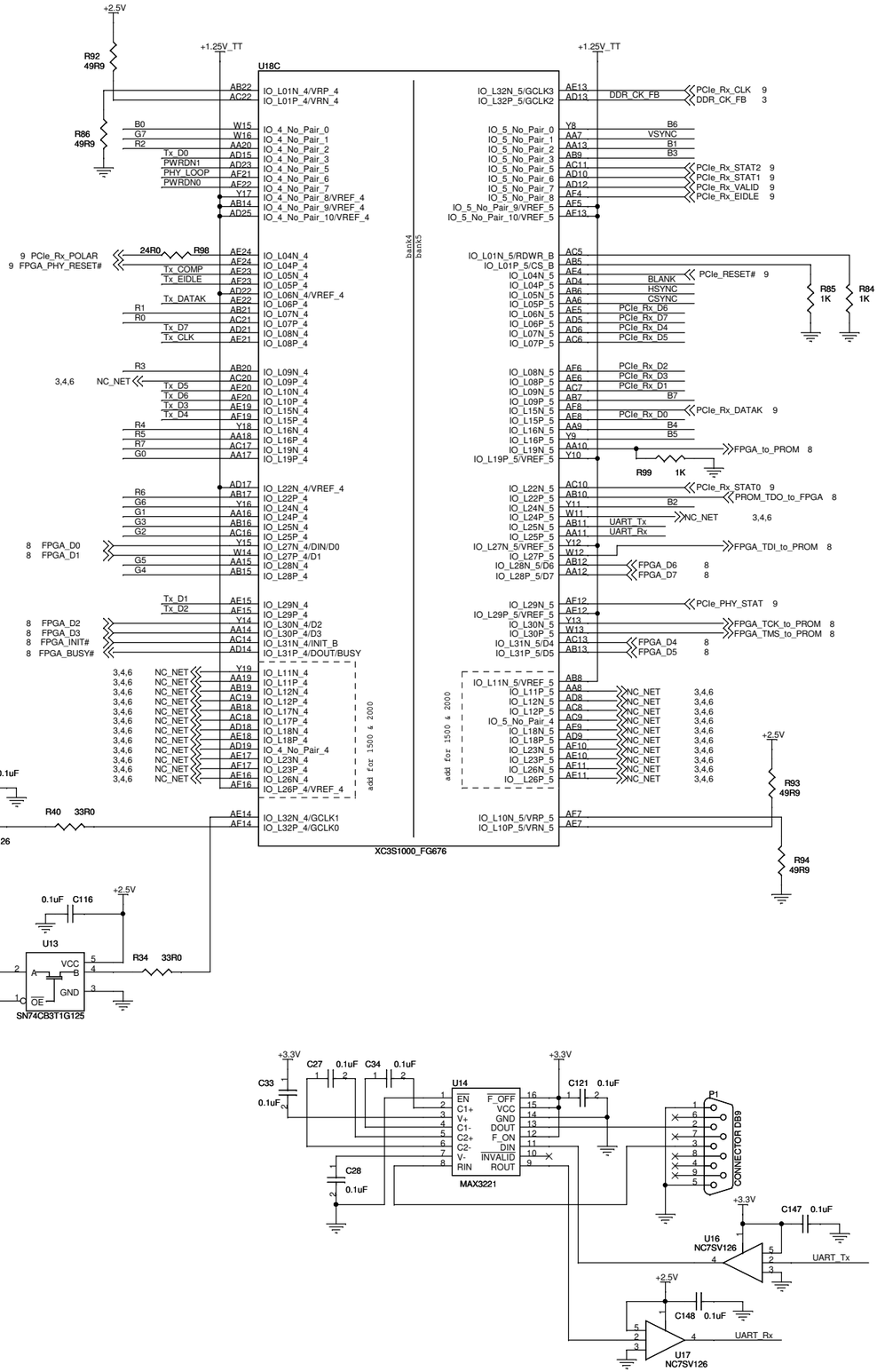
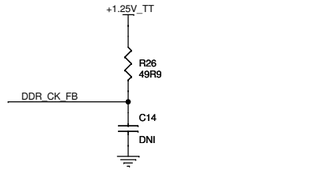
Title	Spartan-3 PCIe Starter Board	FPGA Banks 2 & 3
Size C	Document Number AES-SP3-PCIE-SCH	Rev 2.1
Date: Thursday, May 03, 2007	Sheet 4 of 13	



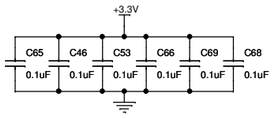
Place RP16 - RP23, R95 - R97 close to U18

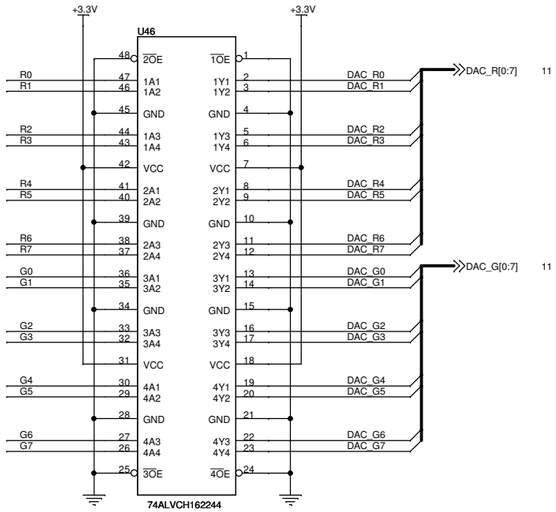


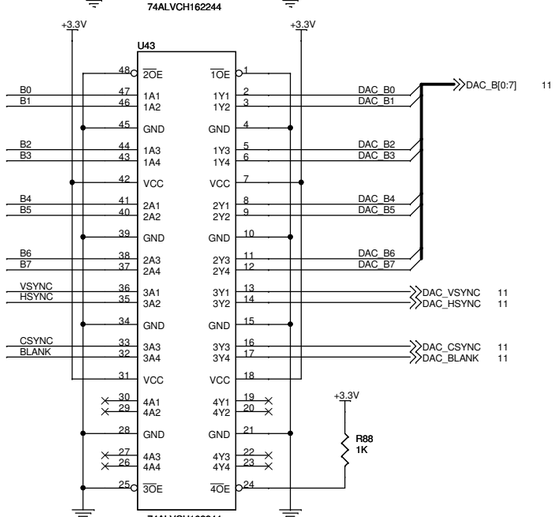


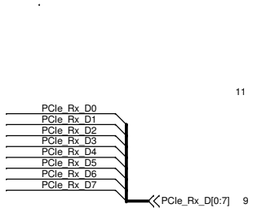


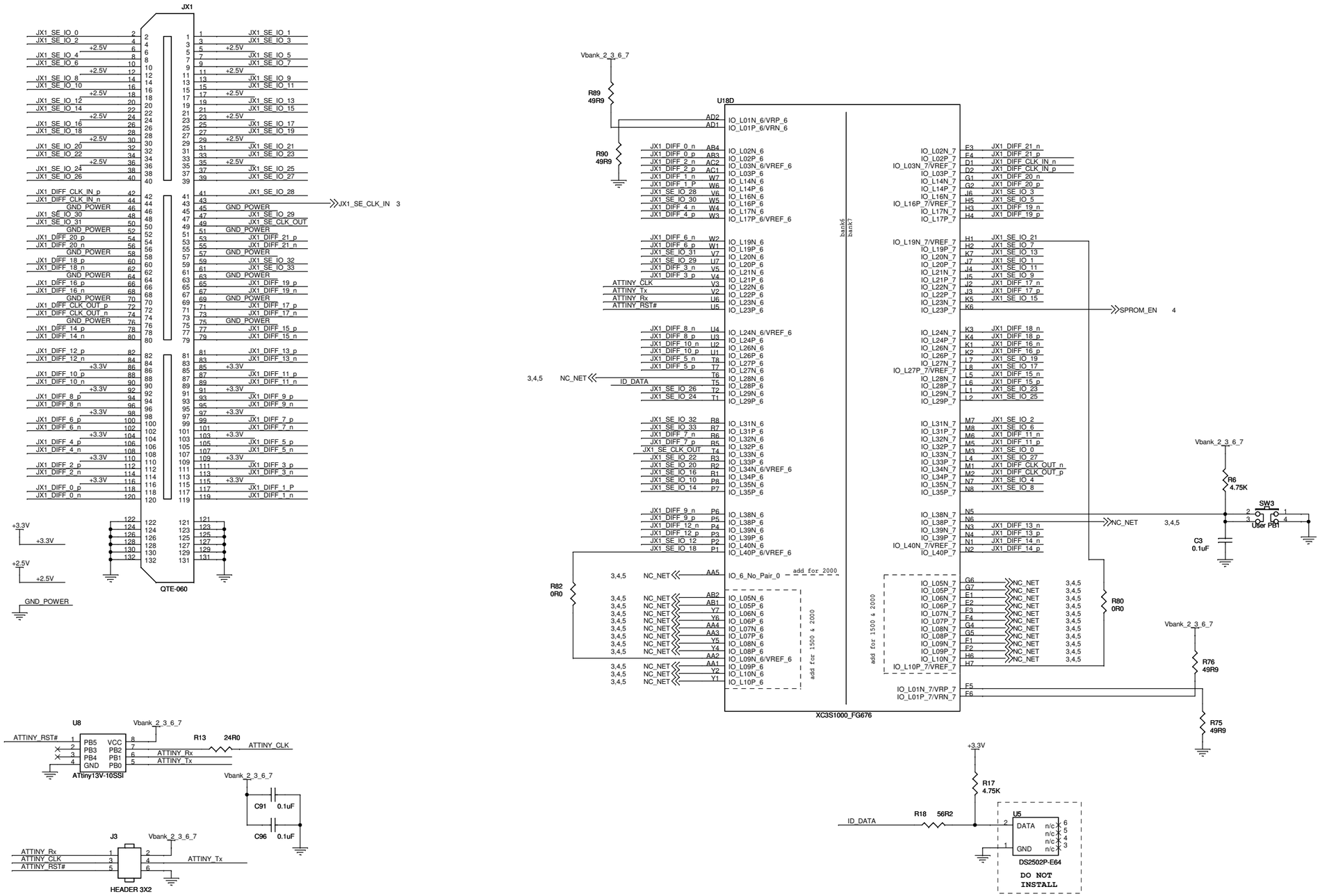
Match lengths of DDR traces, except DDR_CLK_FB make 2X the length











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Title: Spartan-3 PCIe Starter Board — FPGA Banks 6 & 7			
Size: C	Document Number: AES-SP3-PCIE-SCH		Rev: 2.1
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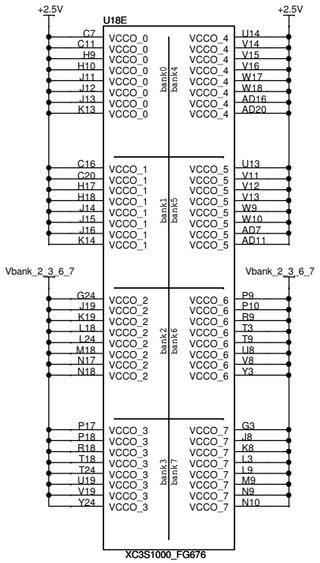
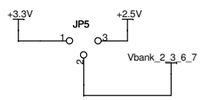
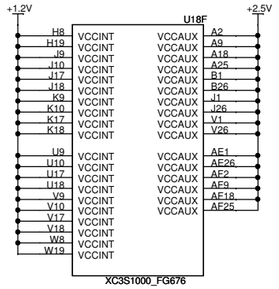
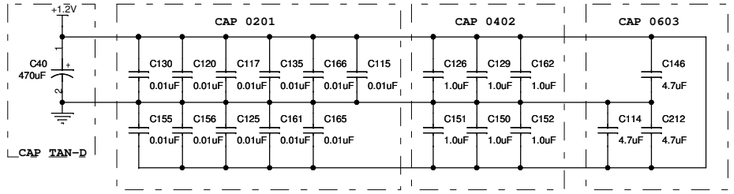
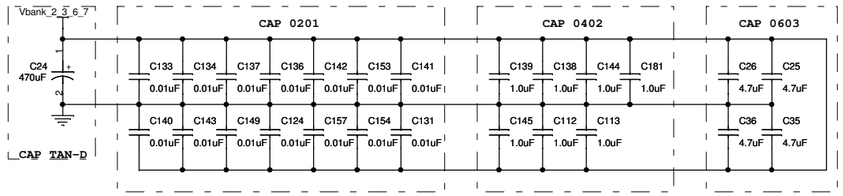


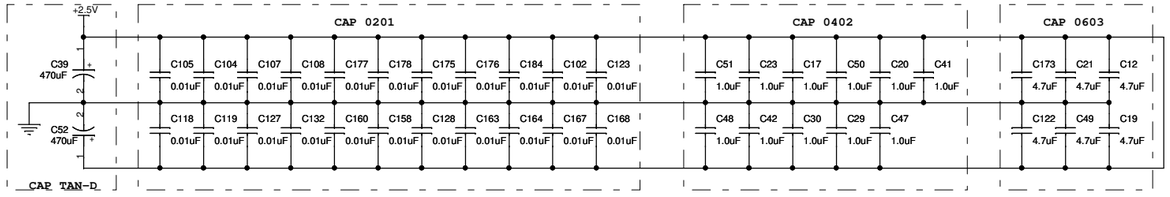
Bank 2, 3, 6, 7 VCCO Select

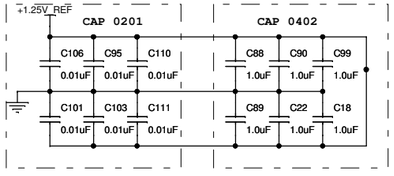


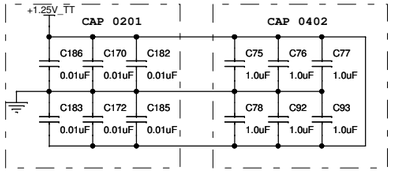












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Title: Spartan-3 PCIe Starter Board	FPGA Power		
Size: C	Document Number: AES-SP3-PCIE-SCH		Rev: 2.1
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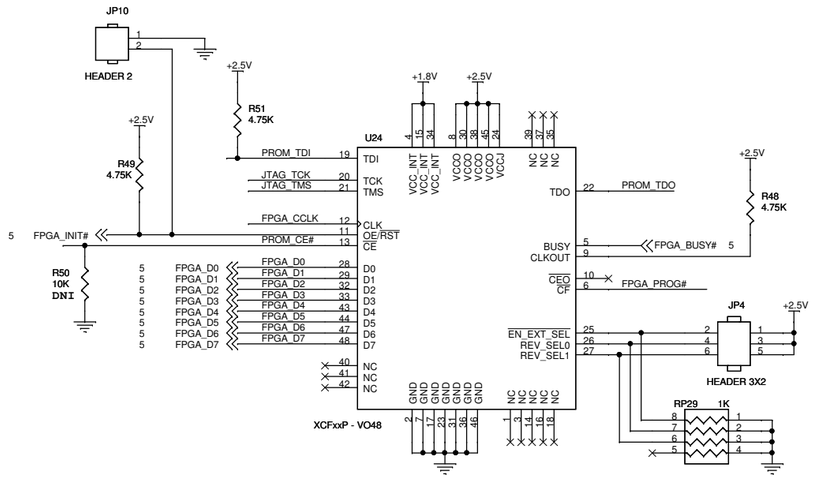
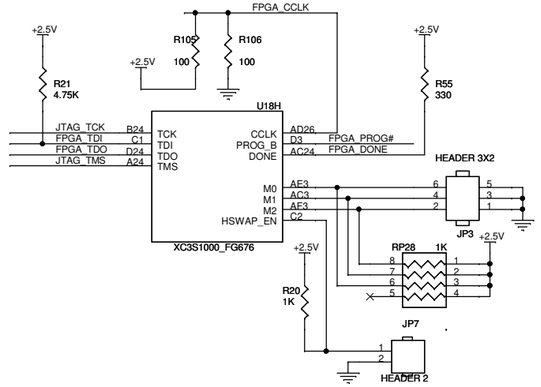
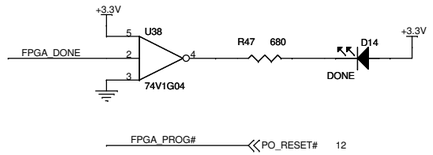
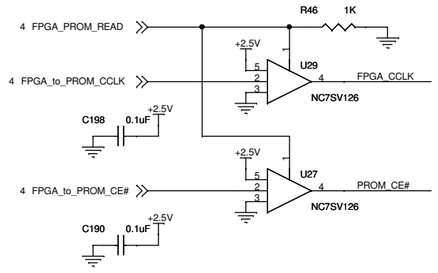


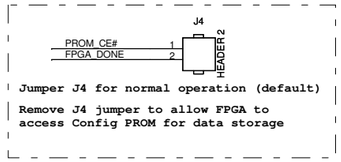




Configuration Mode	M0 (JP3 5:6)	M1 (JP3 3:4)	M2 (JP3 1:2)
Master Serial	0	0	0
Slave Serial	1	1	1
Master Parallel	1	1	0
Slave Parallel	0	1	1
JTAG	1	0	1

Note: With no shunts installed on JP3, M0 = M1 = M2 = 1 via RP28

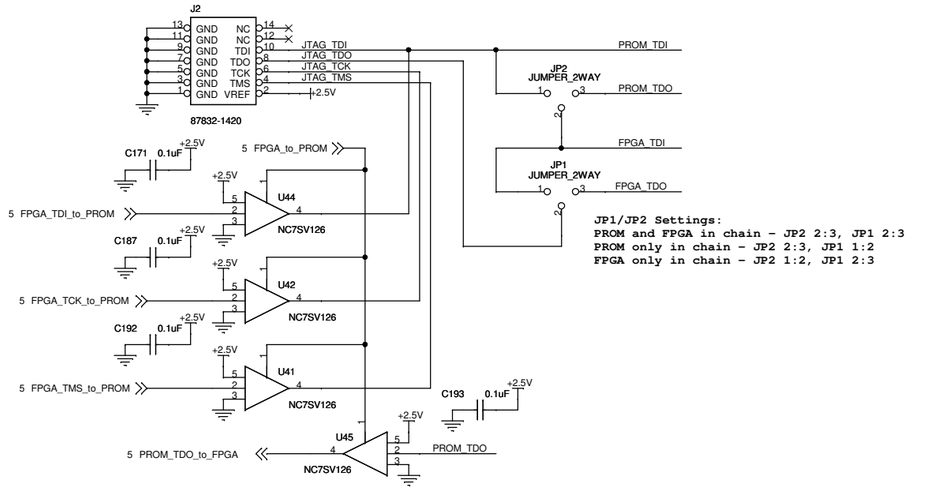




Jumper J4 for normal operation (default)

Remove J4 jumper to allow FPGA to access Config PROM for data storage

JTAG Parallel IV Connector



JP1/JP2 Settings:
PROM and FPGA in chain - JP2 2:3, JP1 2:3
PROM only in chain - JP2 2:3, JP1 1:2
FPGA only in chain - JP2 1:2, JP1 2:3

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Title: Spartan-3 PCIe Starter Board		FPGA Configuration	
Size: C	Document Number: AES-SP3-PCIE-SCH		Rev: 2.1
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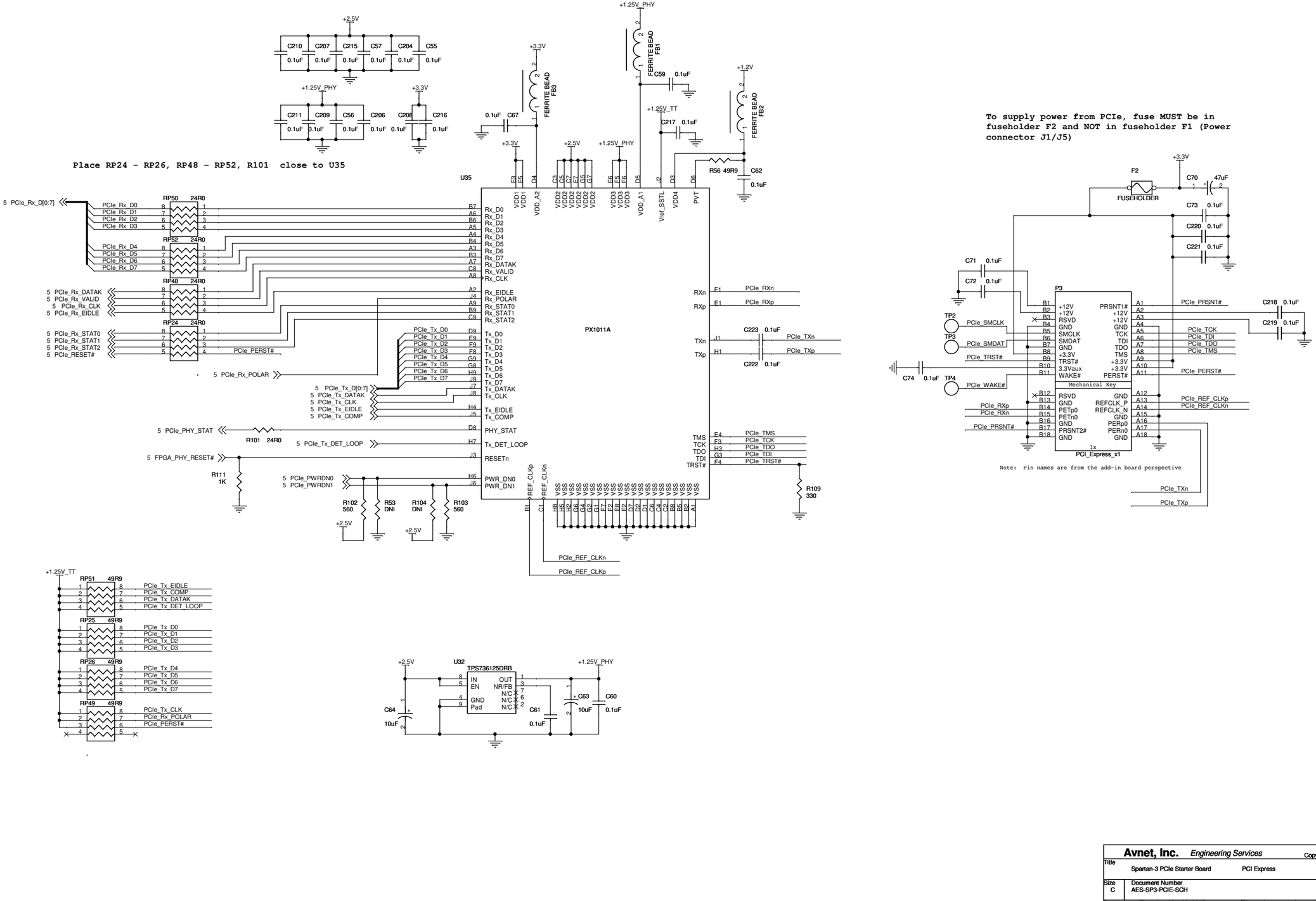
Place RP24 - RP26, RP48 - RP52, R101 close to U35

To supply power from PCIe, fuse MUST be in fuseholder F2 and NOT in fuseholder F1 (Power connector J1/J5)



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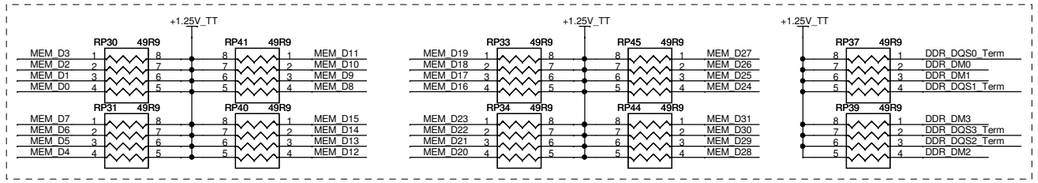
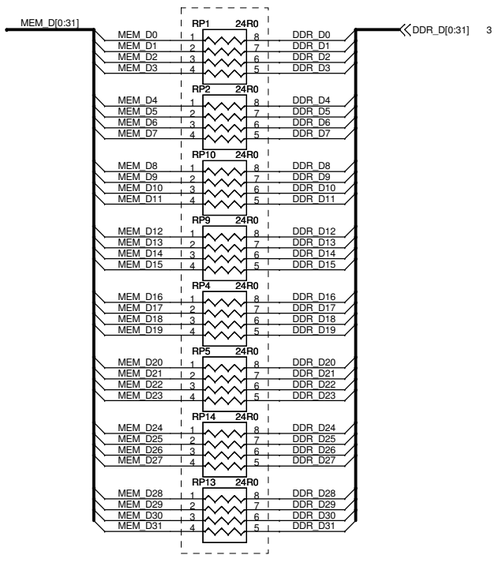
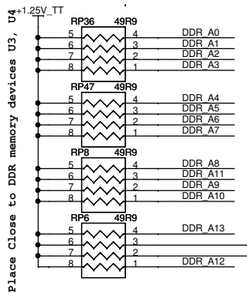
Install Terminators on Far Side of DDR memory devices U3 and U4

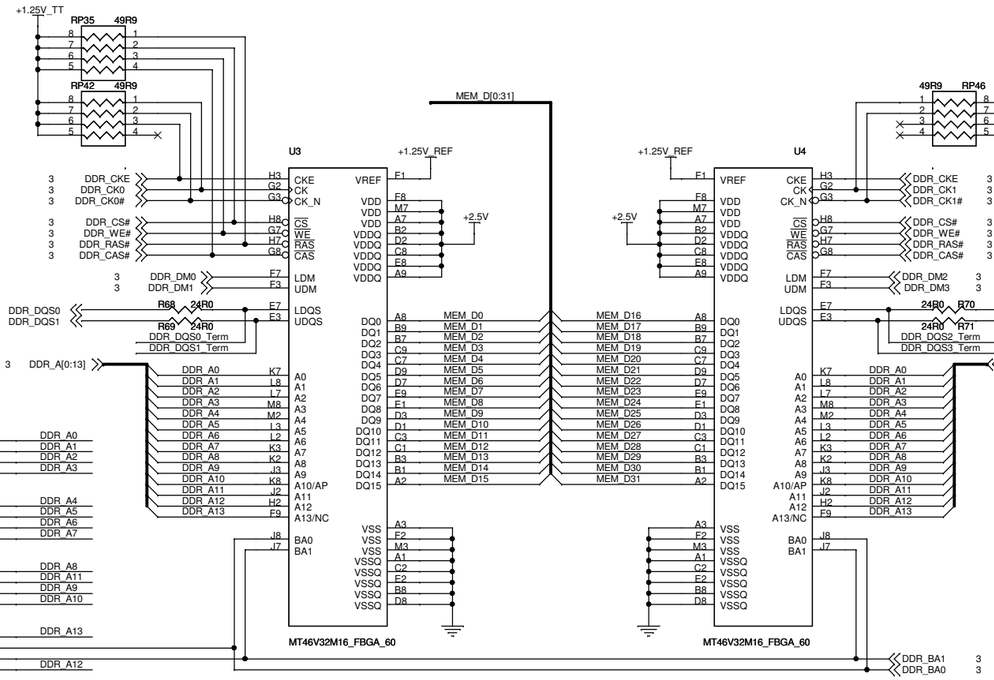


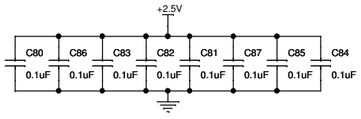
Place Close to DDR memory devices U3 and U4



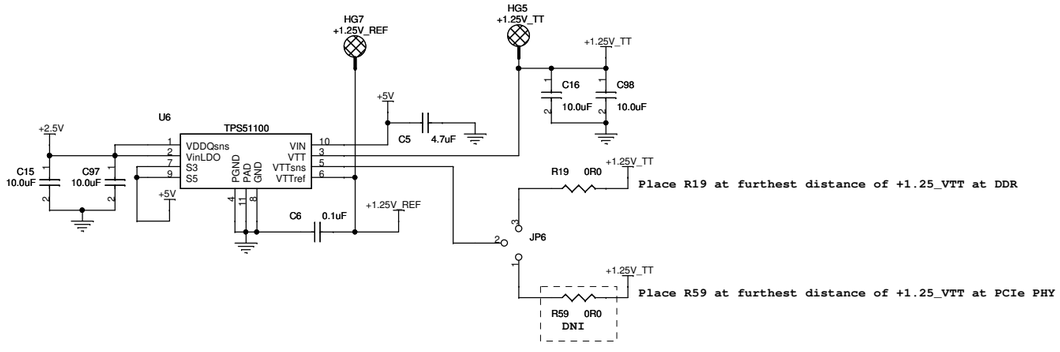
Place Close to DDR memory devices U3, U4







DDR Termination Voltage



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Title	Spartan-3 PCIe Starter Board DDR SDRAM	
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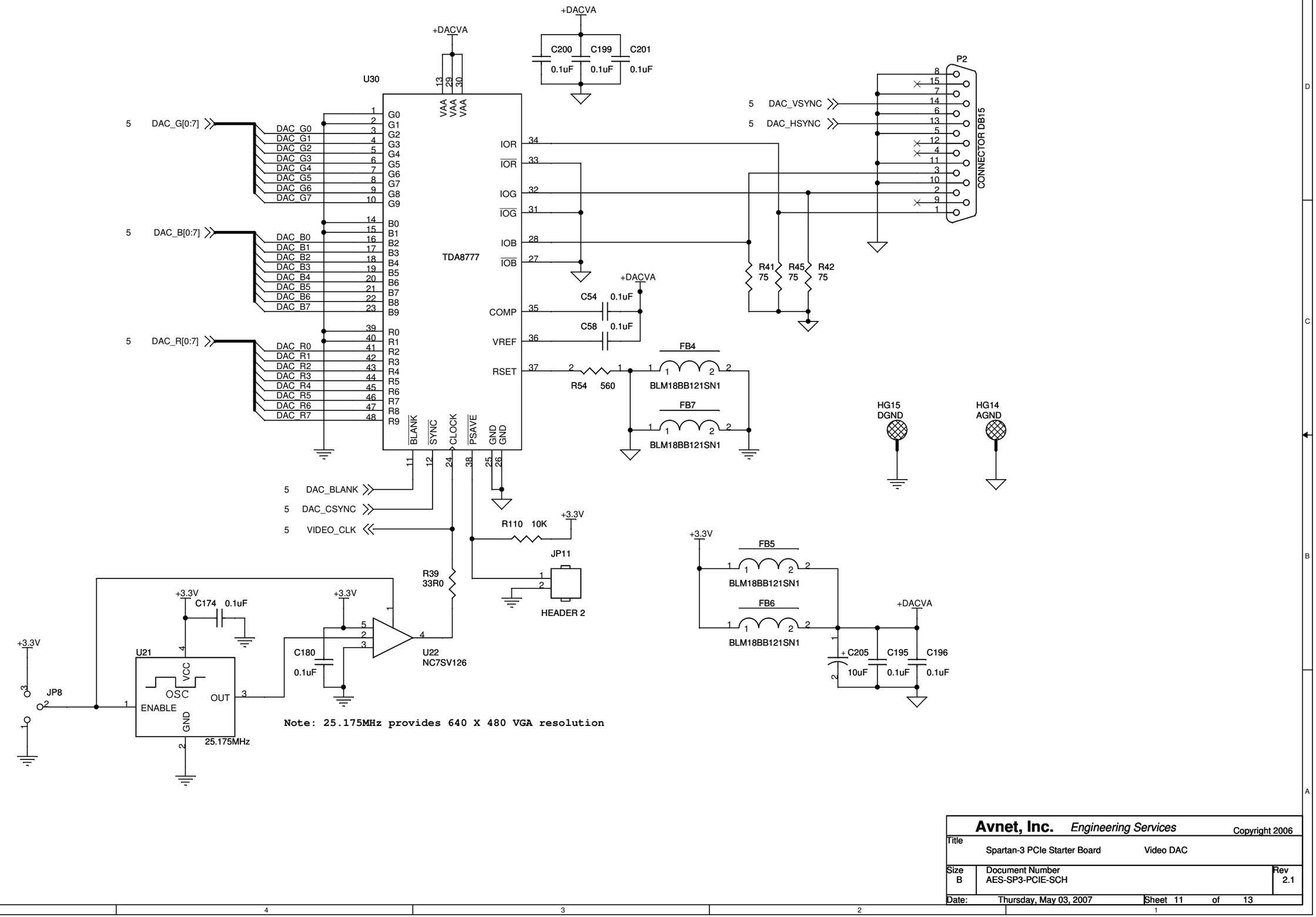

Note: 25.175MHz provides 640 X 480 VGA resolution

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Title	Spartan-3 PCIe Starter Board	Video DAC
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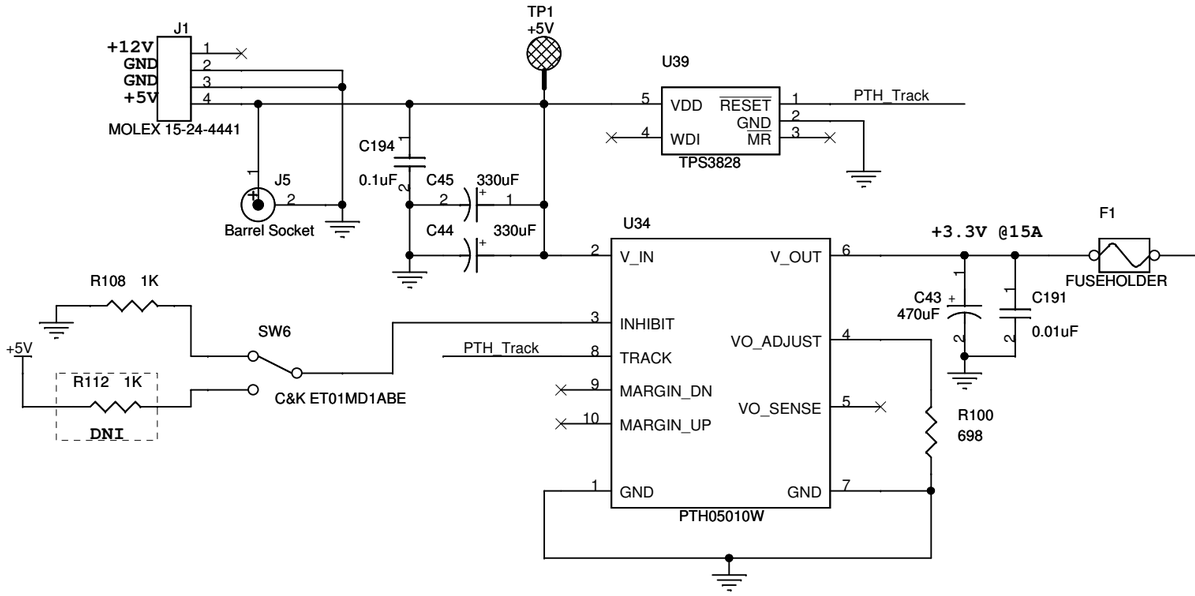
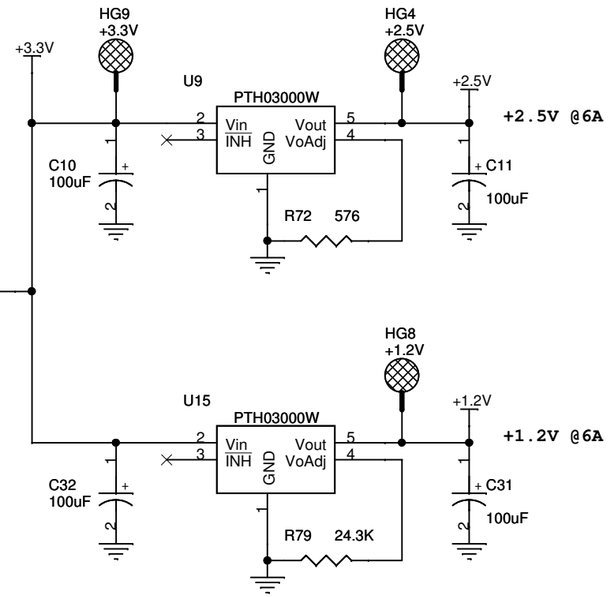
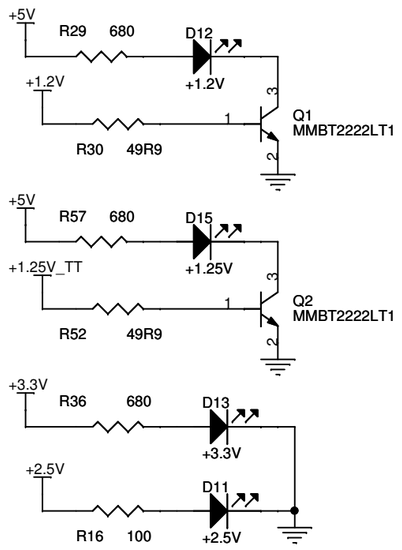
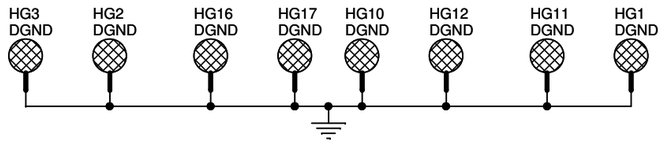
Input Power Vin = +5V Vdc

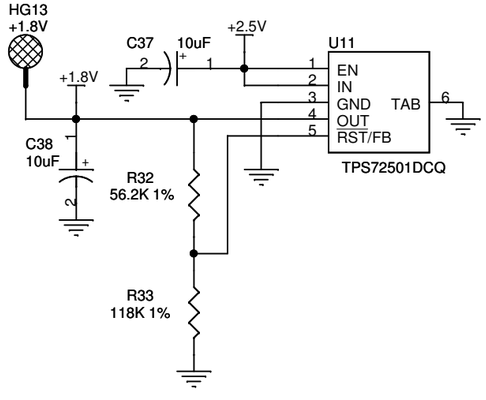
To supply power from J1 or J5, fuse MUST be in fuseholder F1 and NOT in fuseholder F2 (PCIe)

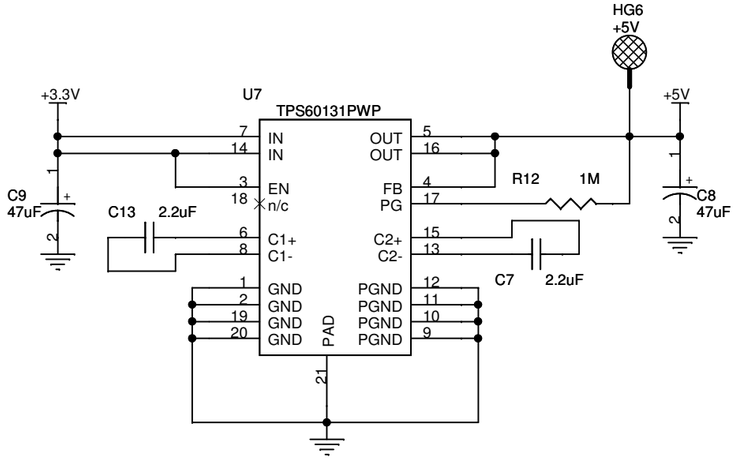


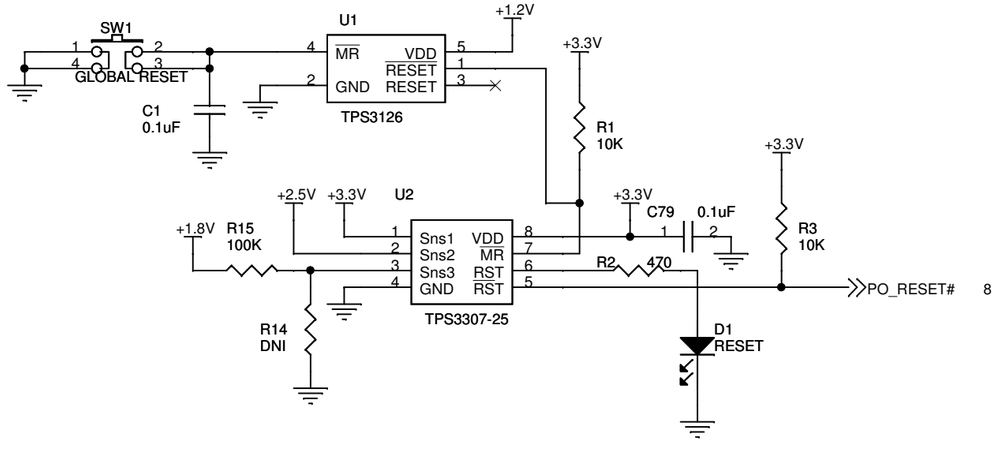












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Title: Spartan-3 PCIe Starter Board	Board Power	
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Changes Rev1 to Rev2:

3/27/06 – Swapped power and ground connections to power switch SW6 to match PCB silk-screen (up = ON)

Clarification:

5/02/07 – Changed names of pin pairs B14/B15 and A16/A17 on PCIe connector P3 to match PCIe CEM Spec.

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Size: A	Document Number: AES-SP3-PCIE-SCH	Rev: 2.1
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