

Spartan-3 PCIe Starter Board

Avnet Engineering Services

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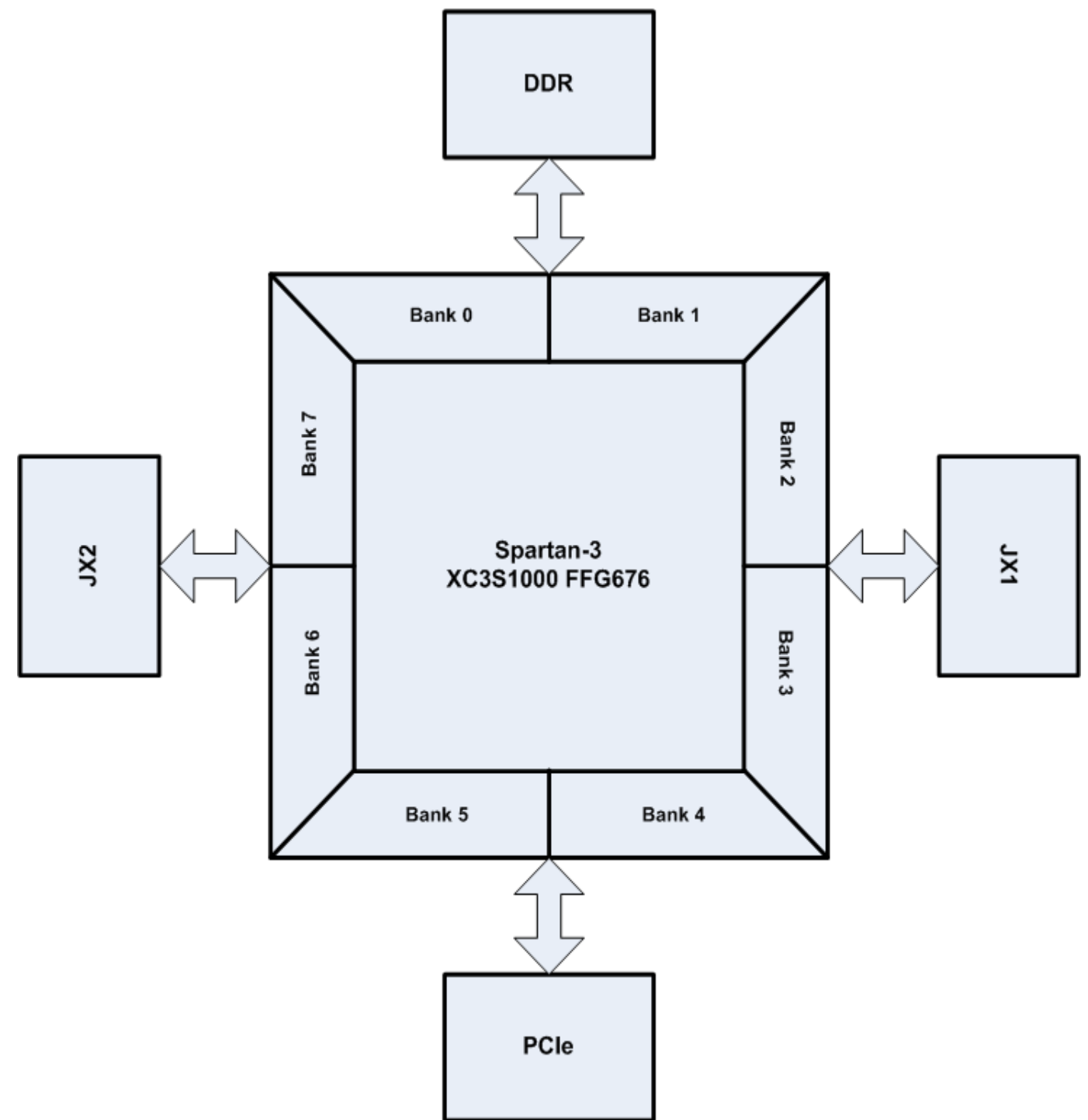
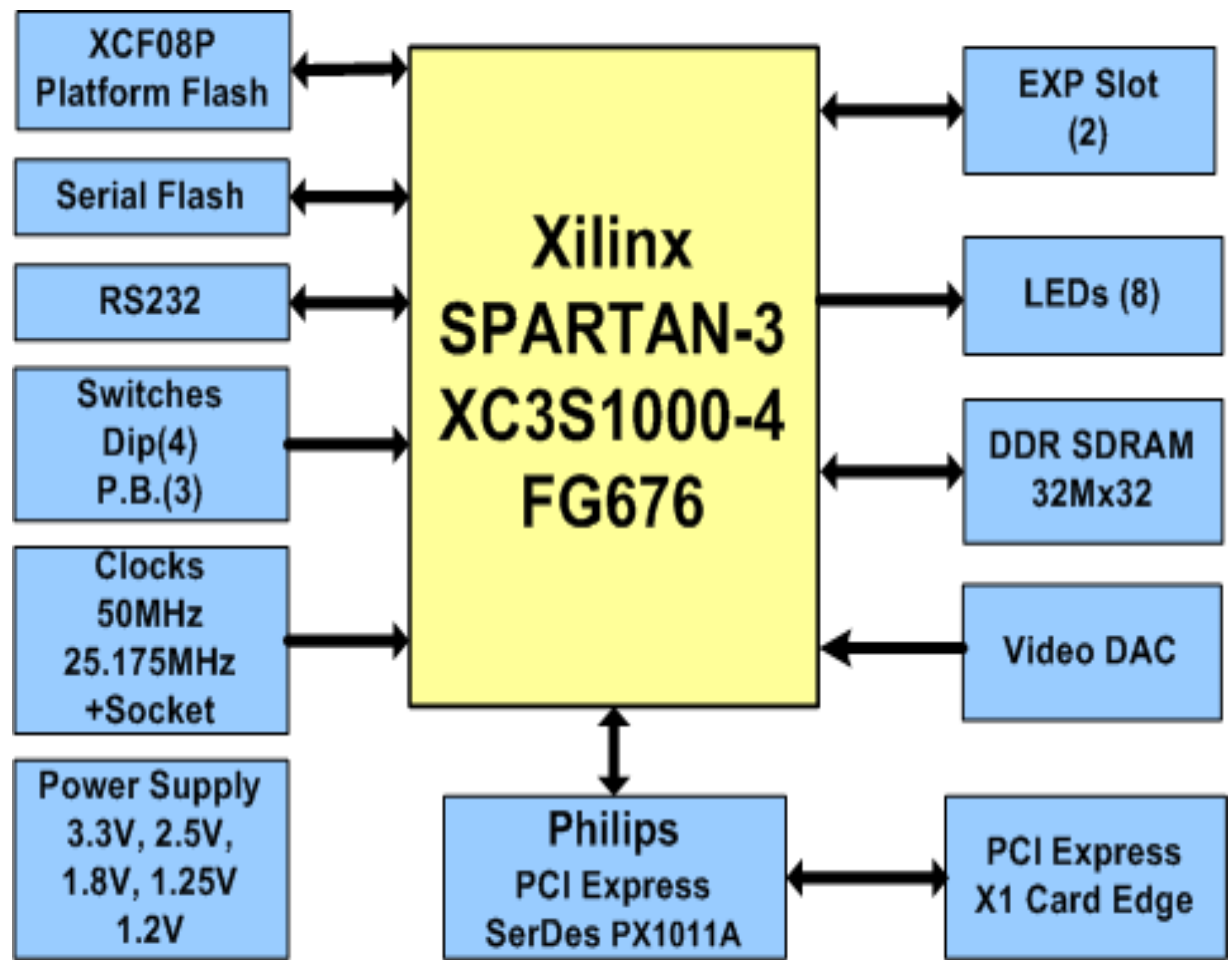
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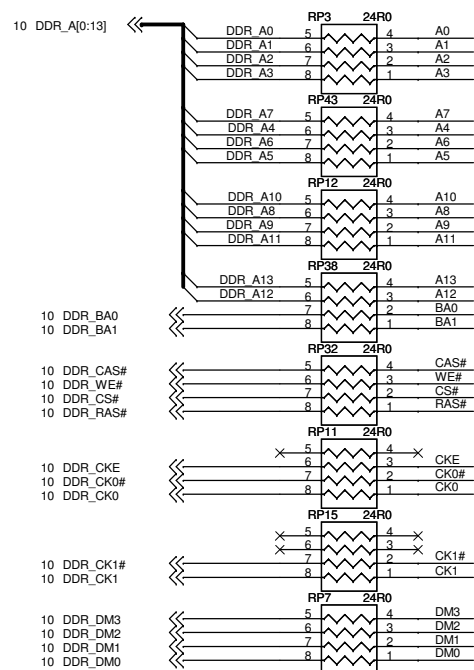
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05/03/07

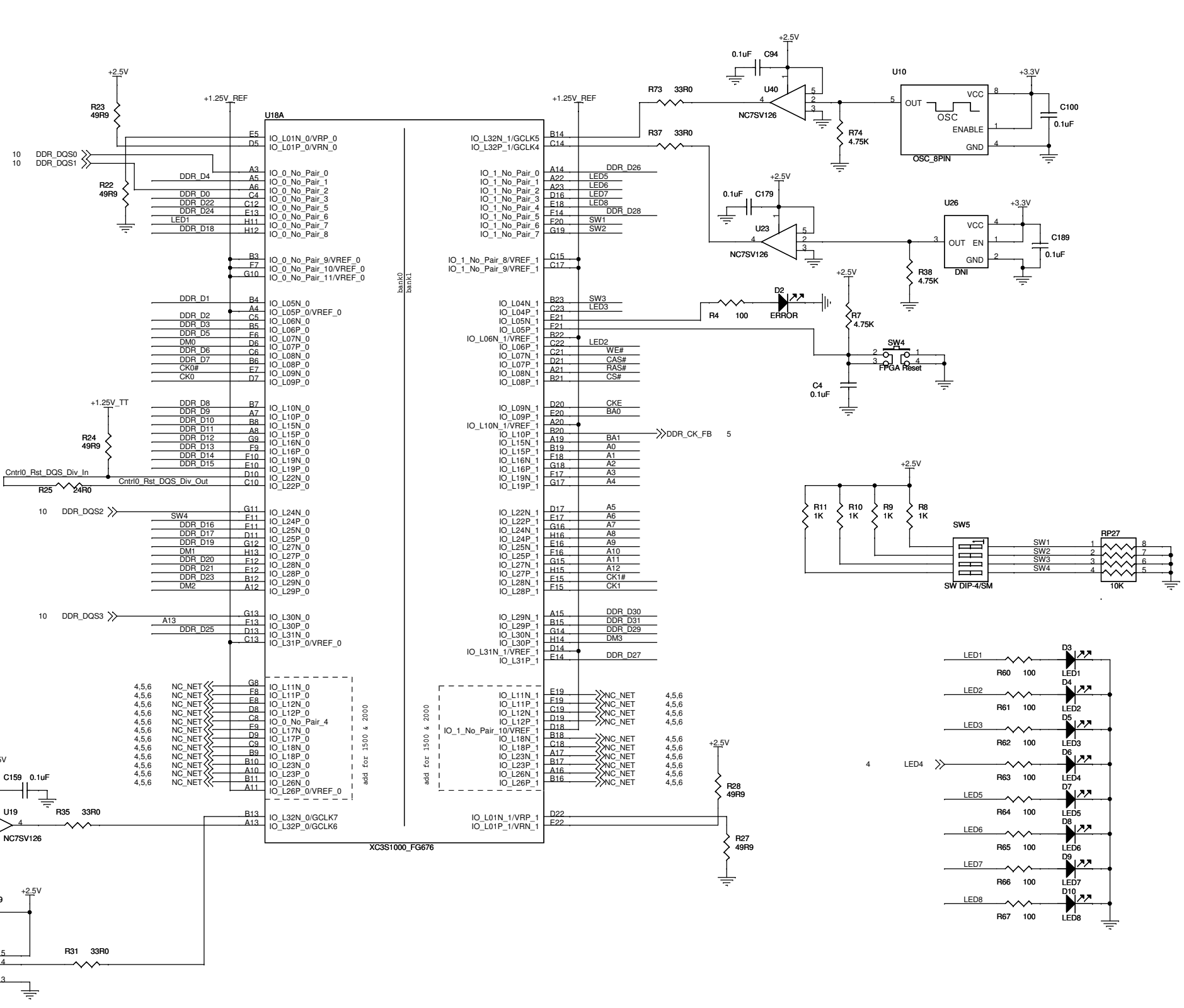
REVISION 2.1

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Title	Spartan-3 PCIe Starter Board	Cover sheet
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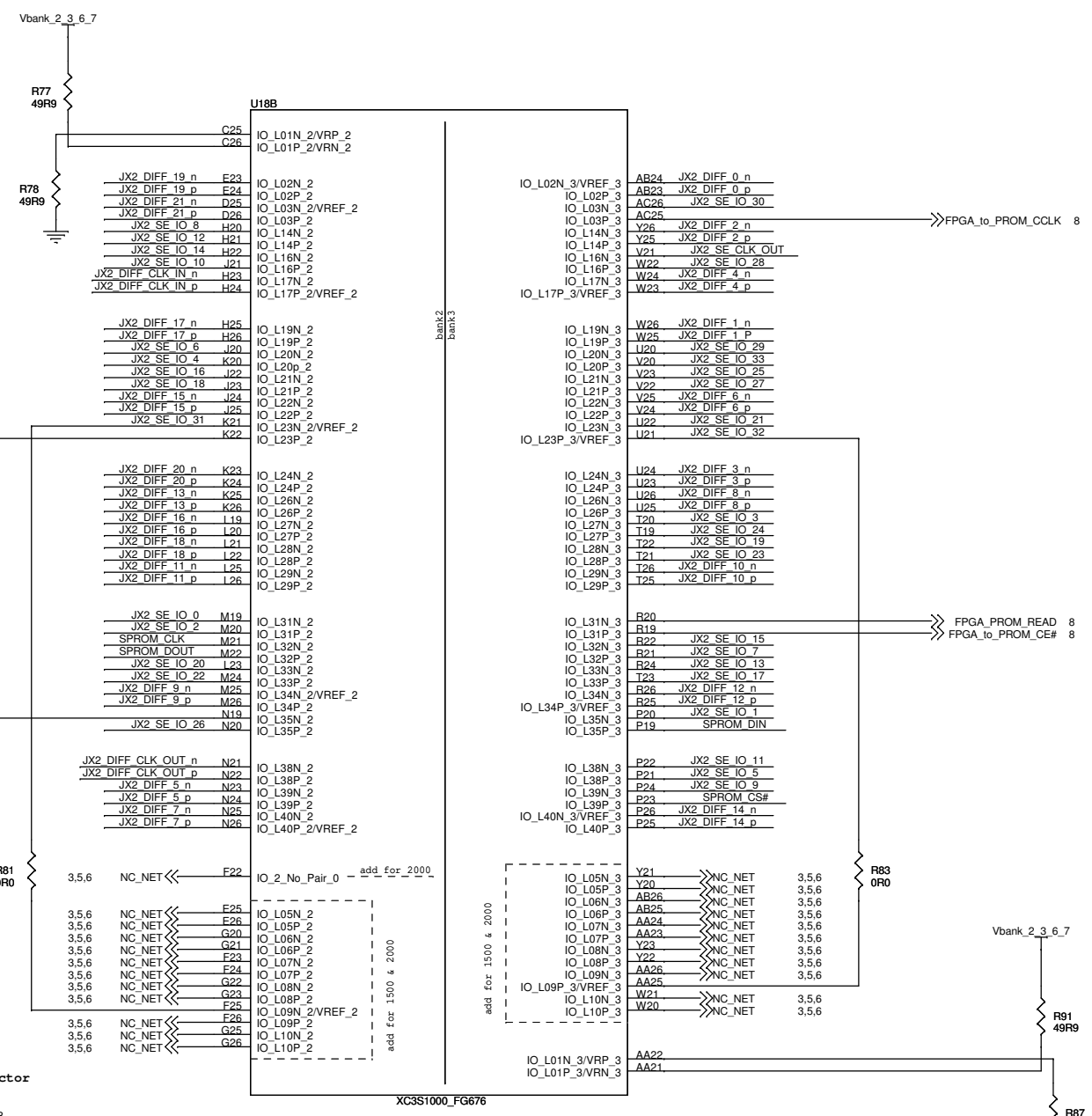
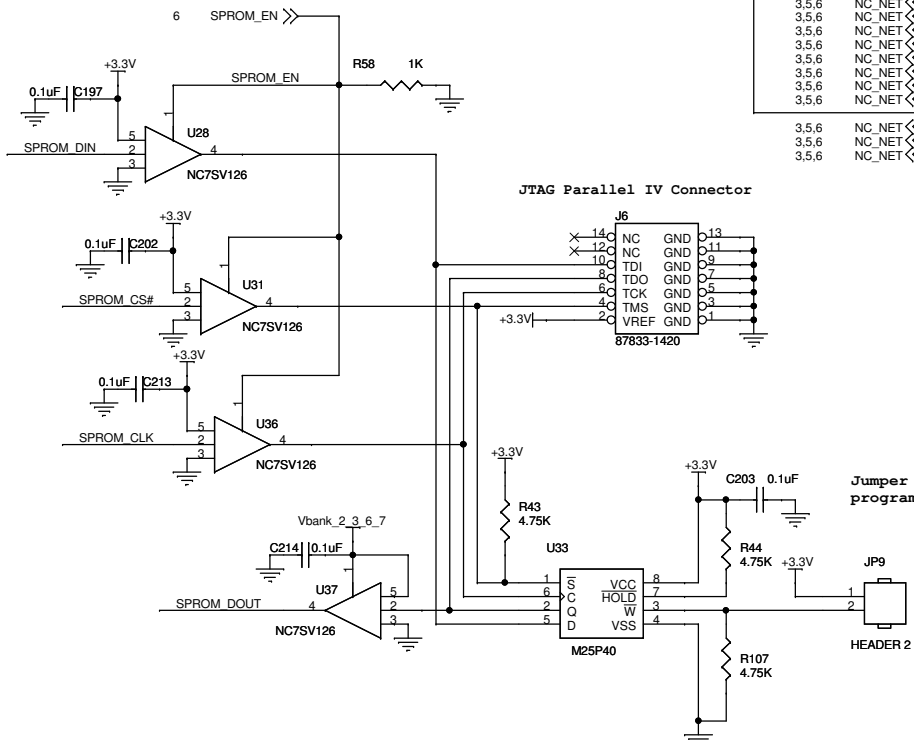
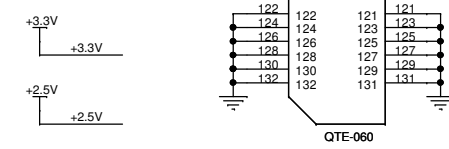


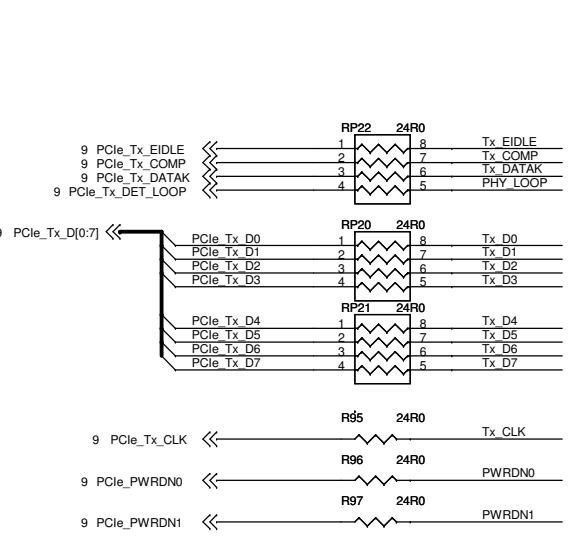


Place R25 close to U18.C10.
Total length of U18.C10 to R25 to U18.D10 is 2X the routed DDR Clock length (DDR_CK0, DDR_CK1).

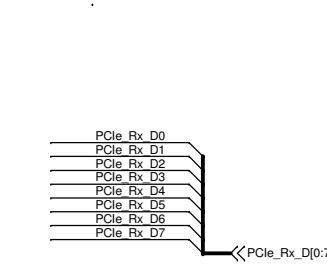
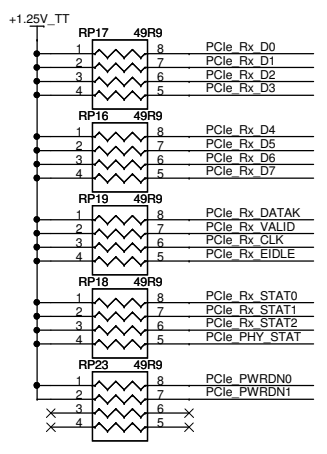


JX2 SE IO 0	2	2	1	JX2 SE IO 1
JX2 SE IO 2	4	4	3	JX2 SE IO 3
	6	6	5	+2.5V
JX2 SE IO 4	8	8	7	JX2 SE IO 5
JX2 SE IO 6	10	10	9	JX2 SE IO 7
	12	12	11	+2.5V
JX2 SE IO 8	14	14	13	JX2 SE IO 9
JX2 SE IO 10	16	16	15	JX2 SE IO 11
	18	18	17	+2.5V
JX2 SE IO 12	20	20	19	JX2 SE IO 13
JX2 SE IO 14	22	22	21	JX2 SE IO 15
	24	24	23	+2.5V
JX2 SE IO 16	26	26	25	JX2 SE IO 17
JX2 SE IO 18	28	28	27	JX2 SE IO 19
	30	30	29	+2.5V
JX2 SE IO 20	32	32	31	JX2 SE IO 21
JX2 SE IO 22	34	34	33	JX2 SE IO 23
	36	36	35	+2.5V
JX2 SE IO 24	38	38	37	JX2 SE IO 25
JX2 SE IO 26	40	40	39	JX2 SE IO 27
	42	42	41	JX2 SE IO 28
JX2 DIFF CLK IN p	44	44	43	GND POWER
JX2 DIFF CLK IN n	46	46	45	JX2 SE IO 29
GND POWER	48	48	47	JX2 SE CLK OUT
JX2 SE IO 30	50	50	49	GND POWER
JX2 SE IO 31	52	52	51	JX2 DIFF 21 p
GND POWER	54	54	53	JX2 DIFF 21 n
JX2 DIFF 20 p	56	56	55	GND POWER
JX2 DIFF 20 n	58	58	57	GND POWER
GND POWER	60	60	59	JX2 SE IO 32
JX2 DIFF 18 p	62	62	61	JX2 SE IO 33
JX2 DIFF 18 n	64	64	63	GND POWER
GND POWER	66	66	65	JX2 DIFF 19 p
JX2 DIFF 16 p	68	68	67	JX2 DIFF 19 n
JX2 DIFF 16 n	70	70	69	GND POWER
GND POWER	72	72	71	JX2 DIFF 17 p
JX2 DIFF CLK OUT p	74	74	73	JX2 DIFF 17 n
JX2 DIFF CLK OUT n	76	76	75	GND POWER
GND POWER	78	78	77	JX2 DIFF 15 p
JX2 DIFF 14 p	80	80	79	JX2 DIFF 15 n
JX2 DIFF 14 n	82	82	81	JX2 DIFF 13 p
JX2 DIFF 12 p	84	84	83	JX2 DIFF 13 n
JX2 DIFF 12 n	86	86	85	+3.3V
JX2 DIFF 10 p	88	88	87	JX2 DIFF 11 p
JX2 DIFF 10 n	90	90	89	JX2 DIFF 11 n
	92	92	91	+3.3V
JX2 DIFF 8 p	94	94	93	JX2 DIFF 9 p
JX2 DIFF 8 n	96	96	95	JX2 DIFF 9 n
	98	98	97	+3.3V
JX2 DIFF 6 p	100	100	99	JX2 DIFF 7 p
JX2 DIFF 6 n	102	102	101	JX2 DIFF 7 n
	104	104	103	+3.3V
JX2 DIFF 4 p	106	106	105	JX2 DIFF 5 p
JX2 DIFF 4 n	108	108	107	JX2 DIFF 5 n
	110	110	109	+3.3V
JX2 DIFF 2 p	112	112	111	JX2 DIFF 3 p
JX2 DIFF 2 n	114	114	113	JX2 DIFF 3 n
	116	116	115	+3.3V
JX2 DIFF 0 p	118	118	117	JX2 DIFF 1 p
JX2 DIFF 0 n	120	120	119	JX2 DIFF 1 n

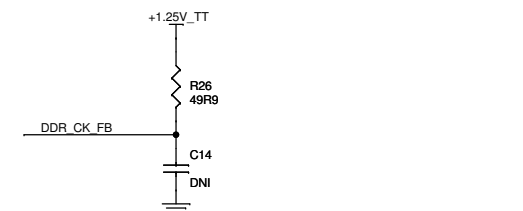
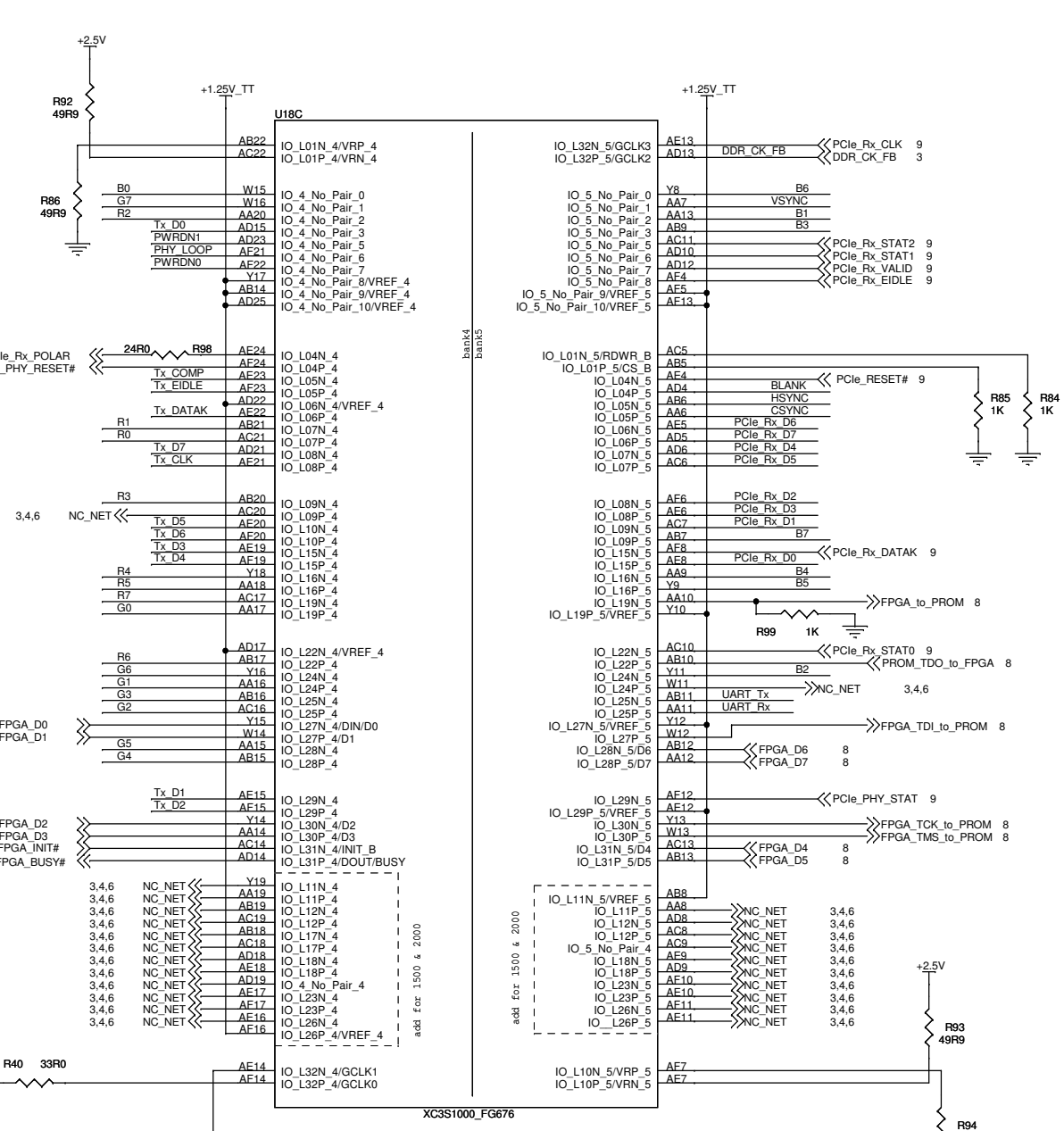
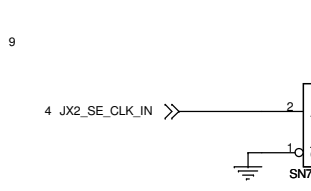




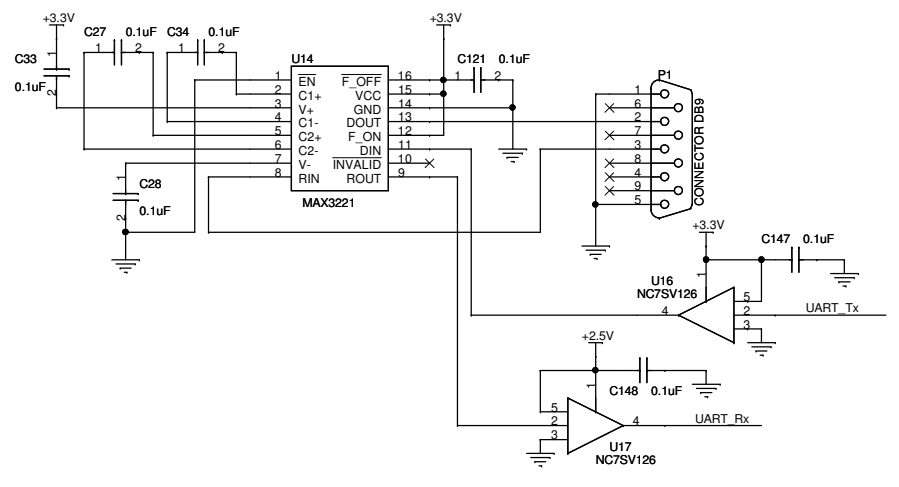
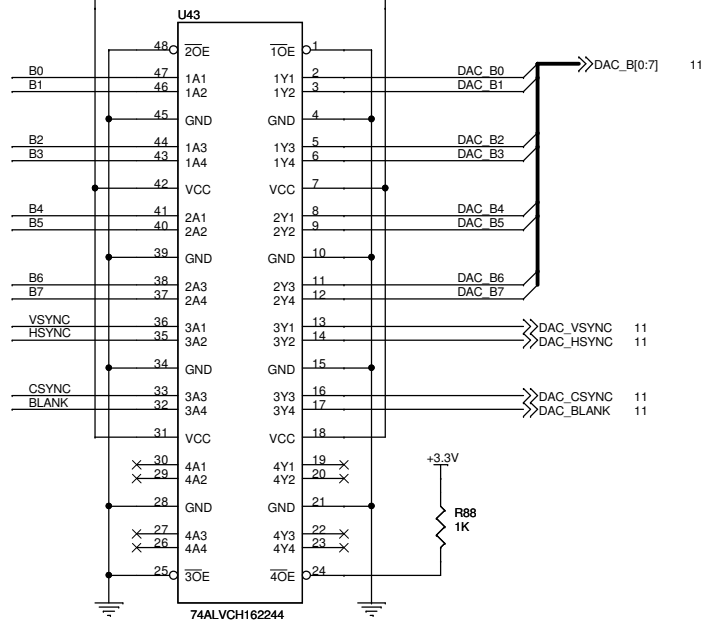
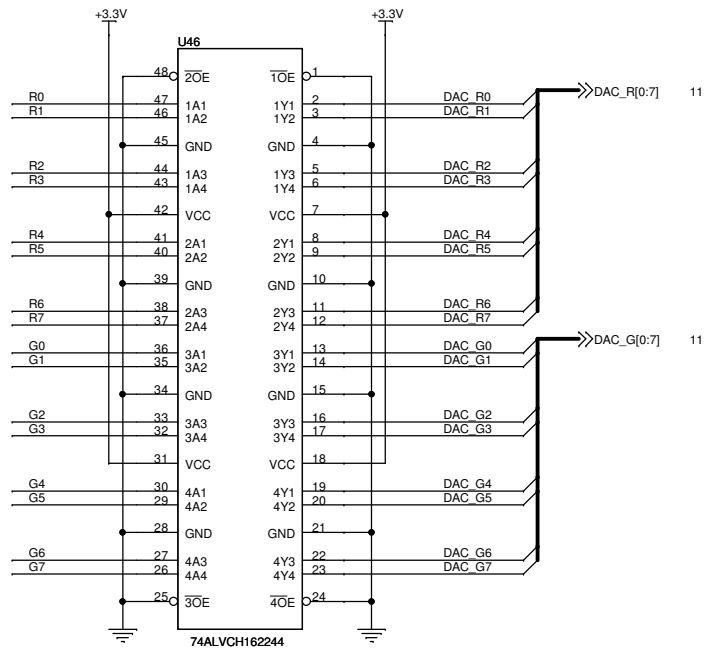
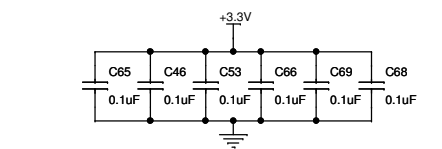
Place RP16 - RP23, R95 - R97 close to U18

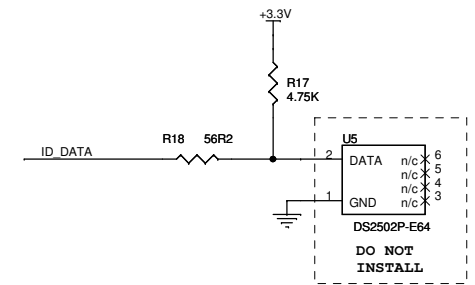
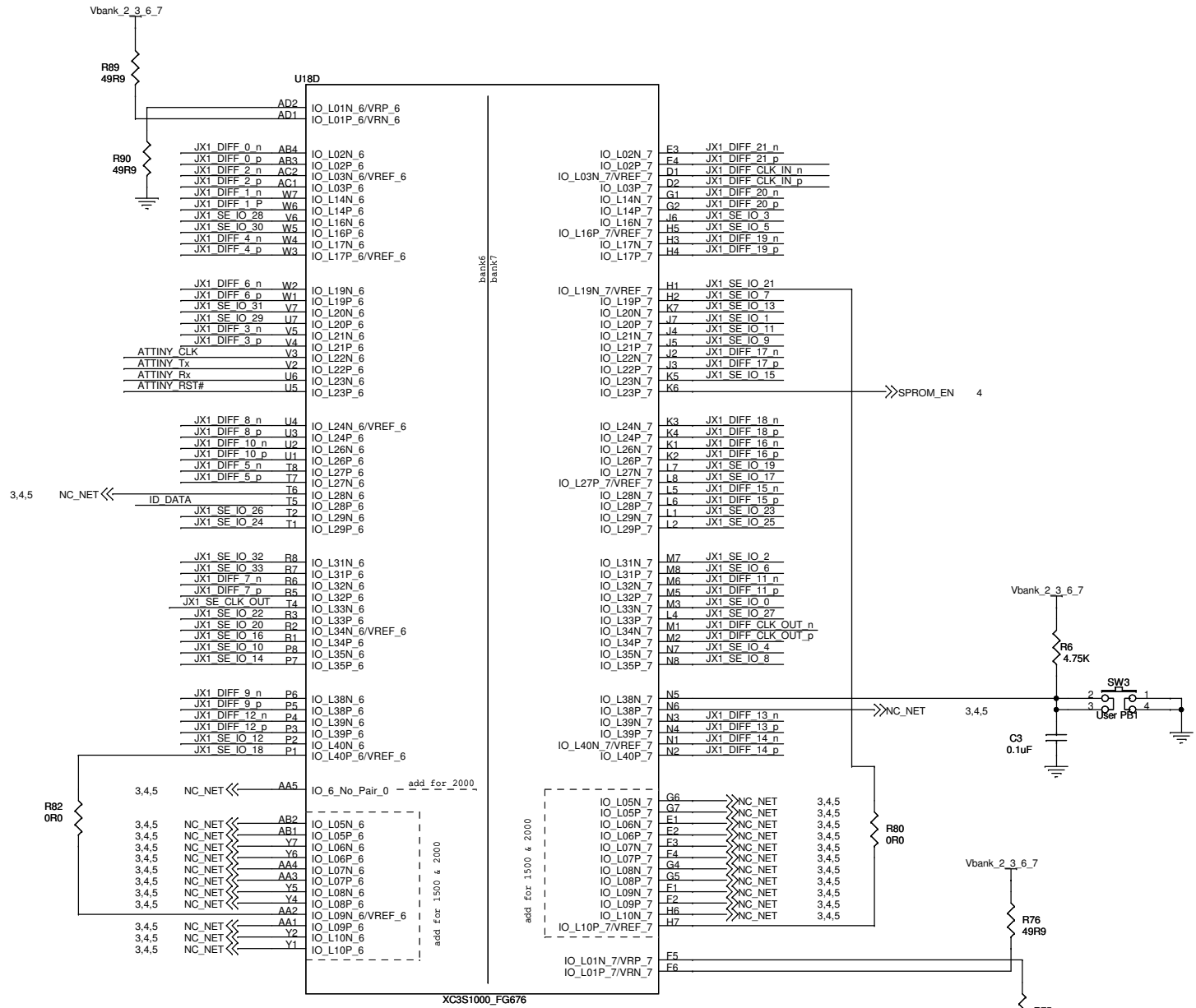
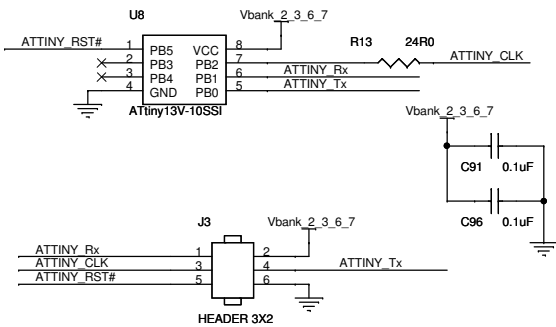
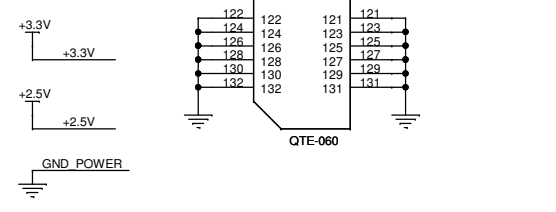
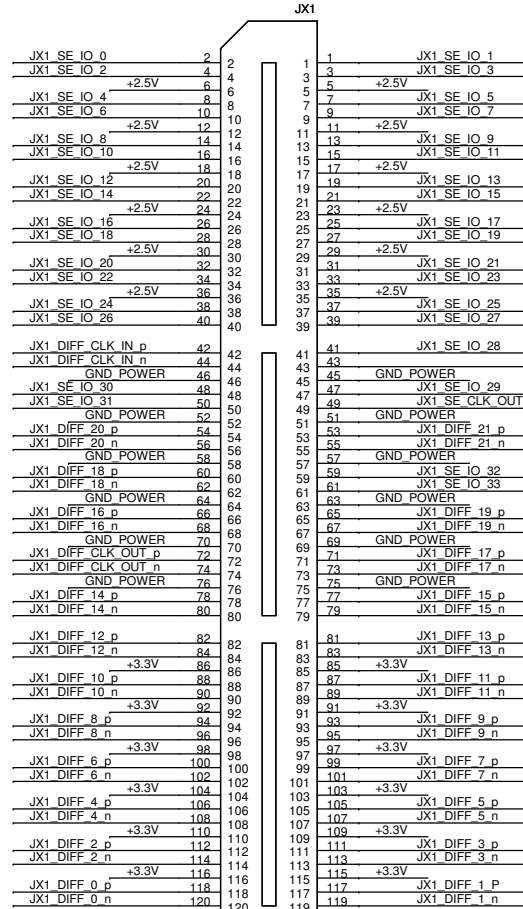


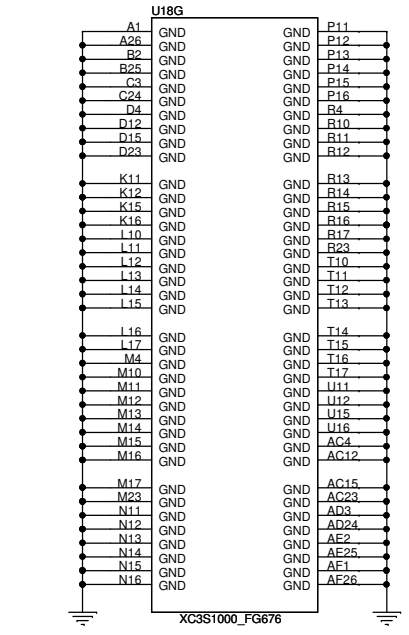
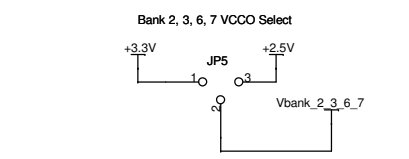
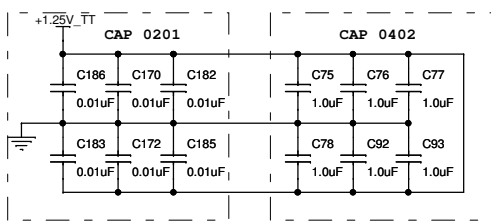
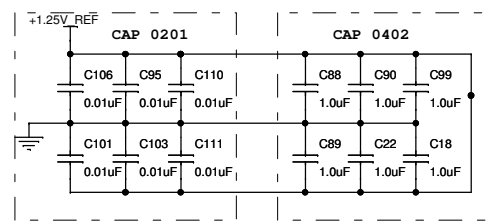
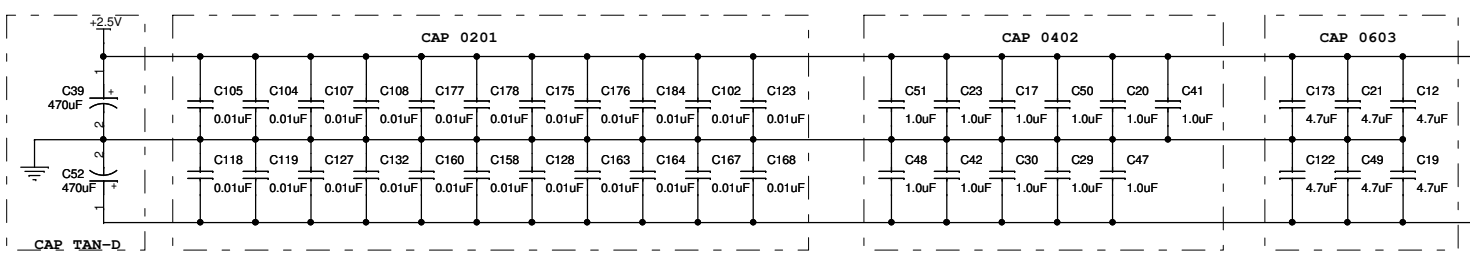
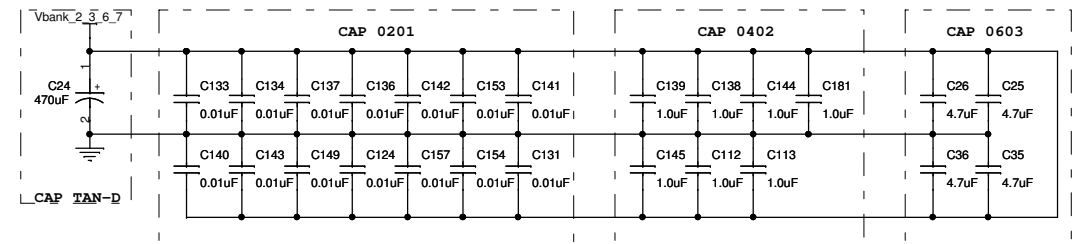
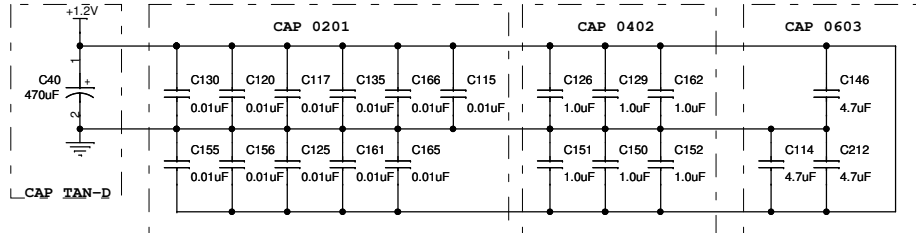
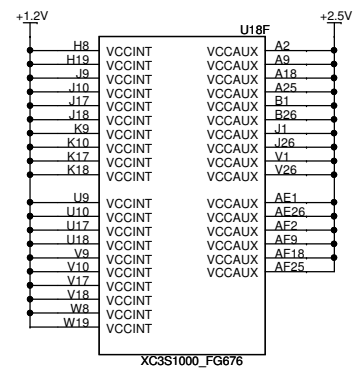
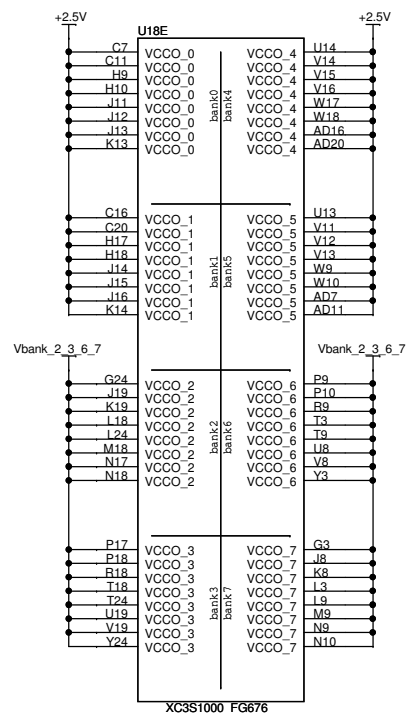
25.175MHz clock for VGA resolution (DAC)

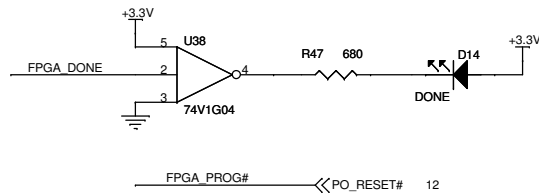
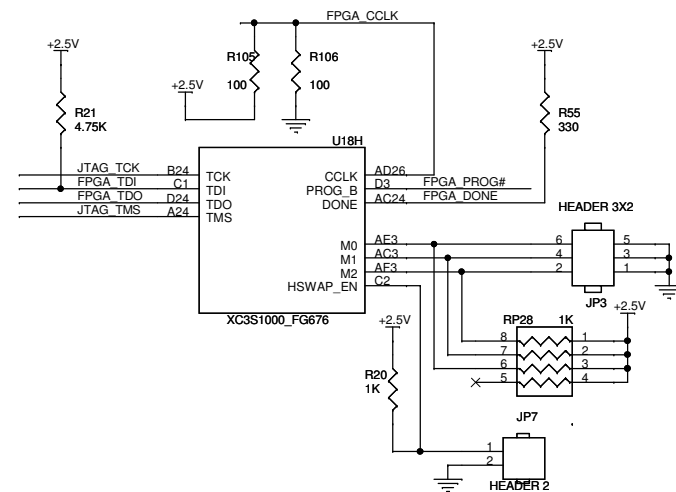
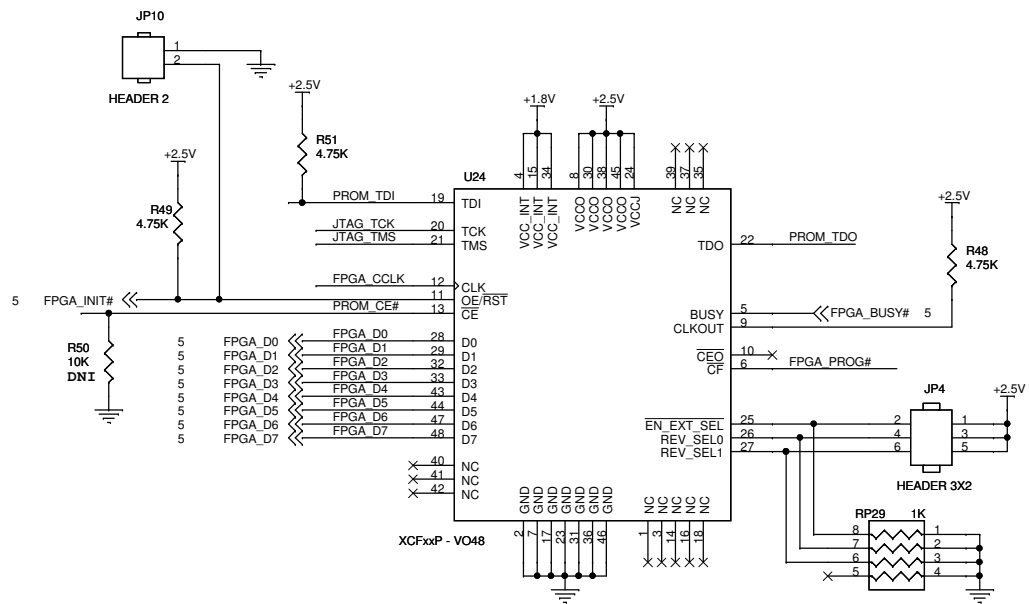


Match lengths of DDR traces, except DDR_CLK_FB make 2X the length



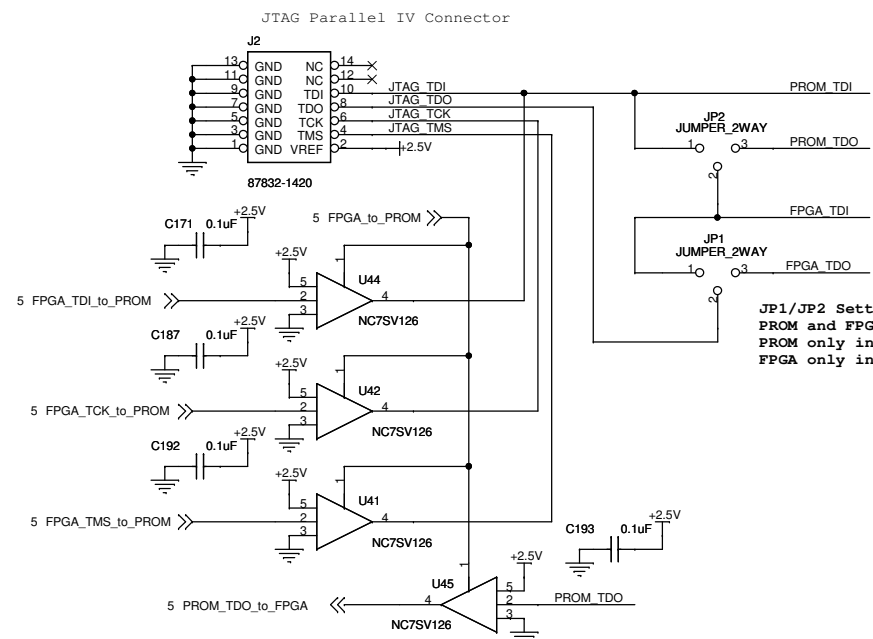
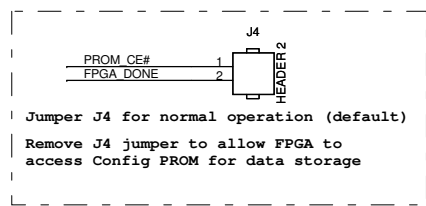
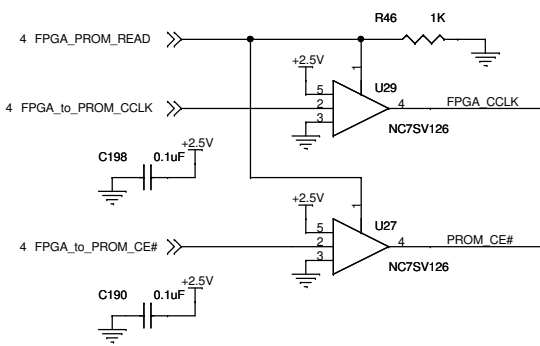




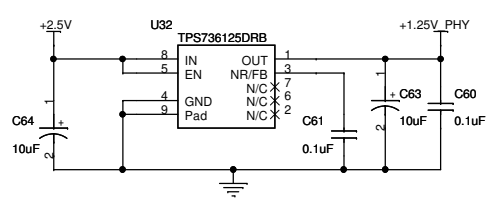
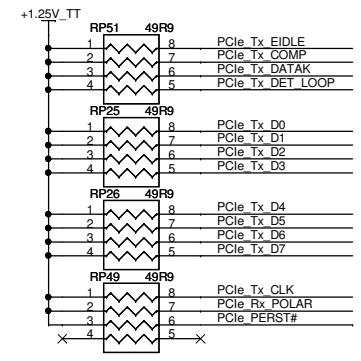
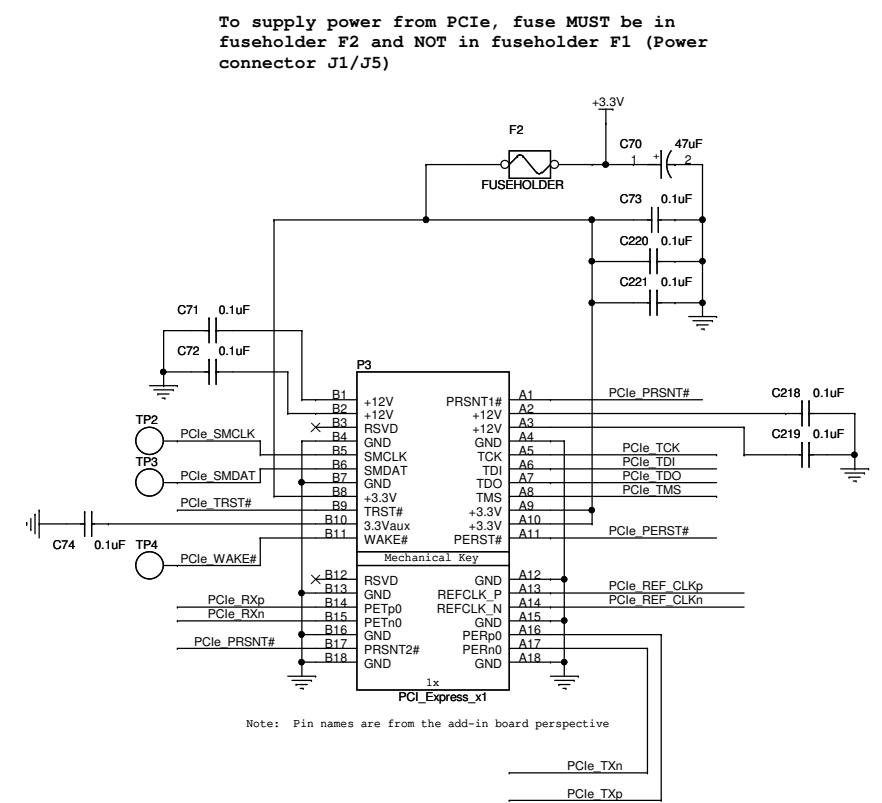
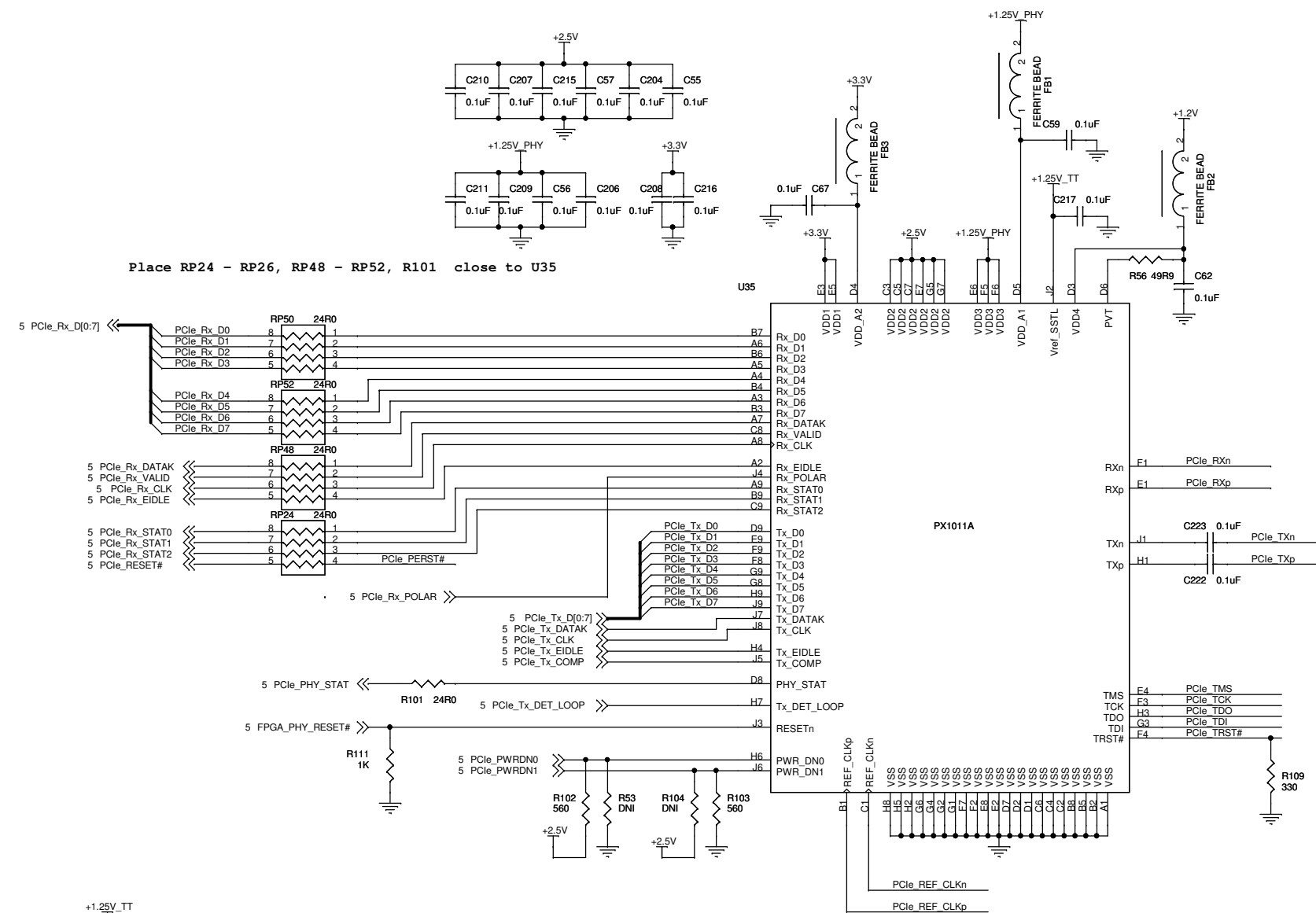


Configuration Mode	M0 (JP3 5:6)	M1 (JP3 3:4)	M2 (JP3 1:2)
Master Serial	0	0	0
Slave Serial	1	1	1
Master Parallel	1	1	0
Slave Parallel	0	1	1
JTAG	1	0	1

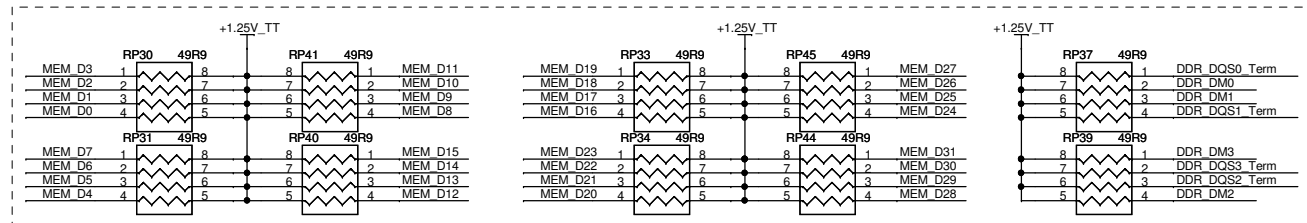
Note: With no shunts installed on JP3, M0 = M1 = M2 = 1 via RP28



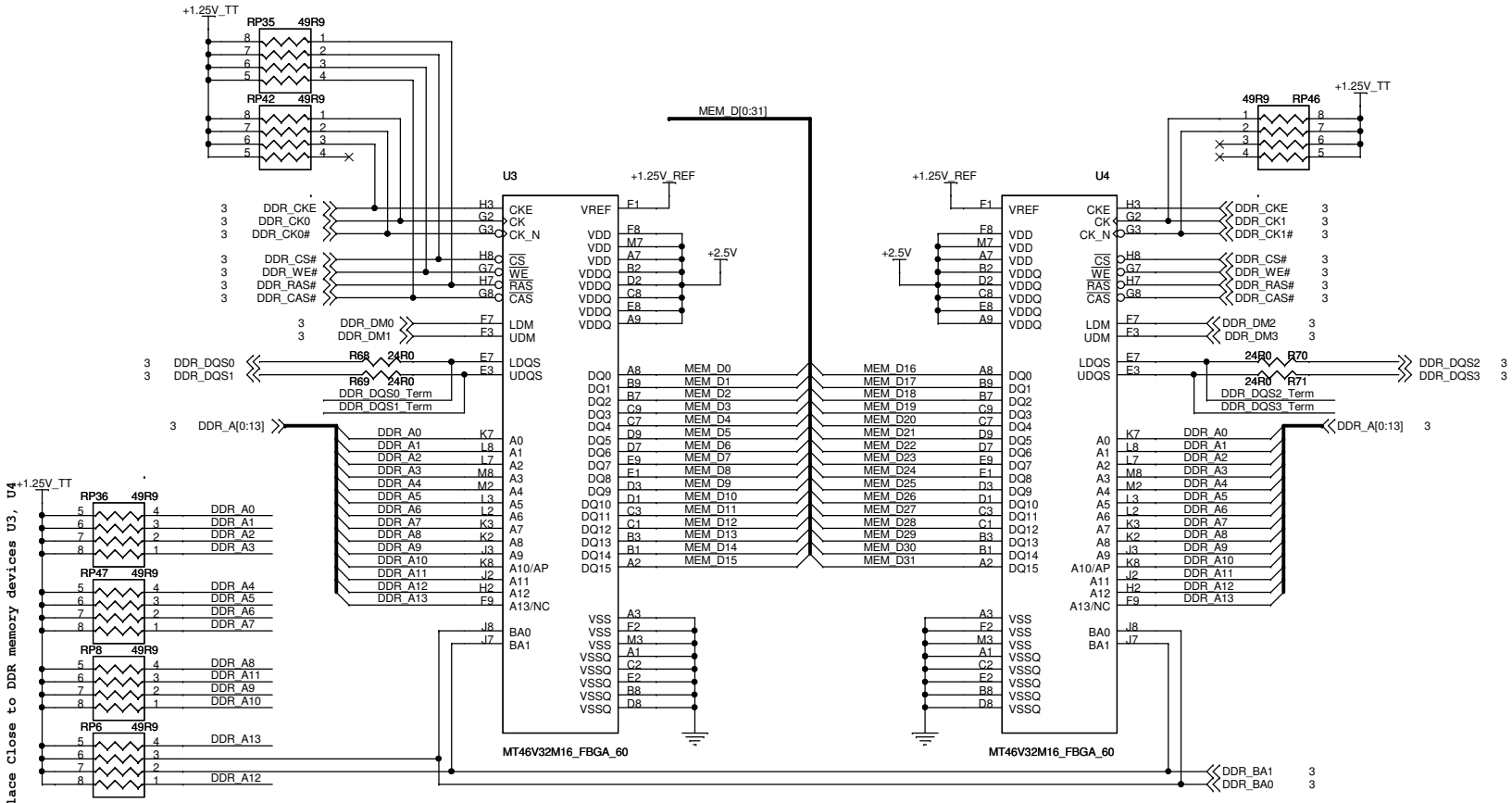
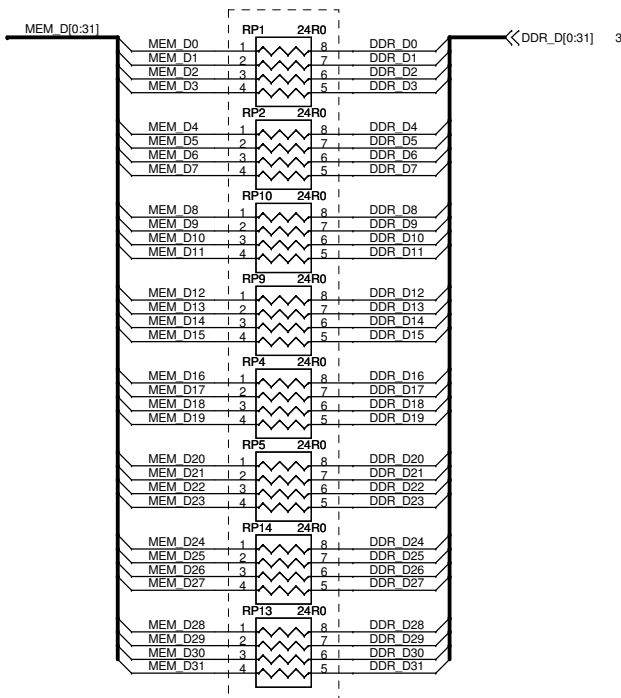
JP1/JP2 Settings:
 PROM and FPGA in chain - JP2 2:3, JP1 2:3
 PROM only in chain - JP2 2:3, JP1 1:2
 FPGA only in chain - JP2 1:2, JP1 2:3



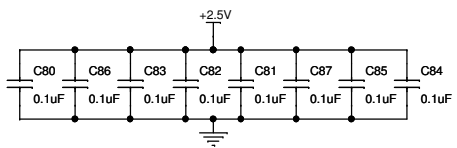
Install Terminators on Far Side of DDR memory devices U3 and U4



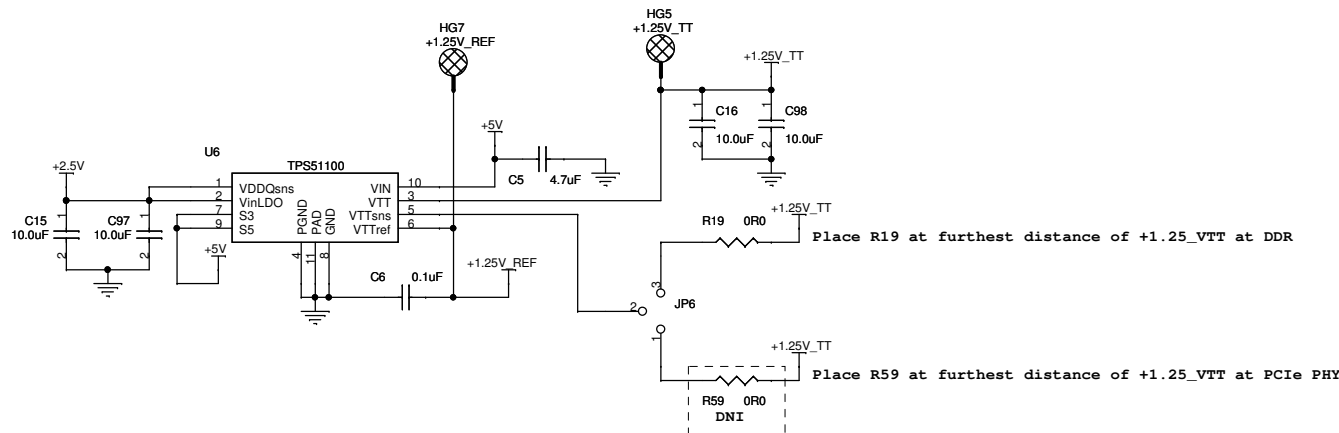
Place Close to DDR memory devices U3 and U4

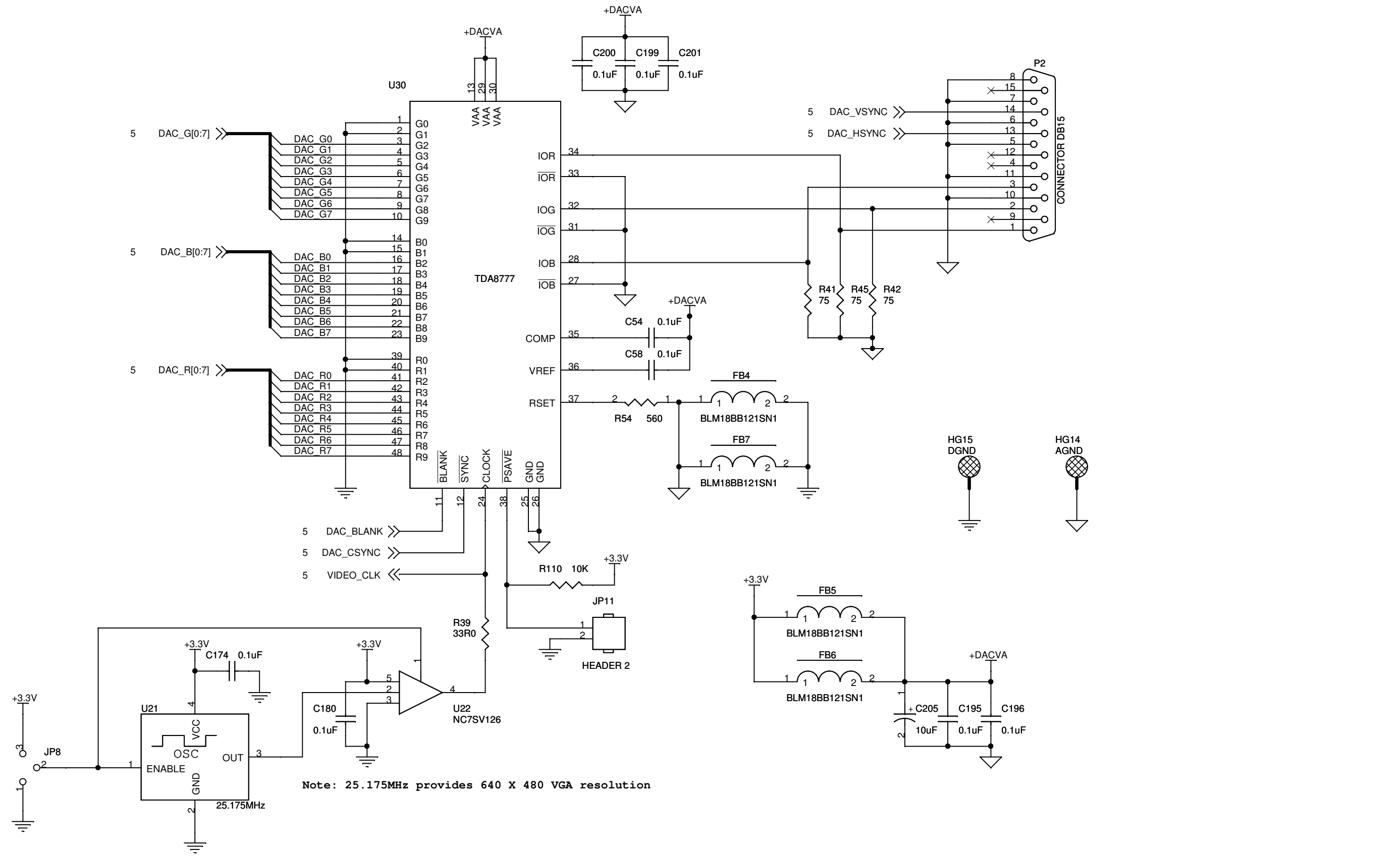


Place Close to DDR memory devices U3, U4



DDR Termination Voltage



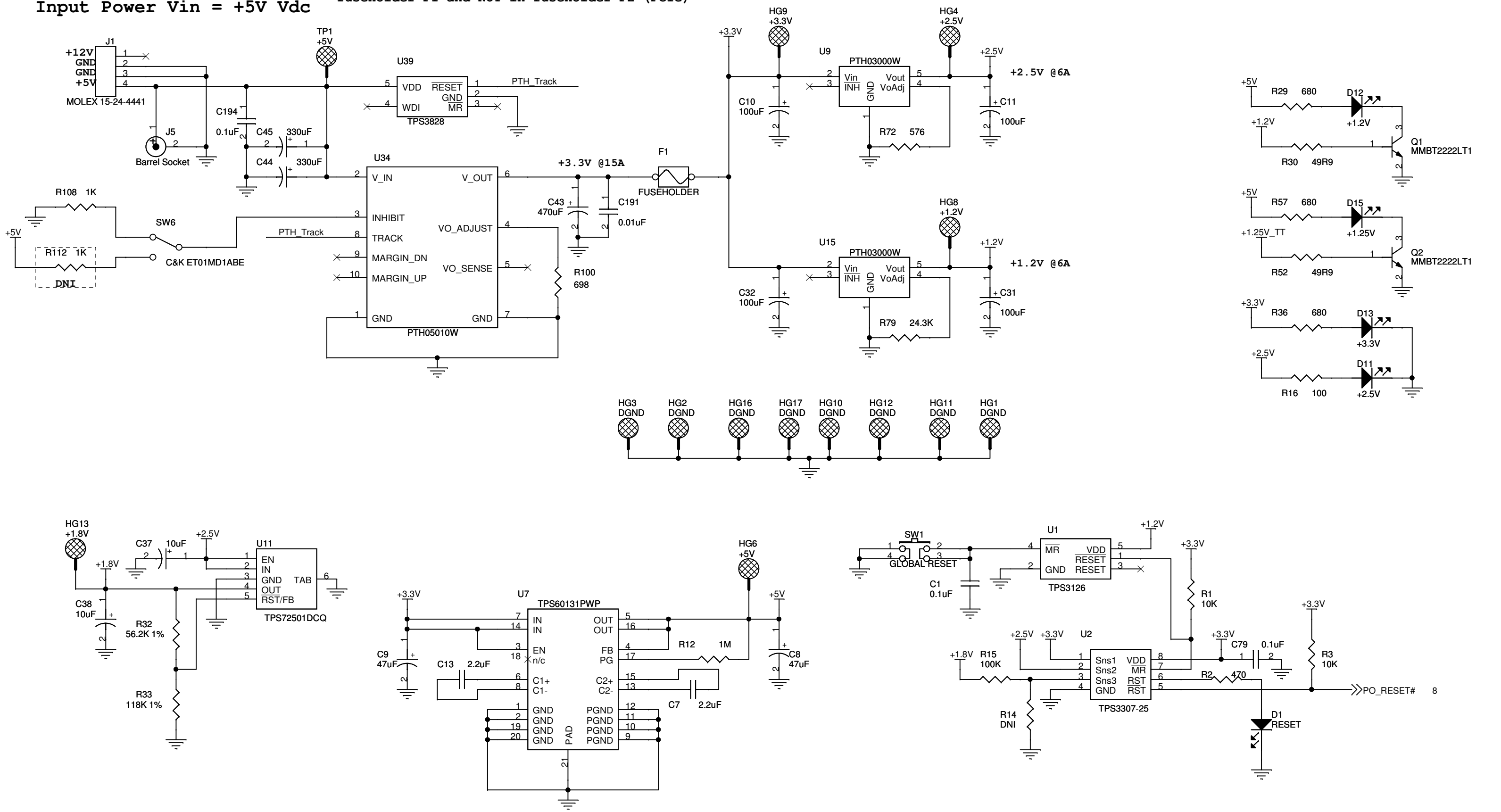


Note: 25.175MHz provides 640 X 480 VGA resolution

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To supply power from J1 or J5, fuse MUST be in fuseholder F1 and NOT in fuseholder F2 (PCIe)

Input Power Vin = +5V Vdc



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Changes Rev1 to Rev2:

3/27/06 - Swapped power and ground connections to power switch SW6 to match PCB silk-screen (up = ON)

Clarification:

5/02/07 - Changed names of pin pairs B14/B15 and A16/A17 on PCIe connector P3 to match PCIe CEM Spec.

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Title		Spartan-3 PCIe Starter Board Revision Notes
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