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Virtex-II Pro ML320, ML321, ML323 Platform

User Guide

UG033 (v2.1) P/N 0402071 March 19, 2004

XILINX®

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The following table shows the revision history for this document..

	Version	Revision
08/13/02	1.0	Initial Xilinx release.
03/03/04	2.0	Updated RocketIO trademark. Updated block diagram (Fig. 1). Updated board (Fig. 2) from ML321 REV C to ML321 REV D. Changed column headings in all tables to ML320, ML321, and ML323 format. Corrected pin names in tables.
03/19/04	2.1	Minor non-technical edits.

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Preface

About This Guide

This document describes the features and operation of the Virtex-II Pro™ ML320/ML321/ML323 prototype and demonstration boards.

Guide Contents

This manual contains the following chapter:

- "Virtex-II Pro ML320, ML321, ML323 Platform User Guide"

Additional Resources

For additional information, go to http://support.xilinx.com. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging http://support.xilinx.com/support/techsup/tutorials/index.htm
Answer Browser	Database of Xilinx solution records http://support.xilinx.com/xlnx/xil_ans_browser.jsp
Application Notes	Descriptions of device-specific design techniques and approaches http://support.xilinx.com/apps/appsweb.htm
Data Sheets	Device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging http://support.xilinx.com/xlnx/xweb/xil_publications_index.jsp
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues http://support.xilinx.com/support/troubleshoot/psolvers.htm
Tech Tips	Latest news, design tips, and patch information for the Xilinx design environment http://www.support.xilinx.com/xlnx/xil_tt_home.jsp

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *`design_name`*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *`design_name`*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required.	**`ngdbuild`** [*`option_name`*] *`design_name`*
Braces { }	A list of items from which you must choose one or more	**`lowpwr ={on|off}`**
Vertical bar |	Separates items in a list of choices	**`lowpwr ={on|off}`**

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis ...	Repetitive material that has been omitted	**`allow block`** *`block_name loc1 loc2 ... locn;`*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Handbook*.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Virtex-II Pro ML320, ML321, ML323 Platform User Guide

Package Contents

- Xilinx Virtex-II Pro™ ML320, ML321, or ML323 platform (referred to as the "ML32*x* platform")
- User guide
- Four SMA-to-SMA coax cable assemblies
- CD-ROM
- System Ace™ CompactFlash memory card
- RS232 cable
- Power supply

CD-ROM Contents

- User guide in PDF format
- Example design file for demonstration of the RocketIO™ transceivers
- System ACE files (`*.ace`) for each part type supported by the board
- Full schematics of the board in both PDF format and ViewDraw schematic format
- PC board layout in Pads PCB format
- Gerber files in `*.pho` and `*.pdf` for the PC board (There are many free or shareware Gerber file viewers available on the Web for viewing and printing these files)

Conventions

The voltage range names used on the ML32*x* platform differs from those shown in the *Virtex-II Pro Platform FPGAs: Complete Data Sheet* (DS083) at http://direct.xilinx.com/bvdocs/publications/ds083.pdf

They correspond as shown in Table 1:

Table 1: **Voltage Range Names**

Data Book	Board		Data Book	Board
VCCAUX	VAUX		VCCO	VCCO
VCCAUXRX	AVCCAUX		VTRX	VT_RX
VCCAUXTX	AVCCAUX		VTTX	VT_TX
VCCINT	VCORE			

Introduction

The ML32*x* platform allows designers to investigate and experiment with the features of RocketIO transceivers. This document describes the features and operation of the boards.

The platforms and their corresponding packages are shown in Table 2.

Table 2: **Platforms and Packages**

Platform	Package
ML320	FG456
ML321	FF672
ML323	FF1152

Features

- Virtex-II Pro FPGA
- On-board power supplies for all necessary voltages capable of supplying 2A each
- Power supply jacks for optional use of external power supplies
- JTAG configuration port for use with Parallel Cable III and Parallel Cable IV cables
- System ACE configuration controller
- RS232 serial port
- Two 125-MHz or 156.25-MHz differential clock oscillators
- Two 2.5V clock oscillator sockets
- Four differential clock pairs with SMA connectors
- Two single-ended clocks with SMA connectors
- Two pairs of 32-position headers with ground headers for parallel BERT cables
- 16 or 32 pairs of SMA connectors for the RocketIO transceivers
- Power indicator LEDs
- General purpose DIP switches, LEDs, and push buttons

Figure 1 shows a block diagram of the board.

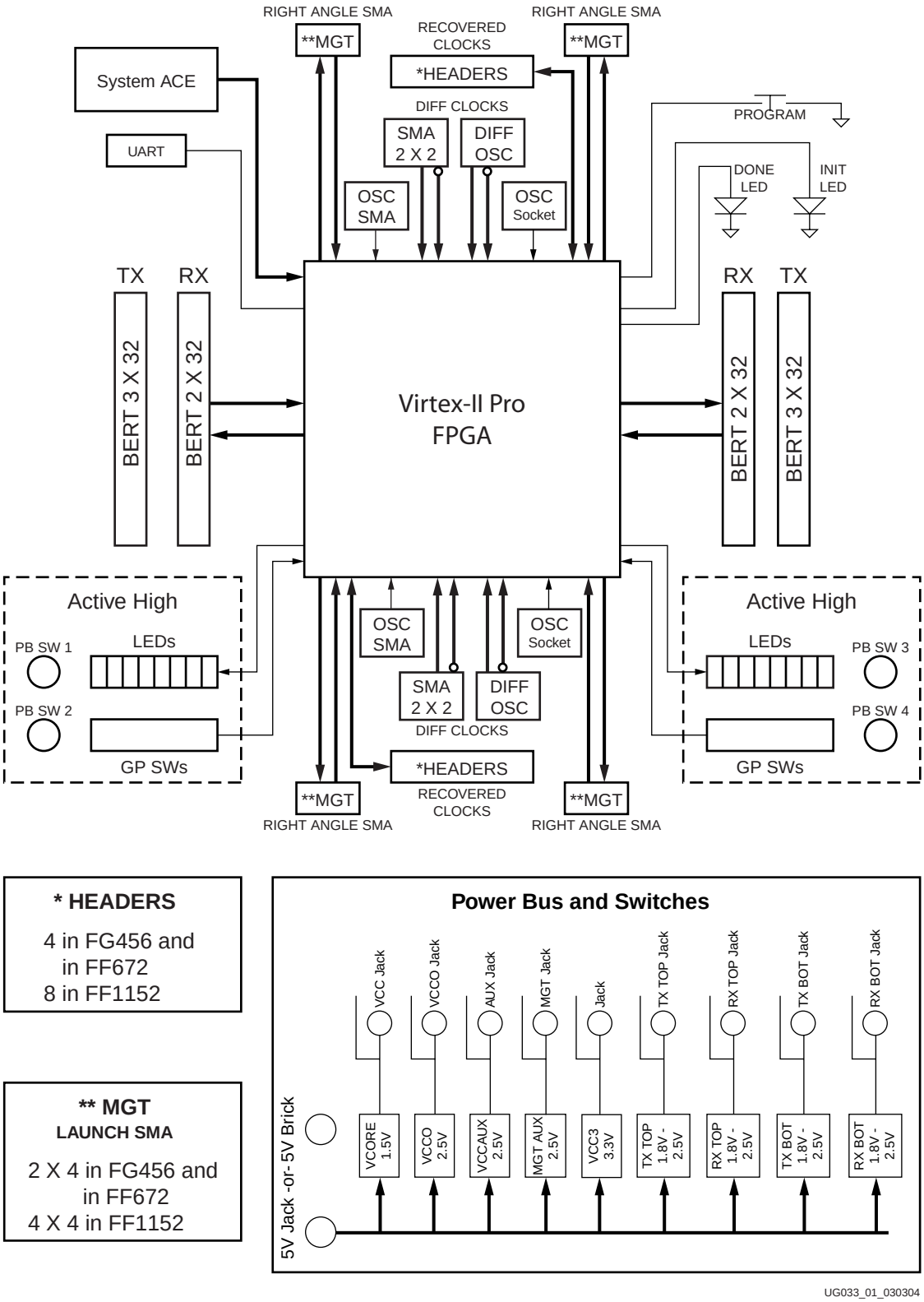

Figure 1: **Virtex-II Pro ML32*x* Platform Block Diagram**

Detailed Description

The ML32*x* platform is shown in Figure 2. Each feature is detailed in the numbered sections that follow.

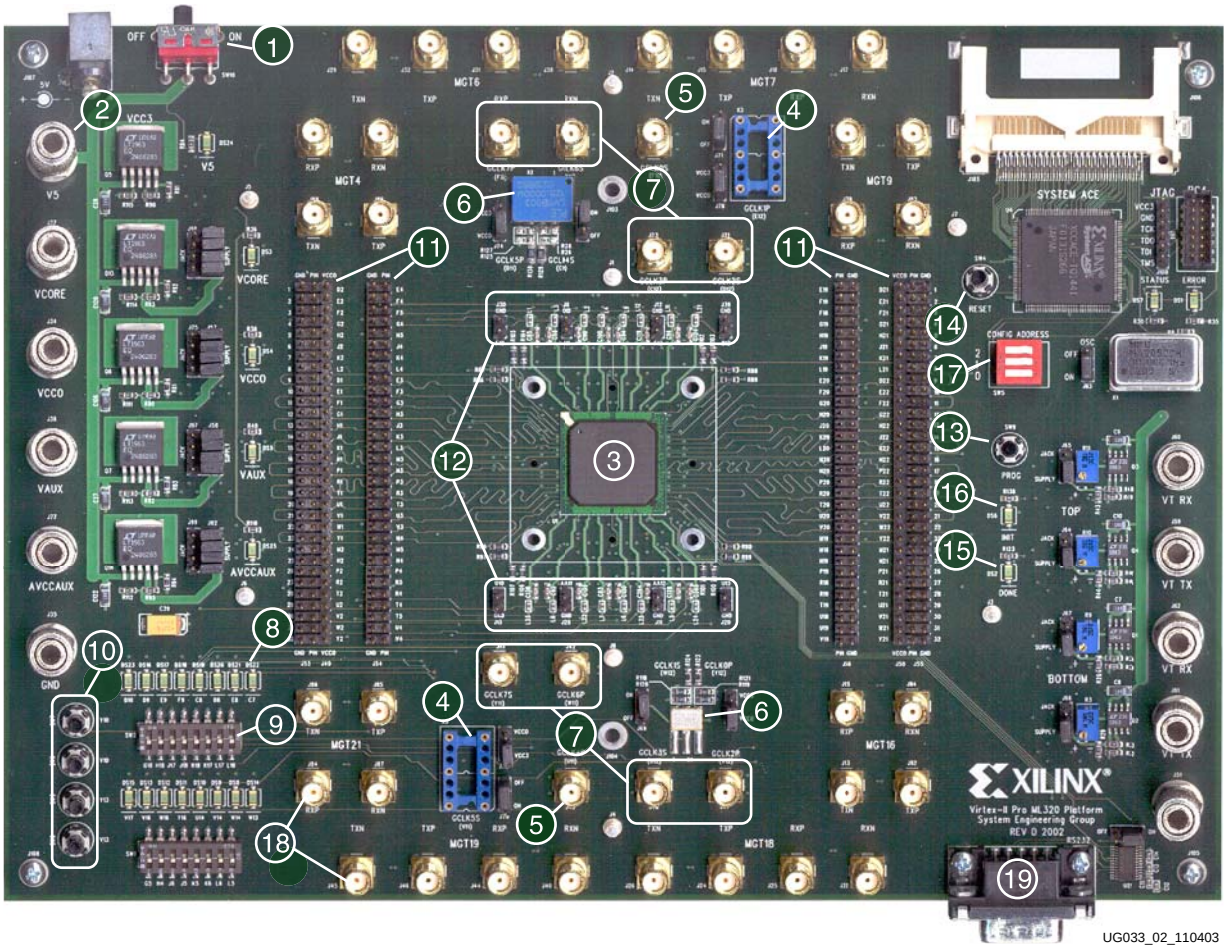

Figure 2: **Detailed Description of Virtex-II Pro ML32*x* Platform Components**

1. Power Switch

The board has an on-board power supply and an on|off power switch. When lit, a green LED indicates power from the power brick connector or the 5V jack.

On Position

In the *on* position, the power switch enables delivery of all power to the board by way of voltage regulators situated close to the left and right edges of the board. These regulators feed off a 5V external power brick or the 5V power supply jack.

The voltage regulators deliver fixed voltages. Maximum current range for each voltage regulator is 2A.

RocketIO termination voltages are situated on the right edge of the board and are marked as VT_RX, VT_TX (top set) and VT_RX, VT_TX (bottom set). These can be used to deliver a fixed voltage by appropriate selection of the resistors designated as R32, R39, R46, and

R49 (default is set to 2.5V). These can be made to deliver a variable voltage by depopulating the above mentioned resistors and manipulating the potentiometers (R3, R9, R10, R11). The voltage range is as shown in Table 3.

Table 3: **Voltage Ranges**

Label	Max Voltage
VCORE	1.5V (1.65V for -ES devices)
VCCO	2.5V
VCCAUX	2.5V
AVCCAUX	2.5V
VT_TX (top set)	1.7 - 2.5V
VT_RX (top set)	1.7 - 2.5V
VT_TX (bottom set)	1.7 - 2.5V
VT_RX (bottom set)	1.7 - 2.5V

Off Position

In the *off* position, the power switch disables all modes of powering the FPGA.

Power Enable Jumpers

For each power supply there are headers marked *Supply* on one side and *Jack* on the other side. Appropriate placements of jumpers on these headers enables delivery of all power from either the on-board regulators or power supply jacks marked V5, VCORE, VCCO, VCCAUX, AVCCAUX, VT_TX, VT_RX (top set) and VT_TX, VT_RX (bottom set).

2. Power Supply Jacks

One method of delivering power to the FPGA is by way of the power supply jacks. These jacks are:

- AVCCAUX
  - Supplies power to the RocketIO transceivers on the FPGA
- VCCAUX
  - Supplies voltage to the V_{AUX} header and the V_{AUX} FPGA pins
- VCCO
  - Supplies I/O voltages to the FPGA
- VCORE
  - Supplies voltage to the core of the FPGA
    (Consult the *Virtex-II Pro Platform FPGAs: Complete Data Sheet* (DS083) at http://direct.xilinx.com/bvdocs/publications/ds083.pdf for the maximum VCORE voltage for the device you are using)

The following two jacks supply termination voltages to the RocketIO transceivers on the top and bottom edges of the FPGA:

- VT_TX (top set and bottom set)
- VT_RX (top set and bottom set)

Note: 5V must always be applied to the 5V jack or to the external power brick connector to power the 3.3V regulator for the System ACE chip.

3. FPGA Configuration

The FPGA can only be configured in JTAG mode using one of the following options:

- Parallel Cable III cable
- Parallel Cable IV cable
- System ACE configuration controller
  (Consult the *System ACE CompactFlash Solution* (DS080) at http://www.xilinx.com/bvdocs/publications/ds080.pdf for more information)

Using the configuration address DIP switches, one of eight bitstreams stored in the CompactFlash memory card can be accessed through the on-board System ACE controller.

Note: When using the flying wire leads or the Parallel Cable IV cable, the System ACE controller will be bypassed, thus causing no disruption in the JTAG chain.

4. Oscillator Sockets

The ML32*x* platform has two crystal oscillator sockets, each wired for standard LVTTL-type oscillators. These connect to the FPGA clock pins as shown in Table 4. The oscillator sockets accept both half- and full-sized oscillators and are powered by the VCCO 2.5V power supply.

Table 4: **OSC Connections**

Label	ML320		ML321		ML323	
	Clock Name	Pin	Clock Name	Pin	Clock Name	Pin
X3	CLK_OSC_TOP	E12	CLK_OSC_TOP	D14	CLK_OSC_TOP	D18
X5	CLK_OSC_BOT	V11	CLK_OSC_BOT	AC13	CLK_OSC_BOT	AJ17

5. Single-Ended SMA Clocks

The ML32*x* platform has two SMA clock inputs that allow connection to an external function generator. These connect to the FPGA clock pins as shown in Table 5.

Table 5: **SMA Clock Pin Connections**

Label	ML320		ML321		ML323	
	Clock Name	Pin	Clock Name	Pin	Clock Name	Pin
J27	CLK_SMA_TOP	F12	CLK_SMA_TOP	E14	CLK_SMA_TOP	E18
J43	CLK_SMA_BOT	U11	CLK_SMA_BOT	AB13	CLK_SMA_BOT	AH17

6. Differential Oscillators

The ML32*x* platform has two differential oscillators, each wired to LVDS inputs on the FPGA. These connect to the FPGA clock pins shown in Table 6. The differential oscillators are powered by the VCCO 2.5V power supply.

Table 6: **Differential Oscillator Pin Connections**

Label	ML320		ML321		ML323	
	Clock Name	Pin	Clock Name	Pin	Clock Name	Pin
X2	CLK_BREF_TOP_P CLK_BREF_TOP_N	C11 D11	CLK_BREF2_TOP_P CLK_BREF2_TOP_N	C13 B13	CLK_BREF2_TOP_P CLK_BREF2_TOP_N	J17 H17
X4	CLK_BREF2_BOT_P CLK_BREF2_BOT_N	Y12 W12	CLK_BREF_BOT_P CLK_BREF_BOT_N	AD14 AE14	CLK_BREF_BOT_P CLK_BREF_BOT_N	AK18 AL18

7. Differential SMA Clocks

There are four pairs of 50Ω SMA connectors that can be used (with 100Ω termination) to connect to an external function generator. These connect to the FPGA pins as shown in Table 7. These SMA connectors can also be used as eight single-ended clock inputs.

Table 7: **Differential Clock Pin Connections**

Label	ML320		ML321		ML323	
	Clock Name	Pin	Clock Name	Pin	Clock Name	Pin
J21	CLK_BREF2_TOP_P	D12	CLK_BREF_TOP_N	C14	CLK_BREF_TOP_N	J18
J23	CLK_BREF2_TOP_N	C12	CLK_BREF_TOP_P	B14	CLK_BREF_TOP_P	H18
J42	CLK_BREF_BOT_P	W11	CLK_BREF2_BOT_N	AD13	CLK_BREF2_BOT_N	AK17
J41	CLK_BREF_BOT_N	Y11	CLK_BREF2_BOT_P	AE13	CLK_BREF2_BOT_P	AL17
J16	CLK_DIFF_TOP_P	E11	CLK_DIFF_TOP_N	D13	CLK_DIFF_TOP_N	D17
J19	CLK_DIFF_TOP_N	F11	CLK_DIFF_TOP_P	E13	CLK_DIFF_TOP_P	E17
J47	CLK_DIFF_BOT_P	V12	CLK_DIFF_BOT_P	AB14	CLK_DIFF_BOT_P	AH18
J48	CLK_DIFF_BOT_N	U12	CLK_DIFF_BOT_N	AC14	CLK_DIFF_BOT_N	AJ18

8. User LEDs (Active High)

There are 16 or 20 active-high LEDs, as shown in Table 8 and Table 9, page 19, connected to user I/O pins on the FPGA. These LEDs can be used to indicate status or any other purpose the user sees fit.

Table 8: **User LEDs - LED Row 1**

LED ROW 1	ML320	ML321	ML323
DS15	V17	AC19	AG25
DS13	V16	AD19	AH25
DS12	W16	AE19	AK27
DS11	Y16	AF19	AL27
DS10	U14	Y18	AH26
DS9	V14	AA18	AK29
DS8	W14	AC20	AK28
DS14	W13	AA20	AF25
DS26		AA19	AE24
DS27		Y19	AF24

Table 9: **User LEDs - LED Row 2**

LED ROW 2	ML320	ML321	ML323
DS29		A8	G10
DS28		B8	J12
DS23	D10	C8	K12
DS16	D9	D8	D6
DS17	E9	E9	D5
DS18	F9	E8	E9
DS19	C8	F8	F9
DS20	D8	D7	J11
DS21	E8	E7	K11
DS22	C7	C6	J10

9. User DIP Switches (Active High)

There are 16 or 20 active-high DIP switches, as shown in Table 10 and Table 11, page 20, connected to user I/O pins on the FPGA. These DIP switches can be used to generate vectors or any other purpose that the user sees fit.

Table 10: **User DIP Switches - SW1**

SW1	ML320	ML321	ML323
1	G5	R23	U4
2	H4	R22	T4
3	J6	T23	R4
4	J5	T22	P4
5	K5	U22	N4
6	K6	V22	M4
7	L6	W22	L4
8	L5	Y22	K4
9		Y21	E4
10		AB23	F7

.

Table 11: **User DIP Switches - SW2**

SW2	ML320	ML321	ML323
1	G18	P4	U30
2	H18	P5	T30
3	J17	R6	P30
4	J18	T6	U29
5	K18	U5	N30
6	K17	V5	L30
7	L17	W5	K30
8	L18	W6	J28
9		Y5	J27
10		Y6	E32

10. User Push Buttons (Active High)

There are four active-high push buttons, as shown in Table 12, connected to user I/O pins on the FPGA. These push buttons can be used for any purpose that the user sees fit.

Table 12: **User Push Buttons**

PB SW	ML320	ML321	ML323
SW7	Y10	G18	E26
SW6	V10	A19	F26
SW3	Y13	AA12	AG16
SW8	V13	AB12	AH15

11. BERT Headers

There are two pairs of 32-position headers intended to be used for parallel Bit Error Rate Testing (BERT). Each header is connected to 32 user I/O pins, as shown in Table 13, page 21, Table 14, page 22, Table 15, page 23, and Table 16, page 24. The 64-pin headers (J54, J56) allow the user to connect 32 user I/O pins to ground. The 96-pin headers (J53, J55) allow the user to connect the 32 user I/O pins to either ground or to VCCO.

.

Table 13: **BERT Header J53**

Header J53	ML320	ML321	ML323
1	D2	A2	N2
2	E2	C2	P2
3	F2	D2	R2
4	G2	E2	T2
5	H2	H2	U2
6	J2	B1	V2
7	K2	C1	E1
8	L2	D1	F4
9	D1	E1	L5
10	E1	F1	H1
11	F1	G1	K1
12	G1	H1	L1
13	H1	J1	M1
14	J1	K1	N1
15	K1	L1	P1
16	N1	M1	R1
17	P1	R1	Y1
18	R1	T1	AA1
19	T1	U1	AB1
20	U1	V1	AC1
21	V1	W1	AD1
22	W1	Y1	AE1
23	Y1	AA1	AG1
24	M2	AC1	AE4
25	N2	AD1	AH5
26	P2	AE1	AK3
27	R2	T2	AL1
28	T2	V2	W2
29	U2	W2	Y2
30	V2	AC2	AA2
31	W2	AD2	AB2
32	Y2	AF2	AC2

Table 14: **BERT Header J54**

Header J54	ML320	ML321	ML323
1	E4	E4	K5
2	F4	G4	L3
3	F5	H4	M3
4	G4	J4	N3
5	H5	E3	P3
6	J4	G3	R3
7	K4	H3	T3
8	L4	J3	U3
9	E3	K3	E2
10	F3	L3	F5
11	G3	M3	L6
12	H3	N3	H2
13	J3	J2	J2
14	K3	L2	K2
15	L3	M2	L2
16	M3	N2	M2
17	N3	P2	AE2
18	P3	R2	AF2
19	R3	P3	AG2
20	T3	R3	AE5
21	U3	T3	AH6
22	V3	U3	AK4
23	M4	V3	AL2
24	M5	W3	V3
25	N4	Y3	W3
26	P4	AB3	Y3
27	R5	AC3	AA3
28	R4	V4	AB3
29	T4	W4	AC3
30	T5	Y4	AD3
31	U4	AB4	AF3
32	V4	AD4	AF4

Table 15: **BERT Header J55**

Header J55	ML320	ML321	ML323
1	D21	A25	N33
2	E21	C25	P33
3	F21	D25	R33
4	G21	E25	T33
5	H21	H25	U33
6	J21	B26	V33
7	K21	C26	E34
8	L21	D26	F30
9	D22	E26	L31
10	E22	F26	H34
11	F22	G26	K34
12	G22	H26	L34
13	H22	J26	M34
14	J22	K26	N34
15	K22	L26	P34
16	N22	M26	R34
17	P22	R26	Y34
18	R22	T26	AA34
19	T22	U26	AB34
20	U22	V26	AC34
21	V22	W26	AD34
22	W22	Y26	AE34
23	Y22	AA26	AG34
24	M21	AC26	AD32
25	N21	AD26	AE30
26	P21	AE26	AK32
27	R21	T25	AL34
28	T21	V25	W33
29	U21	W25	Y33
30	V21	AC25	AA33
31	W21	AD25	AB33
32	Y21	AF25	AC33

Table 16: **BERT Header J56**

Header J56	ML320	ML321	ML323
1	E19	E23	K31
2	F19	G23	L32
3	F18	H23	M32
4	G19	J23	N32
5	H19	E24	P32
6	J19	G24	R32
7	K19	H24	T32
8	L19	J24	U32
9	E20	K24	E33
10	F20	L24	E31
11	G20	M24	F31
12	H20	N24	H33
13	J20	J25	J33
14	K20	L25	K33
15	L20	M25	L33
16	M20	N25	M33
17	N20	P25	AD33
18	P20	R25	AE33
19	R20	P24	AF33
20	T20	R24	AD31
21	U20	T24	AH30
22	V20	U24	AK31
23	M19	V24	AL33
24	M18	W24	V32
25	N19	Y24	W32
26	P19	AB24	Y32
27	R18	AC24	AA32
28	R19	AD23	AB32
29	T19	U23	AC32
30	U18	V23	AF32
31	U19	W23	AD30
32	V19	Y23	AE31

12. Recovered Clock Monitor Headers

There are 8 or 16 2-pin headers connected to user I/O pins near the top and bottom of the FPGA. These headers are intended to be used to monitor the recovered clock for each RocketIO transceiver as shown in Table 17. Note, if these headers are not being used to monitor the clocks, they may be used for any other purpose the user sees fit.

Table 17: **Recovered Clock Monitor Pins**

Name	ML320		ML321		ML323	
	Label	Pin	Label	Pin	Label	Pin
RCV_CLK_OUT_2					J134	H22
RCV_CLK_OUT_4	J30	F10	J39	D17	J96	G22
RCV_CLK_OUT_5					J39	F19
RCV_CLK_OUT_6	J10	B11	J12	C15	J12	L18
RCV_CLK_OUT_7	J12	F13	J30	D12	J30	L17
RCV_CLK_OUT_8					J10	F16
RCV_CLK_OUT_9	J39	B12	J10	E10	J136	H13
RCV_CLK_OUT_11					J135	G13
RCV_CLK_OUT_14					J13	AE13
RCV_CLK_OUT_16	J20	U13	J13	AB10	J28	AF13
RCV_CLK_OUT_17					J140	AJ16
RCV_CLK_OUT_18	J11	AA12	J28	W13	J139	AK16
RCV_CLK_OUT_19	J28	AA11	J11	AD15	J137	AK19
RCV_CLK_OUT_20					J138	AE18
RCV_CLK_OUT_21	J13	U10	J20	AC17	J20	AG22
RCV_CLK_OUT_23					J11	AF22

13. Program Switch (Active Low)

The active-low program switch, when pressed, grounds the program pin on the FPGA.

14. Reset Switch (Active Low)

The active-low reset switch resets the System ACE controller.

15. DONE LED

The DONE LED indicates the status of the **DONE** pin on the FPGA. This LED lights when **DONE** is high or if power is applied to the board without a part in the socket.

16. INIT LED

The INIT LED lights during initialization.

17. Config Address DIP Switch

This switch is used to select one of eight addresses in the CompactFlash memory card, from which a configuration bitstream can be read. The open ("O") position indicates a logic '0' and the closed ("C") position indicates a logic '1' as shown in Table 18.

Table 18: **Bitstream Address Table**

2	1	0	Addr
O	O	O	0
O	O	C	1
O	C	O	2
O	C	C	3
C	O	O	4
C	O	C	5
C	C	O	6
C	C	C	7

18. RocketIO Transceiver Pins

The RocketIO transceiver pins are as shown in Table 19.

Table 19: **RocketIO TX and RX Pin Pairs**

	ML320		ML321		ML323	
RocketIO	TX Pair (P,N)	RX Pair (P,N)	TX Pair (P,N)	RX Pair (P,N)	TX Pair (P,N)	RX Pair (P,N)
2					A32, A33	A31, A30
4	A4, A3	A5, A6	A22, A23	A21, A20	A28, A29	A27, A26
5					A24, A25	A23, A22
6	A8, A7	A9, A10	A17, A18	A16, A15	A20, A21	A19, A18
7	A14, A13	A15, A16	A11, A12	A10, A9	A16, A17	A15, A14
8					A12, A13	A11, A10
9	A18, A17	A19, A20	A6, A7	A5, A4	A8, A9	A7, A6
11					A4, A5	A3, A2
14					AP4, AP5	AP3, AP2
16	AB18, AB17	AB19, AB20	AF6, AF7	AF5, AF4	AP8, AP9	AP7, AP6
17					AP12, AP13	AP11, AP10
18	AB14, AB13	AB15, AB16	AF11, AF12	AF10, AF9	AP16, AP17	AP15, AP14
19	AB8, AB7	AB9, AB10	AF17, AF18	AF16, AF15	AP20, AP21	AP19, AP18
20					AP24, AP25	AP23, AP22
21	AB4, AB3	AB5, AB6	AF22, AF23	AF21, AF20	AP28, AP29	AP27, AP26
23					AP32, AP33	AP31, AP30

Note: Shaded areas denote pins that are not used

19. RS232 Port Pins

The RS232 port pins are as shown in Table 20. The pins are set up in DTE mode as shown in Figure 3.

Table 20: **RS232 Port Pins**

FPGA UART Port Name	Direction	Net	ML320	ML321	ML323
TXD	Out	T1IN	M17	AC15	AL22
RTS	Out	T2IN	N17	AB15	AH21
RXD	In	R1OUT	N18	AA15	AG21
CTS	In	R2OUT	P18	W15	AF20

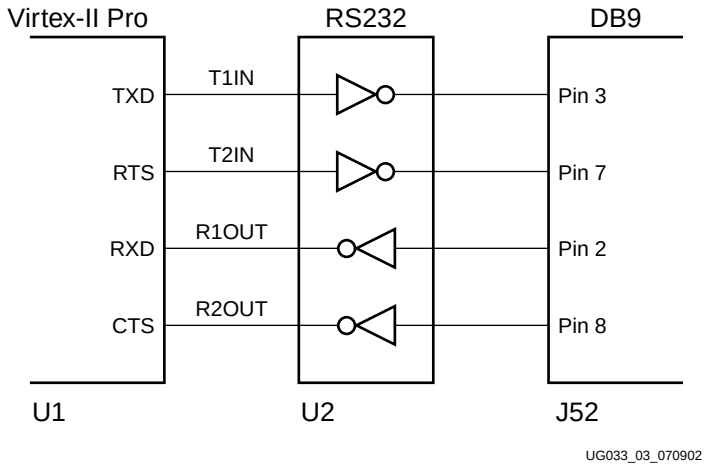

Figure 3: **RS232 Pins in DTE Mode**