Virtex-II Pro X MK322 and MK325 Platform

User Guide

UG062 (v1.0) P/N 0402274 July 1, 2005

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Revision History

Virtex-II Pro X MK322 and MK325 Platform
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The following table shows the revision history for this document.

	Version	Revision
03/26/04	0.10	Preliminary Xilinx release.
07/01/05	1.0	Initial Xilinx release.

Table of Contents

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Preface

About This Guide

This document describes the features and operation of the Virtex™-II Pro X MK322 and MK325 prototype and demonstration boards.

Guide Contents

This manual contains the following chapter:

- "Virtex-II Pro X MK322 and MK325 Platform User Guide"

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/literature/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**

Convention	Meaning or Use	Example
Italic font	Variables in a syntax statement for which you must supply values	**ngdbuild** *design_name*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **bus[7:0]**, they are required.	**ngdbuild** [*option_name*] *design_name*
Braces { }	A list of items from which you must choose one or more	**lowpwr =**{**on**|**off**}
Vertical bar |	Separates items in a list of choices	**lowpwr =**{**on**|**off**}
Vertical ellipsis . . .	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' . . .
Horizontal ellipsis ...	Repetitive material that has been omitted	**allow block** *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Handbook*.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Virtex-II Pro X MK322 and MK325 Platform User Guide

Package Contents

- Xilinx Virtex™-II Pro X MK322 and MK325 platform (referred to as the MK32x platform)
- User guide
- Four SMA-to-SMA coax cable assemblies
- CD-ROM
- System ACE™ CompactFlash memory card
- RS-232 cable
- Power supply
- NQSL (Nelco Quad Serial Loop) board

CD-ROM Contents

- User guide in PDF format
- Example design file for demonstration of the RocketIO™ transceivers
- System ACE files (`*.ace`) for each part type supported by the board
- Full schematics of the board in both PDF format and ViewDraw schematic format
- PC board layout in Pads PCB format
- Gerber files in `*.pho` and `*.pdf` for the PC board (There are many free or shareware Gerber file viewers available on the Internet for viewing and printing these files)

Conventions

The voltage range names used on the MK32x platform differ from those shown in the *Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Complete Data Sheet* (DS083) at http://www.xilinx.com/bvdocs/publications/ds083.pdf

They correspond as shown in Table 1:

Table 1: **Voltage Range Names**

Data Book	Board		Data Book	Board
VCCAUX	VCCAUX		VCCO	VCCO
VCCAUXRX	AVCCAUXRX		VTRX	VT RX
VCCAUXTX	AVCCAUXTX		VTTX	VT TX
VCCINT	VCCINT			

Introduction

The MK32x platform allows designers to investigate and experiment with the features of RocketIO transceivers. This document describes the features and operation of the boards.

The platforms and their corresponding packages are shown in Table 2.

Table 2: **Platforms and Packages**

Platform	Package
MK322	FF896
MK325	FF1704

Features

- Virtex-II Pro FPGA (referred to as the DUT [device under test] in this user guide)
- On-board power supplies for all necessary voltages capable of supplying 3A each
- Power supply jacks for optional use of external power supplies
- JTAG configuration port for use with Parallel Cable III and Parallel Cable IV cables
- System ACE configuration controller
- RS-232 serial port
- One 250 MHz and one 312 MHz differential clock oscillator
- Two 2.5V/3.3V clock oscillator sockets
- Two differential clock pairs with SMA connectors
- Two single-ended clocks with SMA connectors
- Two pairs of 36-position differentially routed headers with ground headers for parallel BERT cables
- 16 or 40 pairs of SMA connectors for the RocketIO transceivers (the number of pairs depends on the board)
- Power indicator LEDs
- General purpose DIP switches, LEDs, and push buttons

Figure 1 shows a block diagram of the board.

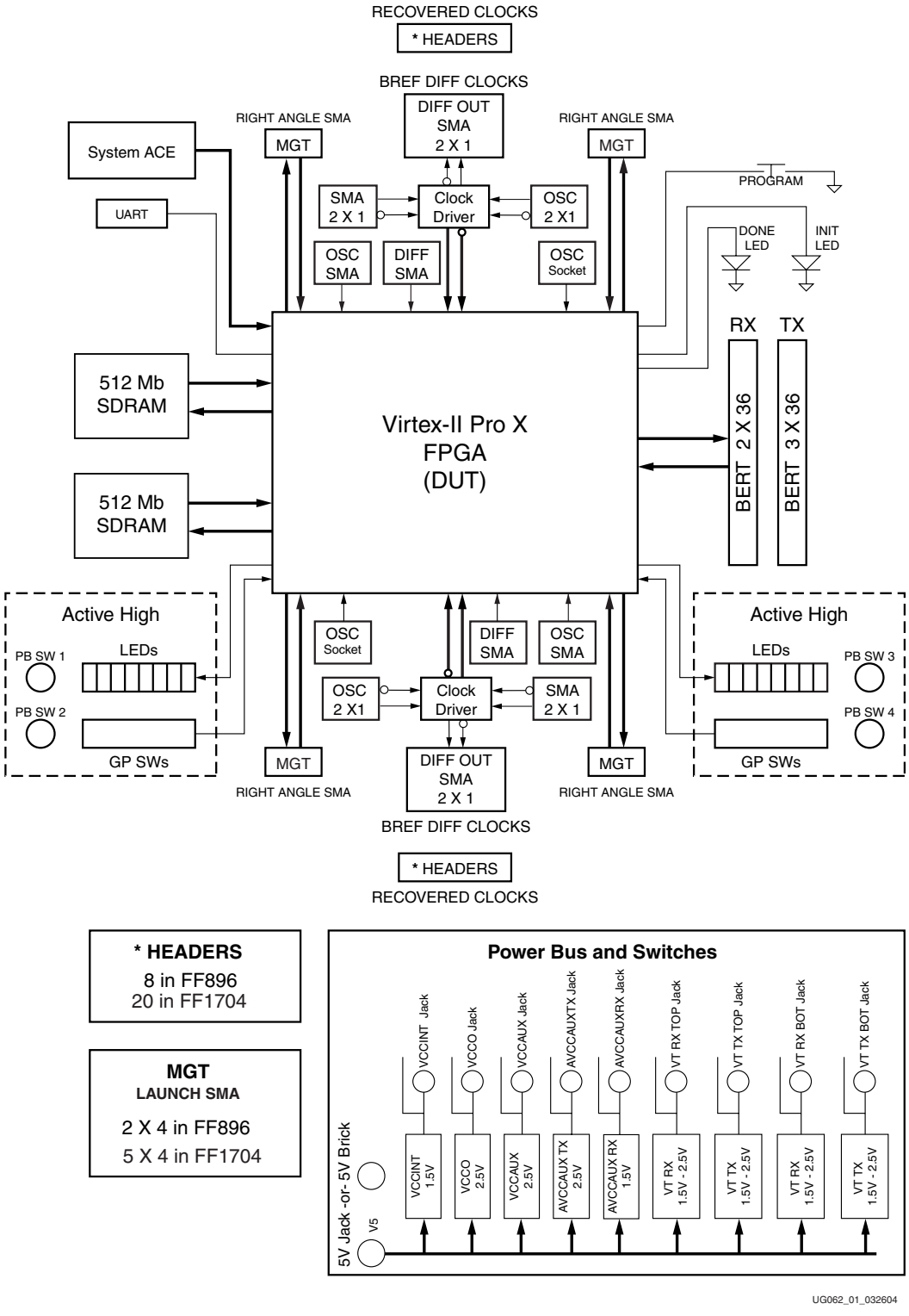

Figure 1: **Virtex-II Pro X MK32x Platform Block Diagram**

Detailed Description

The MK322 platform shown in Figure 2 represents the MK32x platforms described in this user guide. Each feature is detailed in the numbered sections that follow.

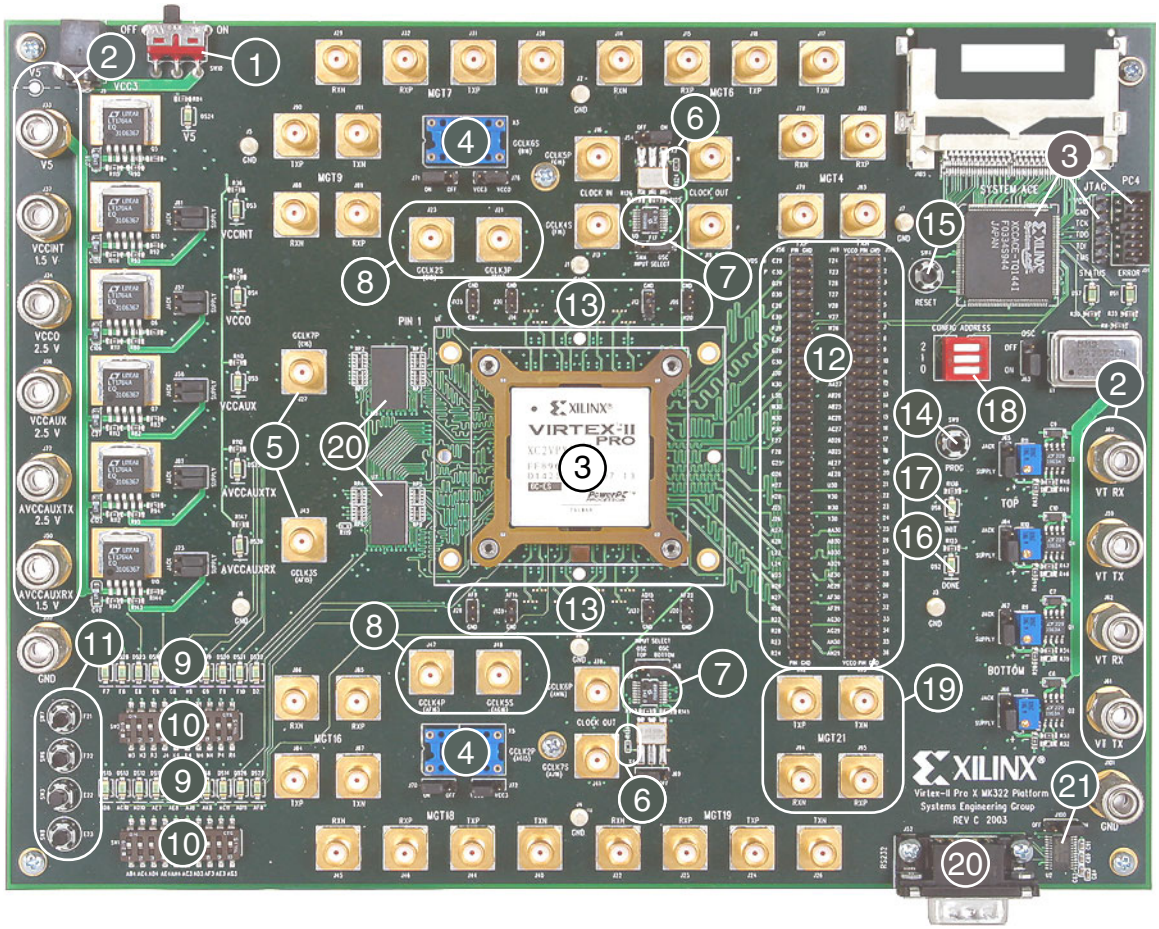

Figure 2: **Detailed Description of Virtex-II Pro X MK32x Platform Components**

1. Power Switch

The board has an on-board power supply and an on|off power switch. When lit, a green LED indicates power from the power brick connector or the 5V jack.

On Position

In the *on* position, the power switch enables delivery of all power to the board by way of voltage regulators situated close to the left and right edges of the board. These regulators feed off a 5V external power brick or the 5V power supply jack.

The voltage regulators deliver fixed voltages. Maximum current range for each voltage regulator is 3A.

RocketIO termination voltages are situated on the right edge of the board and are marked as VT RX, VT TX (top set) and VT RX, VT TX (bottom set). These can be used to deliver a fixed voltage by appropriate selection of the resistors designated as R32, R39, R46, and R49 (default is set to 1.5V). These can be made to deliver a variable voltage by depopulating the

above mentioned resistors and manipulating the potentiometers (R3, R9, R10, R11). The voltage range is as shown in Table 3.

Table 3: **Voltage Ranges**

Label	Max Voltage
VCCINT	1.5V
VCCO	2.5V
VCCAUX	2.5V
AVCCAUXTX	2.5V
AVCCAUXRX	1.5V
VT TX (top set)	1.5V - 2.5V
VT RX (top set)	1.5V - 2.5V
VT TX (bottom set)	1.5V - 2.5V
VT RX (bottom set)	1.5V - 2.5V

Off Position

In the *off* position, the power switch disables all modes of powering the FPGA.

Power Enable Jumpers

For each power supply there are headers marked *Supply* on one side and *Jack* on the other side. Appropriate placements of jumpers on these headers enables delivery of all power from either the on-board regulators or power supply jacks marked V5, VCCINT VCCO, VCCAUX, AVCCAUXTX, AVCCAUXRX, VT RX, VT TX (top set) and VT RX, VT TX (bottom set).

2. Power Supply Jacks

One method of delivering power to the FPGA is by way of the power supply jacks. These jacks are:

- V5
  - Supplies the input voltage to the board
- VCCINT
  - Supplies voltage to the core of the FPGA
    Consult the *Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Complete Data Sheet* (DS083) at http://www.xilinx.com/bvdocs/publications/ds083.pdf for the maximum VCCINT voltage for the device you are using.
- VCCO
  - Supplies I/O voltages to the FPGA
- VCCAUX
  - Supplies power to the RocketIO transceivers on the FPGA
- AVCCAUXRX
  - Supplies voltage to the V_{AUX} header and the V_{AUX} FPGA pins
- AVCCAUXTX
  - Supplies power to the RocketIO transceivers on the FPGA

The following four jacks supply termination voltages to the RocketIO transceivers on the top and bottom edges of the FPGA:

- VT TX (top set and bottom set)
- VT RX (top set and bottom set)

Note: 5V must always be applied to the V5 jack or to the external power brick connector to power the 3.3V regulator for the System ACE chip.

3. FPGA Configuration

The FPGA can only be configured in JTAG mode using one of the following options:

- Parallel Cable III cable
- Parallel Cable IV cable
- System ACE configuration controller
  Consult the *System ACE CompactFlash Solution* (DS080) at http://www.xilinx.com/bvdocs/publications/ds080.pdf for more information

Using the configuration address DIP switches, one of eight bitstreams stored in the CompactFlash memory card can be accessed through the on-board System ACE controller.

Note: When using the flying wire leads or the Parallel Cable IV cable, the System ACE controller will be bypassed, thus causing no disruption in the JTAG chain.

4. Oscillator Sockets

The MK32x platform has two crystal oscillator sockets, each wired for standard LVTTL-type oscillators. These connect to the FPGA clock pins as shown in Table 4. The oscillator sockets accept both half- and full-sized oscillators and are powered by 3.3V or the VCCO 2.5V power supply.

Table 4: **OSC Connections**

Label	MK322		MK325	
	Clock Name	Pin	Clock Name	Pin
X3	CLK_OSC_TOP	B16	CLK_OSC_TOP	J22
X5	CLK_OSC_BOT	AG15	CLK_OSC_BOT	AP21

5. Single-Ended SMA Clocks

The MK32x platform has two single-ended clock input SMA's that allow connection to an external function generator. These connect to the FPGA clock pins as shown in Table 5.

Table 5: **SMA Clock Pin Connections**

Label	MK322		MK325	
	Clock Name	Pin	Clock Name	Pin
J27	CLK_SMA_TOP	C16	CLK_SMA_TOP	K22
J43	CLK_SMA_BOT	AF15	CLK_SMA_BOT	AN21

6. Differential Oscillators

The MK32x platform has two LV-PECL differential oscillators (X2, X4), each wired to BREF clock inputs (Table 6) of the device under test (DUT) through a clock driver (see "7. Clock Multiplexer," page 14). The differential oscillators are powered by the VCC3 power supply. The differential oscillators X2, X4 have output enable circuits that are controlled by (J54, J69) respectively.

Table 6: **Differential Oscillator Pin Connections**

Label	MK322		MK325	
	Clock Name	Pin	Clock Name	Pin
X2	CLK_BREF_TOP_N	G16	CLK_BREF_TOP_P	G21 F21
	CLK_BREF_TOP_P	F16	CLK_BREF_TOP_N	AU22 AT22
X4	CLK_BREF_BOT_P	AH16	CLK_BREF_BOT_P	G21 F21
	CLK_BREF_BOT_N	AJ16	CLK_BREF_BOT_N	AU22 AT22

7. Clock Multiplexer

This section describes how the source clocks for the RocketIO transceivers are connected on the board. The differential oscillators (X2, X4) are connected to the DUT through Micrel Sy89830U differential PECL clock drivers (U5, U6) respectively. The clock multiplexer features a 2:1 differential input multiplexer and a 1:4 fanout buffer.

U5 is connected to the top DUT BREF clocks and can supply clocks either from X2 or the differential clock input SMA's (J13, J16). This selection is made one of two ways. Jumpering (J53) appropriately or by removing the jumper and driving the input select pin from the DUT (see Table 7).

The output of (U5) is fanned out to three places simultaneously: The clock output SMA's (J11, J19); the top DUT BREF clock input pins (Table 7); and one of the bottom clock multiplexer inputs (U6). This gives the user the ability to drive the BREF clocks for both the top and bottom RocketIO transceivers from one clock source or independent clock sources.

U6 is connected to the bottom DUT BREF clock input pins for the bottom RocketIO transceivers and can supply clocks either from X2 or from X4. This selection is made one of two ways: Jumpering (J68) appropriately or by removing the jumper and driving the input select pin from the DUT (Table 7).

The output of (U6) is fanned out to two places simultaneously: The clock output SMA's (J39, J41) and the bottom DUT BREF clock input. (Table 7).

Table 7: **Multiplexer Pin Connections**

Label	J53/J68 INPUT SELECT		DUT INPUT SELECT		SMA		Clock Name
	Pin 1-2	Pin 2-3	MK322	MK325	Input	Output	
U5	INPUT 1 (SMA)	INPUT 0 (X2)	F17	N/A	J13	J11	BREF_OUT_TOP_P
					J16	J19	BREF_OUT_TOP_N
U6	INPUT 1 (X2)	INPUT 0 (X4)	AB17	N/A		J39	BREF_OUT_BOT_P
						J41	BREF_OUT_BOT_N

8. Differential SMA Clocks

There are two pair of 100 Ω differentially routed SMA connectors that allow the user to connect to an external function generator. These connect to the FPGA pins shown in Table 8. These SMA connectors can also be used as four single-ended clock inputs.

Table 8: **Differential Clock Pin Connections**

Label	MK322		MK325	
	Clock Name	Pin	Clock Name	Pin
J21	CLK_DIFF_TOP_P	F15	CLK_DIFF_TOP_P	F22
J23	CLK_DIFF_TOP_N	G15	CLK_DIFF_TOP_N	G22
J47	CLK_DIFF_BOT_P	AF16	CLK_DIFF_BOT_P	AN22
J48	CLK_DIFF_BOT_N	AG16	CLK_DIFF_BOT_N	AP22

9. User LEDs (Active-High)

There are 20 active-High LEDs, as shown in Table 10 and Table 9, connected to user I/O pins on the FPGA. These LEDs can be used to indicate status or any other purpose the user sees fit.

Table 9: **User LEDs - LED Row 1**

LED ROW 1 (BOTTOM)	MK322	MK325
DS15	AD8	AT10
DS13	AC10	AV10
DS12	AD10	AW10
DS11	AE7	AR11
DS10	AE8	AP11
DS9	AJ8	AV11
DS8	AK8	AU11
DS14	AC11	AY10
DS26	AD11	AY11
DS27	AF8	AN12

Table 10: **User LEDs - LED Row 2**

LED ROW 2 (TOP)	MK322	MK325
DS29	F7	AB7
DS28	F8	AB9
DS23	E8	AB10
DS16	E9	AC3
DS17	G8	AC4
DS18	H9	AC11
DS19	G9	A12
DS20	F9	AC6
DS21	F10	AC7
DS22	D7	AC9

10. User DIP Switches (Active-High)

There are 20 active-High DIP switches, as shown in Table 11 and Table 12, connected to user I/O pins on the FPGA. These DIP switches can be used to generate vectors or any other purpose that the user sees fit.

Table 11: **User DIP Switches - SW1**

SW1	MK322	MK325
1	AB4	AM2
2	AC4	AP2
3	AD4	AR2
4	AE4	AT2
5	AH4	AU2
6	AC3	AV2
7	AD3	AW2
8	AF3	AD1
9	AE3	AE1
10	AG3	AF1

Table 12: **User DIP Switches - SW2**

SW2	MK322	MK325
1	M3	AH1
2	N3	AJ1
3	R3	AK1
4	J4	AM1
5	K4	AN1
6	L4	AP1
7	M4	AT1
8	N4	AU1
9	P4	AV1
10	R4	AW1

11. User Push Buttons (Active-High)

There are four active-High push buttons, as shown in Table 13, connected to user I/O pins on the FPGA. These push buttons can be used for any purpose that the user sees fit.

Table 13: **User Push Buttons**

PB SW	MK322	MK325
SW7	F21	G33
SW6	F22	F33
SW3	E22	D34
SW8	E23	C34

12. BERT Headers

To the left of the DUT, there are two headers: One 36X2 header (J56) (see Table 14) and one 36X3 header (J49, J55) (see Table 15, page 19). These two headers are intended to be used for BERT testing.

The column of pins on the left side of (J56) is connected to 36 user I/O pins of the DUT and are routed differentially. The column of pins on the right side of (J56) are connected to ground.

The column of pins on the left side of (J49, 55) is connected to VCCO 2.5V. The column of pins on the right side of (J49, 55) is connected to ground. This gives users the ability to connect unused input pins to either high or low. The center column of pins is connected to 36 user I/O pins of the DUT and are routed differentially.

Table 14: **BERT Header J56**

BERT	MK322		MK325	
Header J56	Pin	Polarity	Pin	Polarity
1	C29	N	D42	N
2	C30	P	D41	P
3	D29	N	E42	N
4	D30	P	E41	P
5	E29	N	F42	N
6	E30	P	F41	P
7	F29	N	G41	N
8	F30	P	G42	P
9	G29	N	J42	N
10	G30	P	J41	P
11	J30	N	K41	N
12	K30	P	K42	P
13	L30	N	L42	N

Table 14: **BERT Header J56 *(Continued)***

BERT	MK322		MK325	
Header J56	Pin	Polarity	Pin	Polarity
14	M30	P	L41	P
15	N30	N	N42	N
16	P30	P	N41	P
17	F27	N	R42	N
18	F28	P	R41	P
19	G25	N	G38	N
20	G26	P	H37	P
21	H27	N	J38	N
22	H28	P	J39	P
23	J25	N	L38	N
24	J26	P	L39	P
25	K27	N	M36	N
26	K28	P	M35	P
27	L23	N	N40	N
28	L24	P	N39	P
29	M25	N	R38	N
30	M26	P	R37	P
31	N27	N	U40	N
32	N28	P	U39	P
33	R27	N	W38	N
34	R28	P	W37	P
35	R23	N	AA37	N
36	R24	P	AA36	P

Table 15: **BERT Header J55**

BERT	MK322		MK325	
Header J55	Pin	Polarity	Pin	Polarity
1	T24	N	AB37	N
2	T23	P	AB36	P
3	T28	N	AD38	N
4	T27	P	AD37	P
5	V28	N	AF40	N
6	V27	P	AF39	P
7	W26	N	AG37	N
8	W25	P	AG38	P
9	Y24	N	AK40	N
10	Y23	P	AK39	P
11	AA28	N	AK36	N
12	AA27	P	AK35	P
13	AB26	N	AM39	N
14	AB25	P	AM38	P
15	AC28	N	AP39	N
16	AC27	P	AP38	P
17	AD26	N	AT38	N
18	AD25	P	AR37	P
19	AE28	N	AH42	N
20	AE27	P	AH41	P
21	U30	N	AK42	N
22	V30	P	AK41	P
23	W30	N	AM42	N
24	Y30	P	AM41	P
25	AA30	N	AN42	N
26	AB30	P	AN41	P
27	AD30	N	AP42	N
28	AD29	P	AP41	P
29	AE30	N	AT42	N
30	AE29	P	AT41	P

Table 15: **BERT Header J55 *(Continued)***

BERT	MK322		MK325	
Header J55	**Pin**	**Polarity**	**Pin**	**Polarity**
31	AF30	N	AU42	N
32	AF29	P	AU41	P
33	AG30	N	AV42	N
34	AG29	P	AV41	P
35	AH30	N	AW42	N
36	AH29	P	AW41	P

13. Recovered Clock Monitor Headers

There are 8 or 20 2-pin headers connected to user I/O pins near the top and bottom of the FPGA. These headers are intended to be used to monitor the recovered clock for each RocketIO transceiver as shown in Table 16. Note, if these headers are not being used to monitor the clocks, they can be used for any other purpose the user sees fit.

Table 16: **Recovered Clock Monitor Headers**

Label	MK322	MK325
	Pin	Pin
J136		C11
J135	C8	C15
J53		D13
J10		F19
J30	E14	M21
J12	C18	H23
J39		D24
J96	H20	L27
J50		F30
J134		G31
J13		AT12
J54		AT13
J28	AF9	AY15
J140		AW19
J139	AF14	AV20
J137	AE17	AR23
J138		AY24
J20	AF22	AY28
J141		AU30
J11		AN31

14. PROG Switch (Active-Low)

The active-Low program (PROG) switch, when pressed, grounds the program pin on the FPGA.

15. RESET Switch (Active-Low)

The active-Low RESET switch resets the System ACE controller.

16. DONE LED

The DONE LED indicates the status of the **DONE** pin on the FPGA. This LED lights when **DONE** is high or if power is applied to the board without a part in the socket.

17. INIT LED

The INIT LED lights during initialization.

18. CONFIG ADDRESS DIP Switch

This switch is used to select one of eight addresses in the CompactFlash memory card, from which a configuration bitstream can be read. The open (O) position indicates a logic zero and the closed (C) position indicates a logic one as shown in Table 17.

Table 17: **Bitstream Address Table**

2	1	0	Addr
O	O	O	0
O	O	C	1
O	C	O	2
O	C	C	3
C	O	O	4
C	O	C	5
C	C	O	6
C	C	C	7

19. RocketIO Transceiver Pins

The RocketIO transceiver pins are shown in Table 18.

Table 18: **RocketIO TX and RX Pin Pairs**

RocketIO Transceiver	MK322			MK325		
	TX Pair (P/N)	RX Pair (P/N)	Die Location	TX Pair (P/N)	RX Pair (P/N)	Die Location
2				A40 /A41	A39 / A38	X9Y1
3				A36 / A37	A35 / A34	X8Y1
4	A26 / A27	A25 / A24	X3Y1	A32/ A33	A31 / A30	X7Y1
5				A28 / A29	A27 / A26	X6Y1
6	A19 / A20	A18 / A17	X2Y1	A24 / A25	A23 / A22	X5Y1
7	A13 / 14	A12 / A11	X1Y1	A20 / A21	A19 / A18	X4Y1
8				A16 / A17	A15 / A14	X3Y1
9	A6 / A7	A5 / A4	X0Y1	A12 / A13	A11 / A10	X2Y1
10				A8 / A9	A7 / A6	X1Y1
11				A4 / A5	A3 / A2	X0Y1
14				BB4 / BB5	BB3 / BB2	X9Y0
15				BB8 / BB9	BB7 / BB6	X8Y0
16	AK6 / AK7	AK5 / AK4	X3Y0	BB12 / BB13	BB11 / BB10	X7Y0
17				BB16 / BB17	BB15 / BB14	X6Y0
18	AK13 / AK14	AK12 / AK11	X2Y0	BB20 / BB21	BB19 / BB18	X5Y0
19	AK19 / AK20	AK18 / AK17	X1Y0	BB24 / BB25	BB23 / BB22	X4Y0
20				BB28 / BB29	BB27 / BB26	X3Y0
21	AK26 / AK27	AK25 / AK24	X0Y0	BB32 / BB33	BB31 / BB30	X2Y0
22				BB36 / BB37	BB35 / BB34	X1Y0
23				BB40 / BB41	BB39 / BB38	X0Y0

20. RS-232 Port Pins

The RS-232 port pins are shown in Table 19. The pins are set up in DTE mode as shown in Figure 3.

Table 19: **RS-232 Port Pins**

FPGA UART Port Name	Direction	Net	MK322	MK325
TXD	OUT	T1IN	AD22	AV34
RTS	OUT	T2IN	AC22	AU34
RXD	IN	R1OUT	AF24	AR34
CTS	IN	R2OUT	AG25	AT34

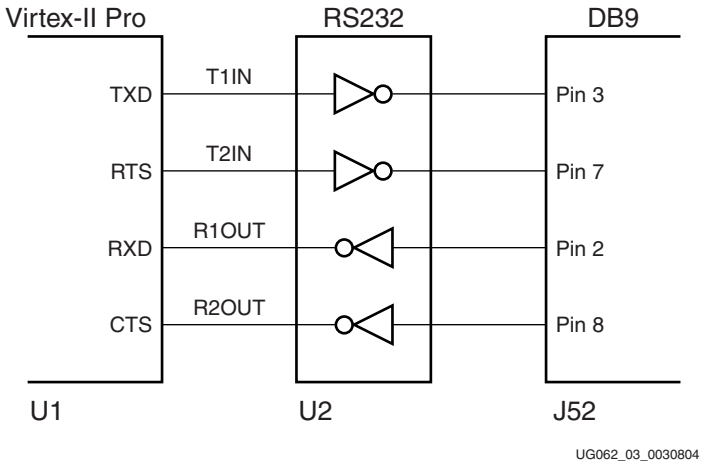

Figure 3: **RS-232 Pins in DTE Mode**

21. SDRAM Connection

The SDRAM port pins are shown in Table 20 (which spans multiple pages).

Table 20: **Headers for the SDRAM signals**

SDRAM PIN	MK322	MK325
A0	U2	AB3
A1	V2	AD4
A2	V1	AE4
A3	U1	AB4
A4	M1	U4
A5	H3	T4
A6	K3	T5

Table 20: **Headers for the SDRAM signals *(Continued)***

SDRAM PIN	MK322	MK325
A7	G3	R3
A8	F3	P3
A9	N2	V4
A10	W1	AE5
A11	E3	N3
A12	D3	N4
DQ0	C1	M2
DQ1	E1	P1
DQ2	D1	N1
DQ3	G1	T2
DQ4	F1	R1
DQ5	K1	V1
DQ6	J1	U1
DQ7	L1	W1
DQ8	K2	W2
DQ9	H2	U2
DQ10	J2	V2
DQ11	F2	R2
DQ12	G2	T3
DQ13	D2	N2
DQ14	E2	P2
DQ15	C2	M3
DQ16	Y1	AD1
DQ17	AB1	AF1
DQ18	AA1	AE1
DQ19	AE1	AH1
DQ20	AD1	AG2
DQ21	AG1	AK1
DQ22	AF1	AJ1
DQ23	AH1	AL2
DQ24	AH2	AL3
DQ25	AF2	AJ2

Table 20: **Headers for the SDRAM signals *(Continued)***

SDRAM PIN	MK322	MK325
DQ26	AG2	AK2
DQ27	AD2	AG3
DQ28	AE2	AH2
DQ29	AB2	AE2
DQ30	AC2	AF2
DQ31	AA2	AD2
BA0	T2	Y3
BA1	W2	Y4
CAS	P2	W4
CKE	J3	W3
RAS	R2	AH3
WE	Y2	AJ3
CS0_A	M2	V5
CS0_B	W3	AK4
CS1_A	U3	AD3
CS1_B	AB3	AL4
UDQM_A	T3	AF3
UDQM_B	AA3	AF4
LDQM_A	L2	U3
LDQM_B	V3	AK3
CLK_A	N1	AA3
CLK_B	P1	AA4
CLK_FB	AJ15	AT21

Note:

1. For proper operation of the SDRAM, use the LVCMOSDCI25 voltage standard on the FPGA pins.
2. Disable the SDRAM when using the DUT pins as standard I/O pins.