Product Not Recommended for New Designs

ML310 User Guide

Virtex-II Pro Embedded Development Platform

UG068 (v1.1.5) February 1, 2007

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/15/04	1.0	Initial Xilinx release.
09/28/04	1.1	Added callouts to Figure 2-1, page 14. Performed miscellaneous edits.
10/04/04	1.1.1	Minor non-technical edits.
11/02/04	1.1.2	Corrected typos in Table 2-10, page 33 and Table 2-12, page 38. Clarified information in Table 2-12, page 38 and Table 2-13, page 38.
11/12/04	1.1.3	Corrected typo in Table 2-3, page 24.
01/14/05	1.1.4	Corrected typos in Table 2-35, page 70.
02/01/07	1.1.5	Revised URL link to *PowerPC Processor Reference Guide* (UG011).

Table of Contents

Preface

About This Guide

This manual accompanies the ML310 Embedded Development System and contains information about the ML310 Hardware Platform and software tools.

Guide Contents

This manual contains the following chapters:

- Chapter 1, "Introduction to Virtex-II Pro, ISE, and EDK," provides an overview of the hardware and software features
- Chapter 2, "ML310 Embedded Development Platform," provides an overview of the embedded development platform and details the components and features of the ML310 board

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/literature.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*

Convention	Meaning or Use	Example
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	`ngdbuild` *design_name*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as `bus[7:0]`, they are required.	`ngdbuild` [*option_name*] *design_name*
Braces { }	A list of items from which you must choose one or more	`lowpwr ={on|off}`
Vertical bar |	Separates items in a list of choices	`lowpwr ={on|off}`

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis . . .	Repetitive material that has been omitted	`allow block` *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Platform FPGA User Guide.*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Chapter 1

Introduction to Virtex-II Pro, ISE, and EDK

Virtex-II Pro FPGAs

The Virtex™-II Pro Platform FPGA solution is the most technically sophisticated silicon and software product development in the history of the programmable logic industry. The goal was to revolutionize system architecture "from the ground up." To achieve that objective, the best circuit engineers and system architects from IBM, Mindspeed, and Xilinx co-developed the world's most advanced Platform FPGA silicon product. Leading teams from top embedded systems companies worked together with Xilinx software teams to develop the systems software and IP solutions that enabled new system architecture paradigm.

The result is the first Platform FPGA solution capable of implementing high performance system-on-a-chip designs previously the exclusive domain of custom ASICs, yet with the flexibility and low development cost of programmable logic. The Virtex-II Pro family marks the first paradigm change from programmable logic to programmable systems, with profound implications for leading-edge system architectures in networking applications, deeply embedded systems, and digital signal processing systems. It allows custom user-defined system architectures to be synthesized, next-generation connectivity standards to be seamlessly bridged, and complex hardware and software systems to be co-developed rapidly with in-system debug at system speeds. Together, these capabilities usher in the next programmable logic revolution.

Summary of Virtex-II Pro Features

The Virtex-II Pro has an impressive collection of both programmable logic and hard IP that has historically been the domain of the ASICs.

- High-performance Platform FPGA solution including
  - Up to twenty RocketIO™ embedded multi-gigabit transceiver blocks (based on Mindspeed's SkyRail™ technology)
  - Up to two IBM® PowerPC™ RISC processor blocks
- Based on Virtex-II Platform FPGA technology
  - Flexible logic resources, up to 99,216 Logic Cells
  - SRAM-based in-system configuration
  - Active Interconnect™ technology
  - SelectRAM™ memory hierarchy
  - Up to 444 dedicated 18-bit x 18-bit multiplier blocks
  - High-performance clock management circuitry
  - SelectIO™-Ultra technology
  - Digitally Controlled Impedance (DCI) I/O

Table 1-1: **Virtex-II Pro Family Members**

Device	XC2VP2	XC2VP4	XC2VP7	XC2VP20	XC2VP30	XC2VP40	XC2VP50	XC2VP70	XC2VP100
Logic Cells	3,168	6,768	11,088	20,880	30,816	43,632	53,136	74,448	99,216
PPC405	0	1	1	2	2	2	2	2	2
MGTs	4	4	8	8	8	12	16	20	20
BRAM (kb)	216	504	792	1,584	2,448	3,456	4,176	5,904	7,992
Xtreme Multipliers	12	28	44	88	136	192	232	328	444

PowerPC™ 405 Core

- Embedded 300+ MHz Harvard architecture core
- Low power consumption: 0.9 mW/MHz
- Five-stage data path pipeline
- Hardware multiply/divide unit
- Thirty-two 32-bit general purpose registers
- 16 kB two-way set-associative instruction cache
- 16 kB two-way set-associative data cache
- Memory Management Unit (MMU)
  - 64-entry unified Translation Look-aside Buffers (TLB)
  - Variable page sizes (1 kB to 16 MB)
- Dedicated on-chip memory (OCM) interface
- Supports IBM CoreConnect™ bus architecture
- Debug and trace support
- Timer facilities

RocketIO 3.125 Gb/s Transceivers

- Full-duplex serial transceiver (SERDES) capable of baud rates from 622 Mb/s to 3.125 Gb/s
- 80 Gb/s duplex data rate (16 channels)
- Monolithic clock synthesis and clock recovery (CDR)
- Fibre Channel, Gigabit Ethernet, 10 Gb Attachment Unit Interface (XAUI), and Infiniband-compliant transceivers
- 8-, 16-, or 32-bit selectable internal FPGA interface
- 8B /10B encoder and decoder
- 50Ω/75Ω on-chip selectable transmit and receive terminations
- Programmable comma detection
- Channel bonding support (two to sixteen channels)
- Rate matching via insertion/deletion characters

- Four levels of selectable pre-emphasis
- Five levels of output differential voltage
- Per-channel internal loopback modes
- 2.5V transceiver supply voltage

Virtex-II FPGA Fabric

Description of the Virtex-II Family fabric follows:

- SelectRAM memory hierarchy
  - Up to 10 Mb of True Dual-Port RAM in 18 kb block SelectRAM resources
  - Up to 1.7 Mb of distributed SelectRAM resources
  - High-performance interfaces to external memory
- Arithmetic functions
  - Dedicated 18-bit x 18-bit multiplier blocks
  - Fast look-ahead carry logic chains
- Flexible logic resources
  - Up to 111,232 internal registers/latches with Clock Enable
  - Up to 111,232 look-up tables (LUTs) or cascadable variable (1 to 16 bits) shift registers
  - Wide multiplexers and wide-input function support
  - Horizontal cascade chain and Sum-of-Products support
  - Internal 3-state busing
- High-performance clock management circuitry
  - Up to eight Digital Clock Manager (DCM) modules
    - Precise clock de-skew
    - Flexible frequency synthesis
    - High-resolution phase shifting
  - 16 global clock multiplexer buffers in all parts
- Active Interconnect technology
  - Fourth-generation segmented routing structure
  - Fast, predictable routing delay, independent of fanout
  - Deep sub-micron noise immunity benefits
- Select I/O-Ultra technology
  - Up to 852 user I/Os
  - Twenty two single-ended standards and five differential standards
  - Programmable LVTTL and LVCMOS sink/source current (2 mA to 24 mA) per I/O
  - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
  - PCI support(1)
  - Differential signaling

- 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
- Bus LVDS I/O
- HyperTransport™ (LDT) I/O with current driver buffers
- Built-in DDR input and output registers

- Proprietary high-performance SelectLink technology for communications between Xilinx devices
  - High-bandwidth data path
  - Double Data Rate (DDR) link
  - Web-based HDL generation methodology
- SRAM-based in-system configuration
  - Fast SelectMAP™ configuration
  - Triple Data Encryption Standard (DES) security option (bitstream encryption)
  - IEEE1532 support
  - Partial reconfiguration
  - Unlimited reprogrammability
  - Readback capability
- Supported by Xilinx Foundation™ and Alliance™ series development systems
  - Integrated VHDL and Verilog design flows
  - ChipScope™ Pro Integrated Logic Analyzer
- 0.13-µm, nine-layer copper process with 90 nm high-speed transistors
- 1.5V (VCCINT) core power supply, dedicated 2.5V VCCAUX auxiliary and VCCO I/O power supplies
- IEEE 1149.1 compatible boundary-scan logic support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) packages in standard 1.00 mm pitch
- Each device 100% factory tested

Foundation ISE

ISE Foundation is the industry's most complete programmable logic design environment. ISE Foundation includes the industry's most advanced timing driven implementation tools available for programmable logic design, along with design entry, synthesis and verification capabilities. With its ultra-fast runtimes, ProActive Timing Closure technologies, and seamless integration with the industry's most advanced verification products, ISE Foundation offers a great design environment for anyone looking for a complete programmable logic design solution.

Foundation Features

Design Entry

ISE greatly improves your "Time-to-Market", productivity, and design quality with robust design entry features.

ISE provides support for today's most popular methods for design capture including HDL and schematic entry, integration of IP cores as well as robust support for reuse of your own

IP. ISE even includes technology called IP Builder, which allows you to capture your own IP and reuse it in other designs.

ISE's Architecture Wizards allow easy access to device features like the Digital Clock Manager and Multi-Gigabit I/O technology.

ISE also includes a tool called PACE (Pinout Area Constraint Editor) which includes a front-end pin assignment editor, a design hierarchy browser, and an area constraint editor. By using PACE, designers are able to observe and describe information regarding the connectivity and resource requirements of a design, resource layout of a target FPGA, and the mapping of the design onto the FPGA via location/area.

This rich mixture of design entry capabilities provides the easiest to use design environment available today for your logic design.

Synthesis

Synthesis is one of the most essential steps in your design methodology. It takes your conceptual Hardware Description Language (HDL) design definition and generates the logical or physical representation for the targeted silicon device.

A state of the art synthesis engine is required to produce highly optimized results with a fast compile and turnaround time. To meet this requirement, the synthesis engine needs to be tightly integrated with the physical implementation tool and have the ability to proactively meet the design timing requirements by driving the placement in the physical device. In addition, cross probing between the physical design report and the HDL design code will further enhance the turnaround time.

Xilinx ISE provides the seamless integration with the leading synthesis engines from Mentor Graphics, Synopsys, and Synplicity. You can use the synthesis engine of our choice. In addition, ISE includes Xilinx proprietary synthesis technology, XST. You have options to use multiple synthesis engines to obtain the best-optimized result of your programmable logic design.

Implementation and Configuration

Programmable logic design implementation assigns the logic created during design entry and synthesis into specific physical resources of the target device.

The term “place and route” has historically been used to describe the implementation process for FPGA devices and “fitting” has been used for CPLDs. Implementation is followed by device configuration, where a bitstream is generated from the physical place and route information and downloaded into the target programmable logic device.

To ensure designers get their product to market quickly, Xilinx ISE software provides several key technologies required for design implementation:

- Ultra-fast runtimes enable multiple “turns” per day
- ProActive™ Timing Closure drives high-performance results
- Timing-driven place and route combined with “push-button” ease
- Incremental Design
- Macro Builder

Board Level Integration

Xilinx understands the critical issues such as complex board layout, signal integrity, high-speed bus interface, high-performance I/O bandwidth, and electromagnetic interference for system level designers.

To ease the system level designers' challenge, ISE provides support to all Xilinx leading FPGA technologies:

- System IO
- XCITE
- Digital clock management for system timing
- EMI control management for electromagnetic interference

To really help you ensure your programmable logic design works in context of your entire system, Xilinx provides complete pin configurations, packaging information, tips on signal integration, and various simulation models for your board level verification including:

- IBIS models
- HSPICE models
- STAMP models

Embedded Development Kit

The Embedded Development Kit (EDK) is Xilinx's solution for embedded programmable systems design and supports designs using the Virtex-II Pro FPGA. EDK hardware and software development tools, combined with the advanced features of Virtex-II Pro FPGA provide you with a new level of system design.

The system design process can be loosely divided into the following tasks:

- Build the software application
- Simulate the hardware description
- Simulate the hardware with the software application
- Simulate the hardware into the FPGA using the software application in on-chip memory
- Run timing simulation
- Configure the bitstream for the FPGA

Chapter 2

ML310 Embedded Development Platform

Overview

The ML310 Embedded Development Platform offers designers a versatile Virtex-II Pro XC2VP30-FF896 based platform for rapid prototyping and system verification. In addition to the more than 30,000 logic cells, over 2,400 kb of block RAM (BRAM), dual IBM PowerPC™ 405 (PPC405) processors, and RocketIO multi-gigabit transceivers (MGTs) available in the FPGA, the ML310 provides an onboard Ethernet MAC/PHY, DDR memory, multiple PCI bus slots, and standard front panel interface ports within an ATX form factor motherboard. An integrated System ACE CompactFlash (CF) controller is deployed to perform board bring-up and to load applications from the included 512 MB CompactFlash card.

A CD packaged with the ML310 contains documentation and files, including tutorials, device data sheets, reference designs, and utilities. Up-to-date documentation and files are available on the Xilinx website at www.xilnx.com/ml310. The EDK *Processor IP User Guide* should be reviewed as well as the data sheets corresponding to the devices listed in "Board Hardware." See "Related Documents" for further information.

The setup and quickstart documentation highlights the functionality of the ML310 using the applications shipped on the included CompactFlash card. The reference designs were produced using the Xilinx Embedded Development Kit (EDK), ISE, and Answer Browser solution records. Tutorials, in coordination with Xilinx documentation for EDK, ISE, and the Answer Browser, describe how the reference designs and applications were produced. These tutorials can be used to re-create the applications provided and also as a basis for the development of new designs. Xilinx EDK provides for the development of basic board-specific systems, beginning with Base System Builder (BSB), to highly customized systems that leverage the flexibility of Xilinx Platform Studio (XPS) and the EDK intellectual property (IP).

An image of the ML310 board and its corresponding block diagram are shown in Figure 2-1, page 14 and Figure 2-2, page 15 respectively.

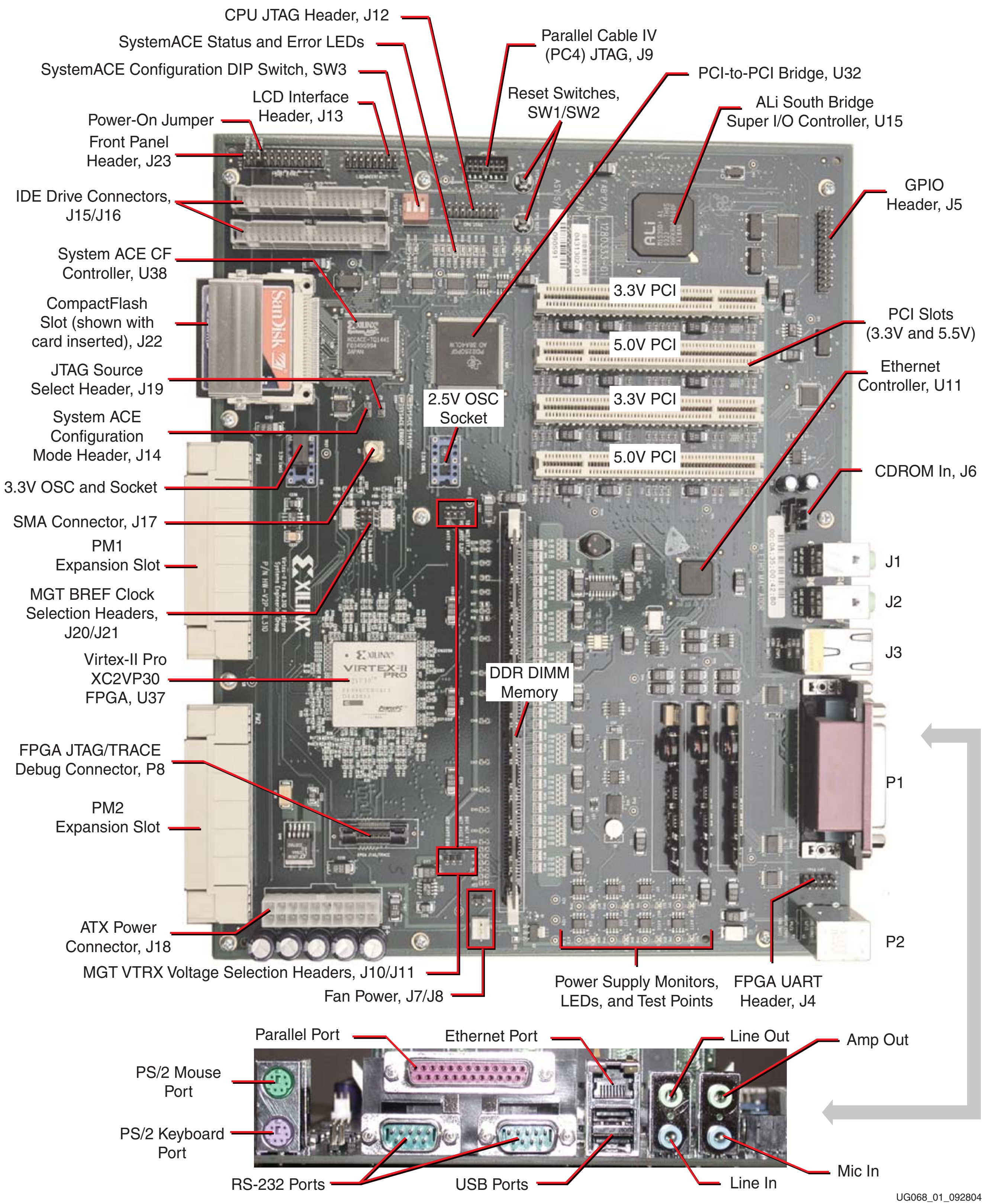

Figure 2-1: **ML310 Board and Front Panel Detail**

Figure 2-2 shows a high-level block diagram of the ML310 and its peripherals.

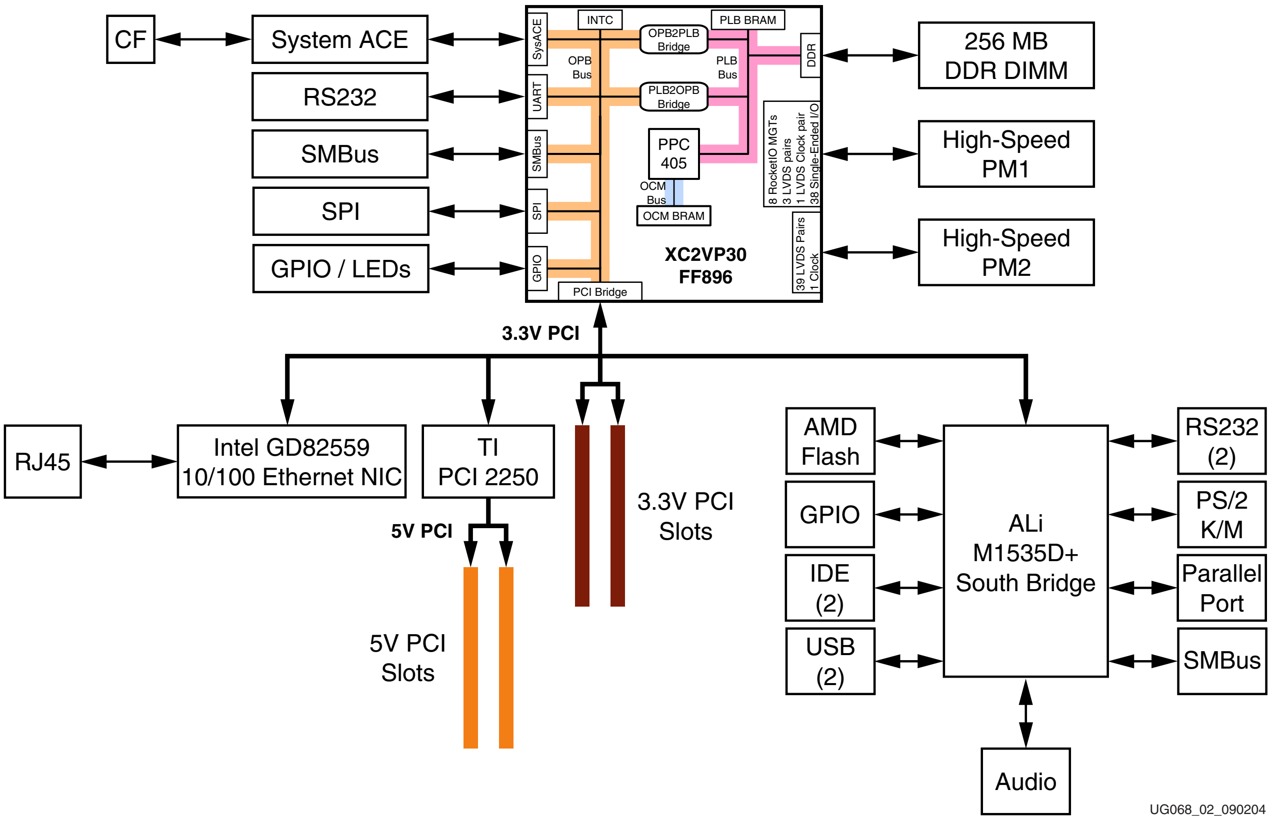

Figure 2-2: **ML310 High-Level Block Diagram**

Features

In addition to the Virtex-II Pro™ FPGA with the embedded PPC405, the ML310 board features the following:

- ATX form factor motherboard
- 256 MB DDR DIMM
- System ACE™ CF controller
- 512 MB CompactFlash card
- Onboard 10/100 Ethernet network interface card (NIC)
- 4 PCI slots (3.3V and 5V)
- LCD character display and cable
- FPGA serial port connection
- RS-232 mini-cable
- Personality module interface for RocketIO MGT and LVDS access
- Standard JTAG connectivity
- ALi South Bridge Super I/O controller
  - 1 parallel and 2 serial ports
  - 2 Universal Serial Bus (USB) ports

- 2 IDE connectors
- General purpose I/O (GPIO)
- System Management Bus (SMBus) interface
- AC'97 audio codec
- PS/2 keyboard and mouse ports
- ATX power supply

Related Documents

Prior to using the ML310 Embedded Development Platform, the user should be familiar with the following:

- *Processor IP User Guide*
  http://www.xilinx.com/ise/embedded/proc_ip_ref_guide.pdf
- *System ACE CompactFlash Solution*
  http://www.xilinx.com/bvdocs/publications/ds080.pdf
- *Virtex-II Pro and Virtex-II Pro X Platform FPGAs Data Sheet*
  http://xilinx.com/bvdocs/publications/ds083.pdf
- *RocketIO Transceiver User Guide*
  http://www.xilinx.com/bvdocs/userguides/ug024.pdf
- *Virtex-II Pro Platform FPGA User Guide*
  http://www.xilinx.com/bvdocs/userguides/ug012.pdf
- *PowerPC Processor Reference Guide*
  http://www.xilinx.com/bvdocs/userguides/ug011.pdf
- *PowerPC 405 Processor Block Reference Guide, Embedded Development Kit*
  http://www.xilinx.com/bvdocs/userguides/ug018.pdf

See the following locations for documentation on Xilinx tools and solutions:

- EDK: http://www.xilinx.com/edk
- ISE: http://www.xilinx.com/ise
- Answer Browser: http://www.xilinx.com/support
- ML310: http://www.xilinx.com/ml310

Board Hardware

The ML310 Virtex-II Pro FPGA is connected to several peripherals (listed below). The peripherals are either directly connected to the FPGA or indirectly accessible by way of the PCI bus. The sections that follow describe the main features of each of the peripherals and how they interface with the FPGA.

- DDR DIMM memory*
- FPGA UART*
- System ACE CF controller*
- GPIO LEDs/LCD*
- PCI bus interface*
  - ALi M1535D+ PCI device
  - Intel Ethernet/NIC PCI device

- IIC/SMBus Interface*
    - LTC1694 SMBus accelerator
    - RTC8566 Real Time Clock (RTC)
    - 64 kb 24LC64 EEPROM
    - LM87 voltage/temp monitor
    - DDR DIMM SPD EEPROM
- SPI EEPROM*
- High-speed I/O through RocketIO MGTs

Note: * Compatible with EDK supported IP and software drivers.

Clock Generation

The ML310 board employs a Xilinx XC2VP30-FF896 FPGA. Several clocks are distributed throughout the ML310 as illustrated in Figure 2-3, page 18. The main system clock is a 100 MHz oscillator, X10. The system clock is typically used to generate multiple clocks with varying frequency and phases within the FPGA fabric by using the Virtex-II Pro Digital Clock Managers (DCMs). The FPGA also generates and drives clocks required by the DDR DIMM memory and PCI bus interfaces.

The FPGA requires different banking voltages that are set based on the I/O voltage interface requirements of each device that is directly connected to the FPGA. Banks 1 and 2 are set to 3.0V, while the remaining six banks are set to 2.5V, as shown in Figure 2-3, page 18. The Virtex-II Pro FPGA I/O can be configured to use different I/O standards such as SSTL2 as required on the DDR DIMM interface. Please review DS083: *Virtex-II Pro and Virtex-II Pro X Platform FPGAs Data Sheet* for more information regarding I/O standards.

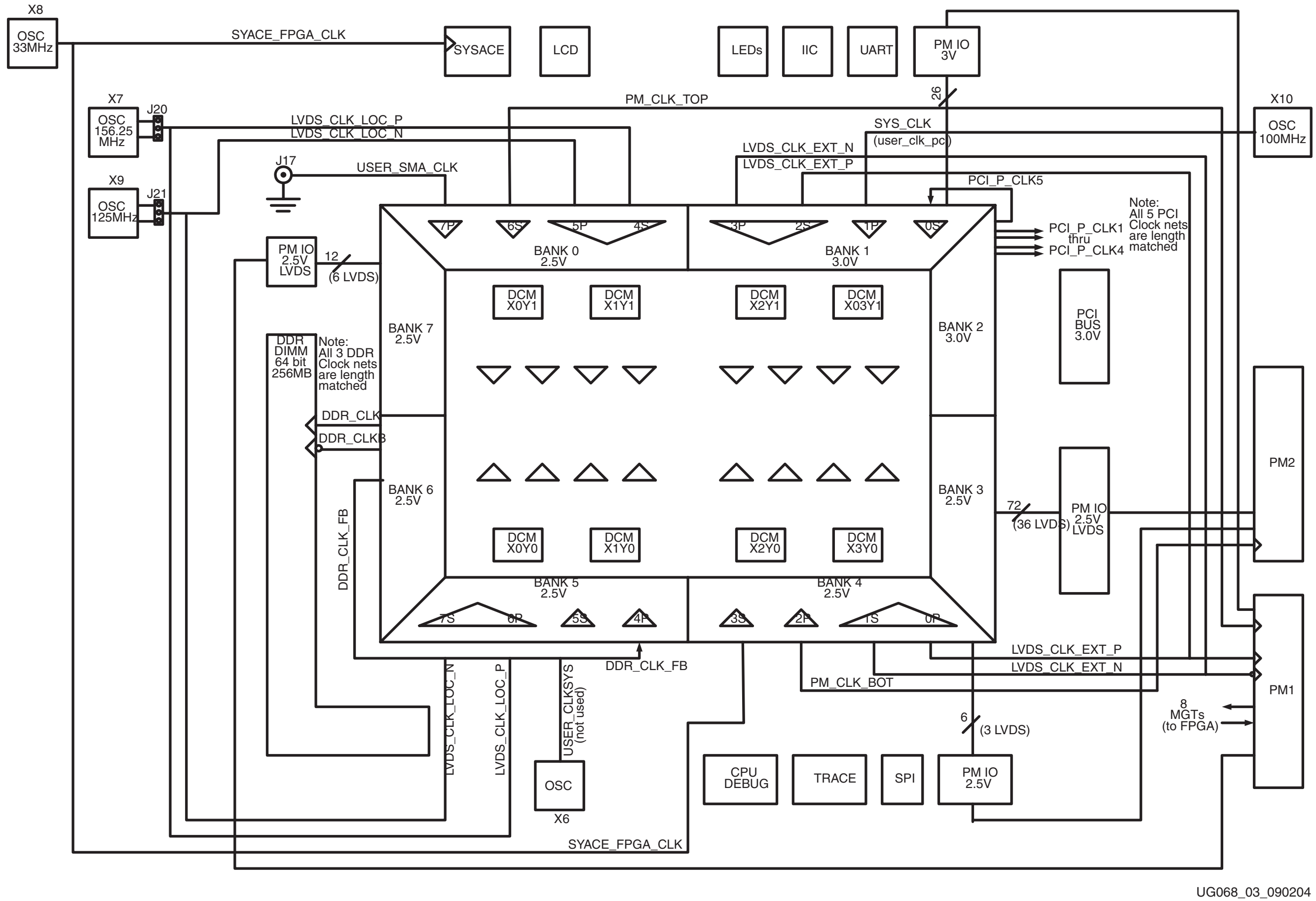

Figure 2-3: **Top-Level Clocking**

Table 2-1: **Clock Connections**

Schem Net Name	Clock Source	XC2VP30 Pin (U37)	Description
USER_CLKPCI	X10	B15	100 MHz system clock oscillator (3.3V)
USER_CLKSYS	X6	AG16	User clock oscillator (2.5V)[1]
USER_SMA_CLK	X6	C16	User clock oscillator (2.5V)[1]
PM_CLK_TOP	PM1.F9	B16	Personality module clock (top) (2.5V)[2]
PM_CLK_BOT	PM2.F10	AG15	Personality module clock (bottom) (2.5V)[2]
LVDS_CLKEXT_P	PM1.F12	G15 and AJ15	LVDS pair (2.5V)[2]
LVDS_CLKEXT_N	PM1.F11	F15 and AH15	LVDS pair (2.5V)[2]
LVDS_CLKLOC_P	X9.4 or X7.4	F16 and AH16	156.26/125.00 MHz selectable LVDS pair (2.5V)[2]

Table 2-1: **Clock Connections *(Continued)***

Schem Net Name	Clock Source	XC2VP30 Pin (U37)	Description
LVDS_CLKLOC_N	X9.5 or X7.5	G16 and AJ16	156.26/125.00 MHz selectable LVDS pair (2.5V)[2]

Notes:

1. The 2.5V X6 socket is not populated. User must provide oscillator.
2. See "High-Speed I/O," page 59.

DDR Memory

DDR DIMM

The ML310 includes a registered 256 MB PC3200 double data rate (DDR) Dual Inline Memory Module (DIMM) with an industry-standard 184-pin count. The DDR DIMM is commercially available from Wintec Industries as part number W4F232726HA-5Q. The DDR DIMM is manufactured using nine Infineon HYB25D256800BT-5, 32Mx8 DDR SDRAM devices with 13-row address lines, 10-column address lines, and four bank select lines. Read and write access to the Infineon devices is programmable in burst lengths of 2-, 4-, or 8-column locations. The memory module inputs and outputs are compatible with SSTL2 signaling. Serial Presence Detect (SPD) using an SMBus interface to the DDR DIMM is also supported. See the "IIC/SMBus Interface" section for more details on accessing the DIMM module's SPD EEPROM.

DDR Signaling

The FPGA DDR DIMM interface supports SSTL2 signaling. All DDR signals are controlled impedance and are SSTL2 terminated.

DDR Memory Expansion

The FPGA is capable of replicating up to three differential clock output pairs to the DIMM in order to support either registered or unbuffered DIMMs. The ML310 DDR interface is very flexible in the event different DDR memory is desired such as an unbuffered DIMM or increased memory size. The DDR interface core delivered with EDK supports both registered and unbuffered DRR memory interfaces. Please review the EDK *Processor IP User Guide* when migrating to a different DDR DIMM.

Figure 2-4 is a block diagram of the DDR DIMM interface.

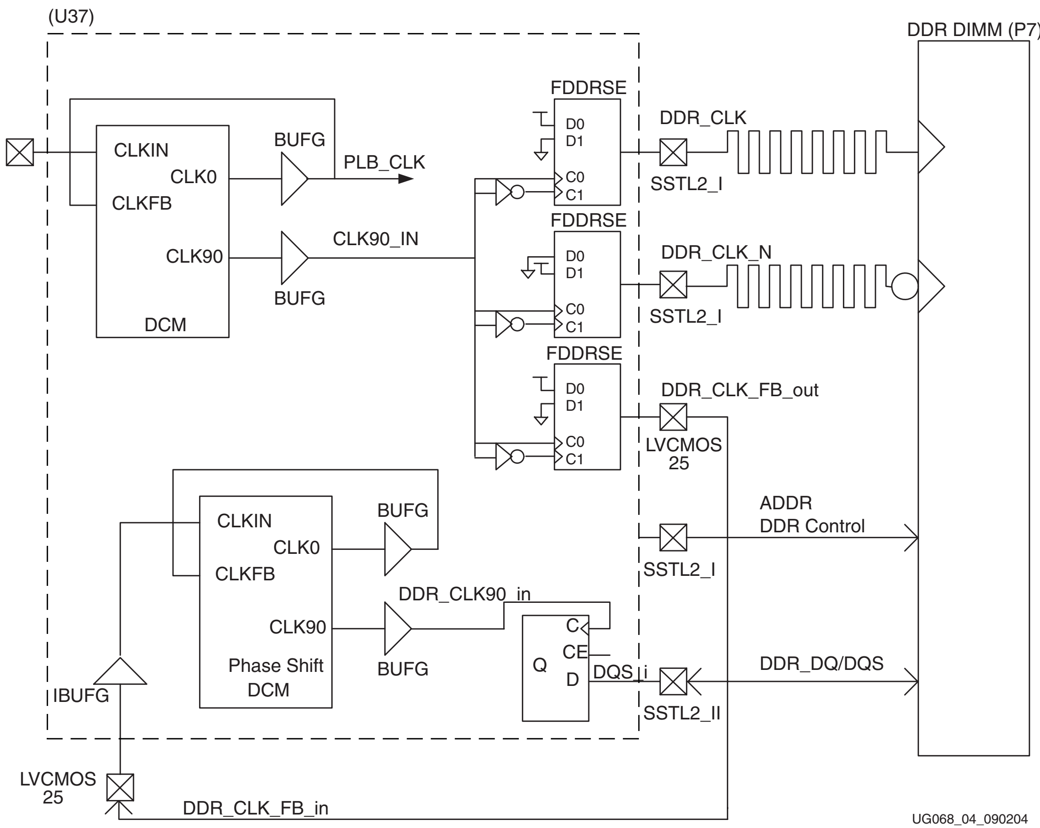

Figure 2-4: **DDR DIMM Interface Block Diagram**

Table 2-2 lists the connections from the FPGA to the DDR DIMM interface. Note that the DDR_DQ signal names do not correlate as the FPGA uses IBM notation, big endian, while the DDR DIMMs use Intel notation, little endian.

Table 2-2: **Connections from FPGA to DIMM Interface (P7)**

UCF Signal Name	XC2VP30 Pin (U37)	Schem Signal Name	DIMM (P7)
ddr_ad[0]	AE23	DDR_A0	48
ddr_ad[1]	AJ23	DDR_A1	43
ddr_ad[2]	AG20	DDR_A2	41
ddr_ad[3]	AF23	DDR_A3	130
ddr_ad[4]	AH22	DDR_A4	37
ddr_ad[5]	AF22	DDR_A5	32
ddr_ad[6]	AF21	DDR_A6	125
ddr_ad[7]	AH21	DDR_A7	29
ddr_ad[8]	AG21	DDR_A8	122
ddr_ad[9]	AJ21	DDR_A9	27
ddr_ad[10]	AK21	DDR_A10	141

Table 2-2: **Connections from FPGA to DIMM Interface (P7) *(Continued)***

UCF Signal Name	XC2VP30 Pin (U37)	Schem Signal Name	DIMM (P7)
ddr_ad[11]	AH20	DDR_A11	118
ddr_ad[12]	AF20	DDR_A12	115
ddr_ba[0]	AG18	DDR_BA0	59
ddr_ba[1]	AF19	DDR_BA1	62
ddr_casb	AF17	DDR_CAS_N	65
ddr_cke	AG24	DDR_CKE0	21
ddr_csb	AE17	DDR_S0_N	157
ddr_rasb	AE16	DDR_RAS_N	154
ddr_web	AD16	DDR_WE_N	63
ddr_clk	V30	DDR_CK0	137
ddr_clkb	U30	DDR_CK0_N	138
ddr_clk_fb	AF16	DDR_CLK_FB	N/A
ddr_clk_fb_out	AG25	DDR_CLK_FB	N/A
ddr_dm[0]	AH29	DDR_DQM07	177
ddr_dm[1]	AE29	DDR_DQM06	169
ddr_dm[2]	AA24	DDR_DQM05	159
ddr_dm[3]	AB30	DDR_DQM04	149
ddr_dm[4]	P30	DDR_DQM03	129
ddr_dm[5]	M30	DDR_DQM02	119
ddr_dm[6]	K24	DDR_DQM01	107
ddr_dm[7]	E30	DDR_DQM00	97
ddr_dqs[0]	AG30	DDR_DQS07	86
ddr_dqs[1]	AF30	DDR_DQS06	78
ddr_dqs[2]	AA28	DDR_DQS05	67
ddr_dqs[3]	Y29	DDR_DQS04	56
ddr_dqs[4]	P28	DDR_DQS03	36
ddr_dqs[5]	M29	DDR_DQS02	25
ddr_dqs[6]	H29	DDR_DQS01	14
ddr_dqs[7]	F29	DDR_DQS00	5
ddr_dq[0]	AG28	DDR_DQ63	179
ddr_dq[1]	AG26	DDR_DQ62	178
ddr_dq[2]	AE26	DDR_DQ61	175
ddr_dq[3]	AD26	DDR_DQ60	174
ddr_dq[4]	AH27	DDR_DQ59	88
ddr_dq[5]	AH26	DDR_DQ58	87

Table 2-2: **Connections from FPGA to DIMM Interface (P7) *(Continued)***

UCF Signal Name	XC2VP30 Pin (U37)	Schem Signal Name	DIMM (P7)
ddr_dq[6]	AF25	DDR_DQ57	84
ddr_dq[7]	AD25	DDR_DQ56	83
ddr_dq[8]	AF28	DDR_DQ55	171
ddr_dq[9]	AD28	DDR_DQ54	170
ddr_dq[10]	AB25	DDR_DQ53	166
ddr_dq[11]	AB26	DDR_DQ52	165
ddr_dq[12]	AF27	DDR_DQ51	80
ddr_dq[13]	AD27	DDR_DQ50	79
ddr_dq[14]	AC25	DDR_DQ49	73
ddr_dq[15]	AC26	DDR_DQ48	72
ddr_dq[16]	AC27	DDR_DQ47	162
ddr_dq[17]	AC28	DDR_DQ46	161
ddr_dq[18]	AA26	DDR_DQ45	155
ddr_dq[19]	Y26	DDR_DQ44	153
ddr_dq[20]	AB27	DDR_DQ43	69
ddr_dq[21]	AB28	DDR_DQ42	68
ddr_dq[22]	AA25	DDR_DQ41	64
ddr_dq[23]	Y27	DDR_DQ40	61
ddr_dq[24]	W28	DDR_DQ39	151
ddr_dq[25]	W25	DDR_DQ38	150
ddr_dq[26]	V27	DDR_DQ37	147
ddr_dq[27]	V25	DDR_DQ36	146
ddr_dq[28]	W27	DDR_DQ35	60
ddr_dq[29]	W26	DDR_DQ34	57
ddr_dq[30]	V28	DDR_DQ33	55
ddr_dq[31]	V26	DDR_DQ32	53
ddr_dq[32]	N27	DDR_DQ31	133
ddr_dq[33]	P26	DDR_DQ30	131
ddr_dq[34]	R25	DDR_DQ29	127
ddr_dq[35]	R27	DDR_DQ28	126
ddr_dq[36]	N28	DDR_DQ27	40
ddr_dq[37]	P27	DDR_DQ26	39
ddr_dq[38]	R26	DDR_DQ25	35
ddr_dq[39]	R28	DDR_DQ24	33
ddr_dq[40]	K27	DDR_DQ23	123

Table 2-2: **Connections from FPGA to DIMM Interface (P7) *(Continued)***

UCF Signal Name	XC2VP30 Pin (U37)	Schem Signal Name	DIMM (P7)
ddr_dq[41]	L26	DDR_DQ22	121
ddr_dq[42]	M27	DDR_DQ21	117
ddr_dq[43]	N26	DDR_DQ20	114
ddr_dq[44]	K28	DDR_DQ19	31
ddr_dq[45]	L27	DDR_DQ18	28
ddr_dq[46]	M28	DDR_DQ17	24
ddr_dq[47]	N25	DDR_DQ16	23
ddr_dq[48]	K25	DDR_DQ15	110
ddr_dq[49]	K26	DDR_DQ14	109
ddr_dq[50]	J27	DDR_DQ13	106
ddr_dq[51]	J28	DDR_DQ12	105
ddr_dq[52]	M25	DDR_DQ11	20
ddr_dq[53]	M26	DDR_DQ10	19
ddr_dq[54]	J25	DDR_DQ09	13
ddr_dq[55]	J26	DDR_DQ08	12
ddr_dq[56]	H28	DDR_DQ07	99
ddr_dq[57]	G27	DDR_DQ06	98
ddr_dq[58]	F28	DDR_DQ05	95
ddr_dq[59]	E27	DDR_DQ04	94
ddr_dq[60]	H27	DDR_DQ03	8
ddr_dq[61]	G28	DDR_DQ02	6
ddr_dq[62]	F27	DDR_DQ01	4
ddr_dq[63]	E28	DDR_DQ00	2

An unbuffered DIMM requires more than one clock input pair versus a single clock input pair for a registered DIMM. Table 2-3 shows clocking connections that are required for interfacing the FPGA to unbuffered DDR DIMMs.

Table 2-3: **Optional DDR DIMM Clocks for Use with Unbuffered DIMMs**

Schem Signal Name	XC2VP30 Pin (U37)	DIMM (P7)
DDR_CK1	K29	16
DDR_CK1_N	L29	17
DDR_CK2	AD30	76
DDR_CK2_N	AD29	75

Note:
All three DDR differential clock pairs are length matched and controlled impedance.

Serial Port FPGA UART

Introduction to Serial Ports

Serial ports are useful as simple, low-speed interfaces between *data terminal equipment* (DTE) such as PCs or terminals and *data communication equipment* (DCE) such as modems. A DTE-to-DCE connection uses a "straight-through" type of cable in which the transmit (TX) and receive (RX) wires of one end of the cable directly connect to the corresponding TX and RX wires on the other end of the cable. A DTE-to-DTE connection uses a "null-modem" type of cable which cross-wires the TX and RX signals from one end of the cable to the RX and TX signals on the other end. Since the ML310 is a DTE, use a null modem cable when connecting to another DTE such as a personal computer (PC).

RS-232 Standard

The RS-232 standard specifies output voltage levels between -5V to -15V for logic 1 and +5V to +15V for logic 0. Inputs must be compatible with voltages in the range of -3V to -15V for logic 1 and +3V to +15V for logic 0. This ensures data bits are read correctly at the maximum cable length of 50 feet between two RS-232 connected devices.

Note: A negative voltage represents a logic 1 while a positive voltage represents a logic 0. As these signaling levels are quite high compared to current signaling levels, transceivers are often used to convert to more manageable levels.

RS-232 on the ML310

Three RS-232 ports are available on the ML310. Two ports (P1) are connected to the ALi M1535D+ South Bridge controller (U15) and a third port (J4) is connected to the XC2VP30 FPGA (U37) through a MAX3232 Transceiver (U7).

The two P1 ports are wired such that the ML310 is a DTE device. These ports are only accessible by the FPGA through the PCI bus. Please review the "ALi South Bridge Interface, M1535D+ (U15)" section and the M1535D+ data sheet for more information.

The J4 port connects directly to the XC2VP30 FPGA by way of a 10-pin header. It can be accessed by simply implementing a UART in the FPGA fabric. An RS-232 mini-cable adapter included with the ML310 converts the 10-pin header to a DB9 male connector. The adapter is a standard DTK/Intel IDC-10 to DB9 male. The FPGA RS-232 port on the ML310 is wired as a DTE and meets the *EIA/TIA-574* standard.

Note: EDK provides many IP cores, including a UART usable with any member of the Virtex-II Pro family. See the EDK *Processor IP User Guide* for more details.

Figure 2-5 shows the RS-232 connectivity from the XC2VP30 FPGA to the DTK adapter.

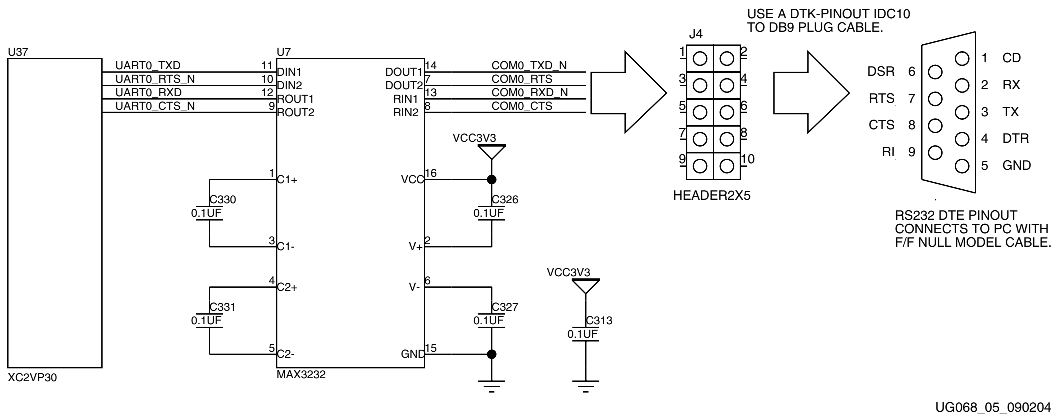

Figure 2-5: **FPGA UART and RS-232 Connectivity**

Table 2-4 shows the RS-232 connections to the XCV2VP30 FPGA.

Table 2-4: **FPGA RS-232 Connections**

UCF Signal Name	XC2VP30 Pin (U37)	Schem Signal Name	10-Pin Header (J4)	DTK Adapter (DB9)
uart1_ctsn	B10	UART0_CTS_N	6	8
uart1_rtsn	G14	UART0_RTS_N	4	7
uart1_sin	F14	UART0_RXD	3	2
uart1_sout	F12	UART0_TXD	5	3

System ACE CF Controller

Board Bring-Up

The System ACE CF controller is the primary means of configuring the XC2VP30 on the ML310 board through the JTAG interface. The System ACE CF controller is located between the JTAG connector and the XC2VP30, and passes the JTAG signals back and forth between the two. During configuration, the System ACE CF controller has full control of the JTAG signals.

Non-Volatile Storage

In addition to programming the FPGA and storing bitstreams, the System ACE CF controller can be used to facilitate general-use, non-volatile storage. The System ACE CF controller provides an MPU interface for allowing a microprocessor to access the CompactFlash memory, enabling the use of the CompactFlash card as a file system.

XC2VP30 Connectivity

The System ACE CF controller is connected to the XC2VP30 through the JTAG chain, for configuration, and through the MPU port of the System ACE, for allowing the XC2VP30 to control System ACE and access the CompactFlash. Table 2-5 shows the connection between the System ACE CF controller and the XC2VP30. It shows the signal names with associated pins on System ACE and the XC2VP30 for both the MPU interface.

Table 2-5: **System ACE MPU Connection from FPGA to Controller**

UCF Signal Name	XC2VP30 Pin (U37)	Schem Signal Name	System ACE (U38)
sysace_clk_in	AF15	sysace_clk_in	93
sysace_clk_oe	C22	sysace_clk_oe	77
sysace_mpa[0]	B22	sysace_mpa[0]	70
sysace_mpa[1]	E19	sysace_mpa[1]	69
sysace_mpa[2]	E18	sysace_mpa[2]	68
sysace_mpa[3]	H19	sysace_mpa[3]	67
sysace_mpa[4]	G19	sysace_mpa[4]	45
sysace_mpa[5]	B23	sysace_mpa[5]	44
sysace_mpa[6]	A23	sysace_mpa[6]	43
sysace_mpd[0]	E20	sysace_mpd[0]	66
sysace_mpd[1]	D20	sysace_mpd[1]	65
sysace_mpd[2]	H20	sysace_mpd[2]	63
sysace_mpd[3]	G20	sysace_mpd[3]	62
sysace_mpd[4]	D23	sysace_mpd[4]	61
sysace_mpd[5]	C23	sysace_mpd[5]	60
sysace_mpd[6]	E21	sysace_mpd[6]	59
sysace_mpd[7]	D21	sysace_mpd[7]	58
sysace_mpoe	E23	sysace_mpoe	77
sysace_mpce	E22	sysace_mpce	42
sysace_mpwe	G23	sysace_mpwe	76
sysace_mpirq	F23	sysace_mpirq	41

JTAG

JTAG (Joint Test Action Group) is a simple interface that provides for many uses. On the ML310 Hardware Platform, the primary uses include configuration of the XC2VP30, debugging software (similar to the CPU debug interface), and debugging hardware using the ChipScope™ Integrated Logic Analyzer (ILA).

The Virtex-II Pro family is fully compliant with the *IEEE Standard 1149.1 Test Access Port and Boundary-Scan Architecture*. The architecture includes all mandatory elements defined in the IEEE 1149.1 Standard. These elements include the Test Access Port (TAP), the TAP controller, the instruction register, the instruction decoder, the boundary-scan register, and the bypass register. The Virtex-II Pro family also supports some optional instructions; the 32-bit identification register, and a configuration register in full compliance with the standard.

JTAG Connection to XC2VP30

The JTAG connector initially connects to the System ACE CF controller, which passes the JTAG connections through to the XC2VP30 FPGA. Figure 2-6 is a block diagram showing the connections between the JTAG connector, System ACE CF controller, and the XC2VP30 FPGA. This diagram also shows the logic that allows the CPU JTAG header (J12) to be used to access the JTAG interface to program the XC2VP30.

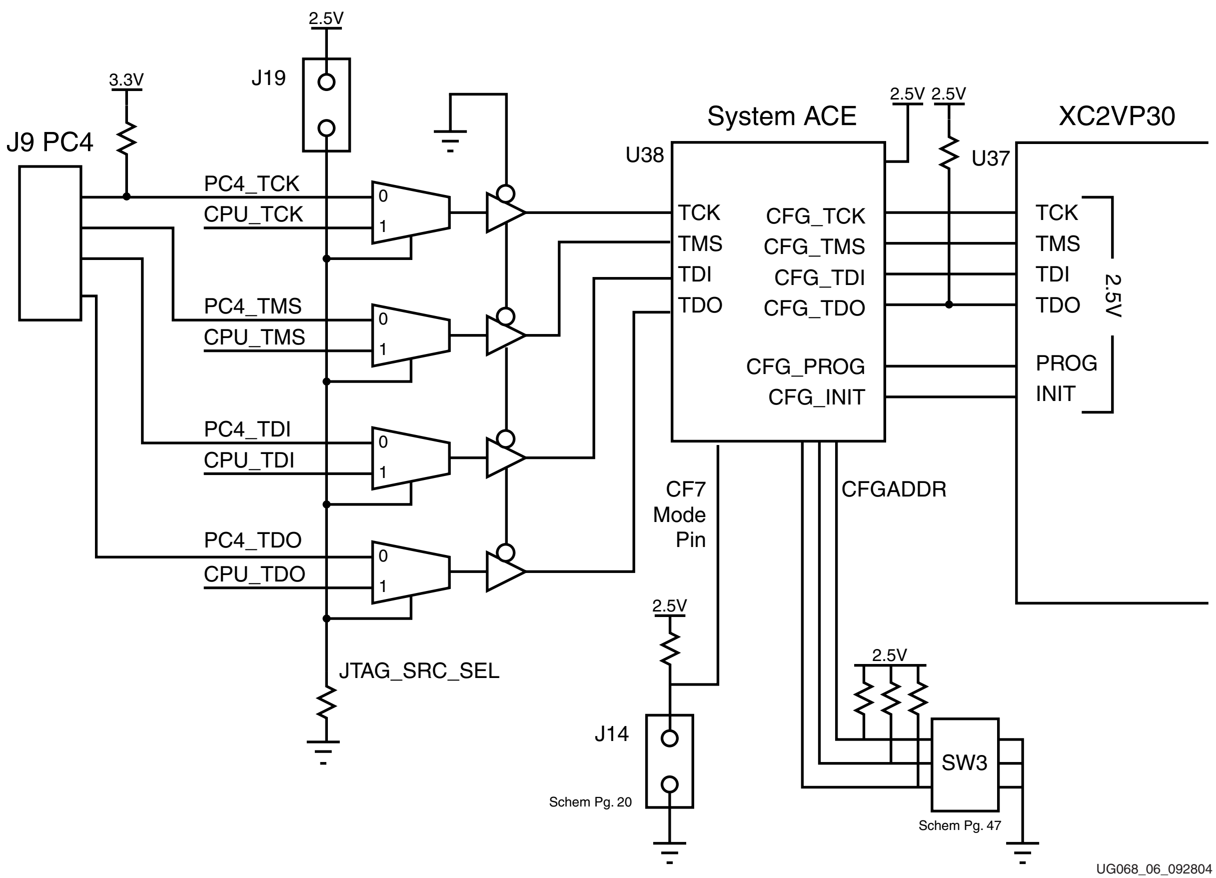

Figure 2-6: **JTAG Connections to the XC2VP30 and System ACE CF Controller**

Parallel Cable IV Interface

The Parallel Cable IV (PC4) download cable can also be used to program the XC2VP30. The pinout in Figure 2-7 is compatible with the PC4 JTAG programming solution.

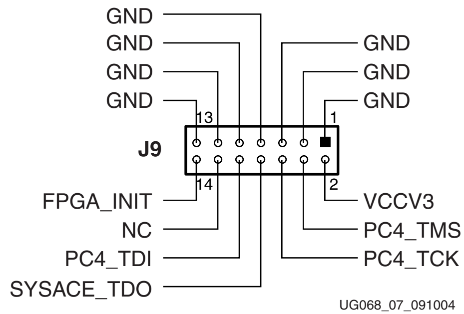

Figure 2-7: **PC4 JTAG Connector Pinout**

System ACE JTAG Configuration Interface

The JTAG configuration port on the System ACE CF controller is connected directly to the JTAG interface of the XC2VP30 FPGA, as shown in Table 2-6.

Table 2-6: **JTAG Connection from System ACE to XC2VP30**

Pin Name	System ACE (U38)	XC2VP30 (U37)
FPGA_TCK	80	G7
FPGA_TDO	81	F5
FPGA_TDI	82	F26
FPGA_TMS	85	H8

GPIO LEDs and LCD

GPIO

The ML310 Hardware Platform provides direct GPIO access to eight LEDs for general purpose use, and provides indirect access to a 16-pin connector (J13) that interfaces the ML310 to a 2-line by 16-character LCD display, AND491GST. A simple register interface handles access to the XC2VP30 GPIO signals.

The user also has indirect access to additional GPIO capability by way of the PCI bus through the GPIO header (J5) connected to the ALi M1535D+ South Bridge. See the "ALi South Bridge Interface, M1535D+ (U15)" section for more details on programming and controlling the ALi M1535D+ GPIO port.

Figure 2-8, page 29 shows the connectivity of the ML310 LEDs and LCD.

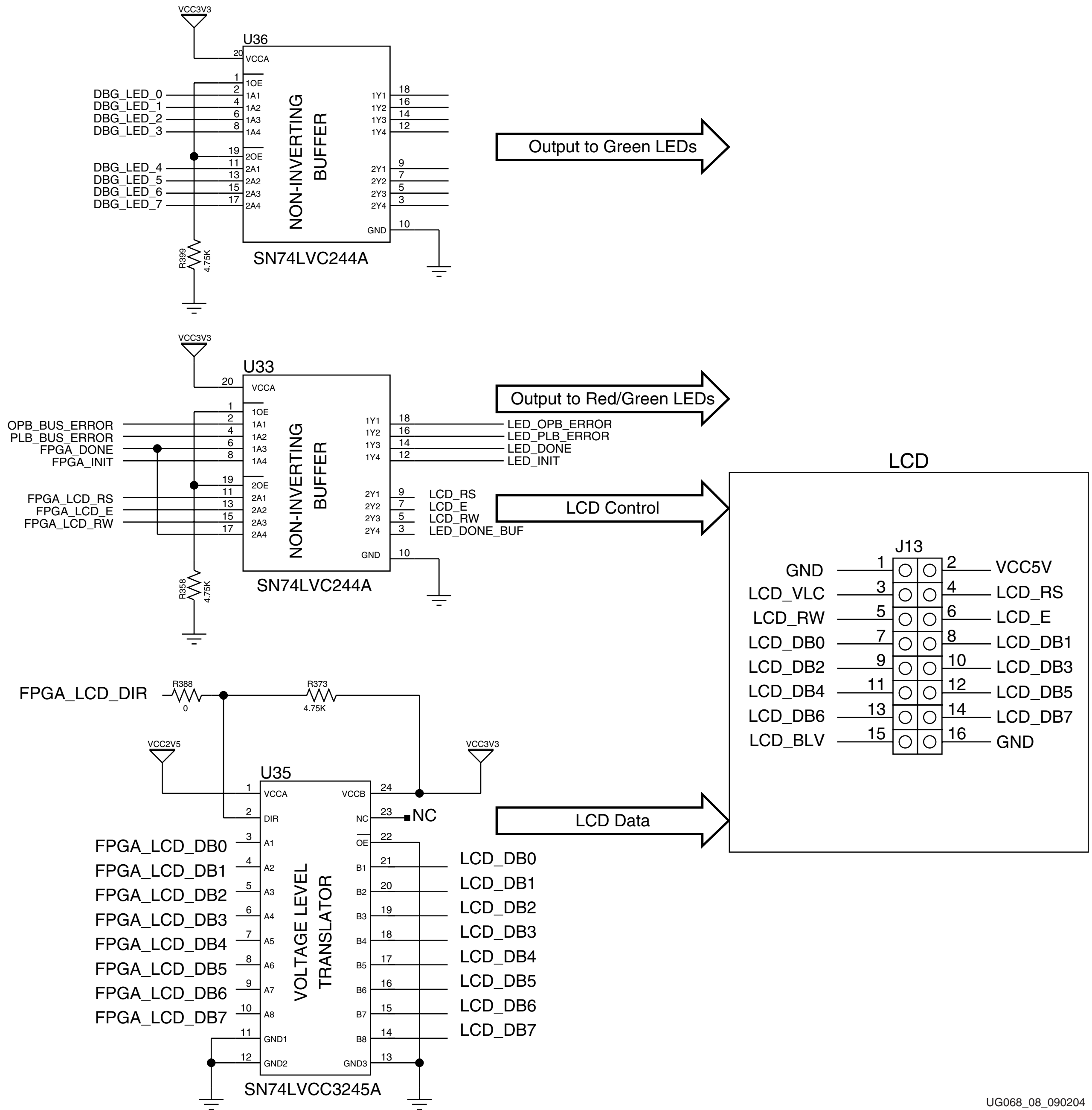

Figure 2-8: **LEDs and LCD Connectivity**

GPIO LED Interface

All LEDs connected to the GPIO lines illuminate green when driven with a logic 0 and extinguish with a logic 1. Table 2-7 shows the connections for the GPIO LEDs from the FPGA to the non-inverting buffer (U36).

Table 2-7: **GPIO LED Connection from FPGA to U36**

UCF Signal Name	XC2VP30 Pin (U37)	Schem Signal Name	LVC244 Buffer (U36)	LED
DBG_LED_0	H13	DBG_LED_0	2	DBG0
DBG_LED_1	G13	DBG_LED_1	4	DBG1
DBG_LED_2	C10	DBG_LED_2	6	DBG2
DBG_LED_3	C11	DBG_LED_3	8	DBG3
DBG_LED_4	J14	DBG_LED_4	11	DBG4
DBG_LED_5	H14	DBG_LED_5	13	DBG5
DBG_LED_6	E14	DBG_LED_6	15	DBG6
DBG_LED_7	D14	DBG_LED_7	17	DBG7

GPIO LCD Interface

The GPIO LCD interface has eight input/output signals used as data and three output-only signals used as control. The data signals are controlled by the logic level of the FPGA_LCD_DIR signal. A logic 1 on FPGA_LCD_DIR configures the LVCC3245 to drive the J13 header, while a logic 0 on FPGA_LCD_DIR configures the LVCC3245 to drive the XC2VP30 FPGA.

Table 2-8 shows the data bus signals on the GPIO LCD interface from the FPGA to U35.

Table 2-8: **GPIO LCD Data Signals from FPGA to U35**

UCF Signal Name	XC2VP30 Pin (U37)	Schem Signal Name	LVCC3245 Translator (U35)	LCD I/F (J13)
FPGA_LCD_DB0	F19	FPGA_LCD_DB0	3	7
FPGA_LCD_DB1	F20	FPGA_LCD_DB1	4	8
FPGA_LCD_DB2	F17	FPGA_LCD_DB2	5	9
FPGA_LCD_DB3	G17	FPGA_LCD_DB3	6	10
FPGA_LCD_DB4	B21	FPGA_LCD_DB4	7	11
FPGA_LCD_DB5	A21	FPGA_LCD_DB5	8	12
FPGA_LCD_DB6	G18	FPGA_LCD_DB6	9	13
FPGA_LCD_DB7	H18	FPGA_LCD_DB7	10	14
FPGA_LCD_DIR	C20	FPGA_LCD_DIR	2	-

The control signals allow the user to read/write the LCD character display in conjunction with the eight LCD data signals defined in Table 2-8. Please review the AND491GST LCD display data sheet located on the ML310 documentation CD for more detailed information.

Table 2-9 shows the control signal connections for the GPIO LCD from the FPGA to U33.

Table 2-9: **GPIO LCD Control Signals from FPGA to U33**

UCF Signal Name	XC2VP30 Pin (U37)	Schem Signal Name	LVC244 Buffer (U33)	LCD I/F (J13)
FPGA_LCD_E	C21	FPGA_LCD_E	13	6
FPGA_LCD_RS	J17	FPGA_LCD_RS	11	4
FPGA_LCD_RW	H17	FPGA_LCD_RW	15	5

CPU Debugging Interfaces

The ML310 board includes two optional CPU debugging interfaces; the combined FPGA JTAG/TRACE (P8) mictor connector and the CPU JTAG header (J12). These connectors can be used in conjunction with third party tools, or in some cases with the Xilinx Parallel Cable IV, to debug software as it runs on the processor. The PPC405 CPU core includes dedicated debug resources that support a variety of debug modes for debugging during hardware and software development. These debug resources include:

- Internal debug mode for use by ROM monitors and software debuggers
- External debug mode for use by JTAG debuggers
- Debug wait mode, which allows the servicing of interrupts while the processor appears to be stopped
- Real-time trace mode, which supports event triggering for real-time tracing

Debug modes and events are controlled using debug registers in the processor. The debug registers are accessed through either software running on the processor or through the JTAG port. The debug modes, events, controls, and interfaces provide a powerful combination of debug resources for hardware and software development tools. The JTAG port interface supports the attachment of external debug tools, such as the ChipScope™ Integrated Logic Analyzer, a tool providing logic analyzer capabilities for signals inside an FPGA, without the need for expensive external instrumentation. Using the JTAG test access port, a debug tool can single-step the processor and examine the internal processor state to facilitate software debugging. This capability complies with the *IEEE 1149.1 Standard* specification for vendor-specific extensions and is, therefore, compatible with standard JTAG hardware for boundary-scan system testing.

CPU Debug Description

External-debug mode can be used to alter normal program execution. It provides the ability to debug both system hardware and software. External-debug mode supports setting of multiple breakpoints, as well as monitoring processor status. Access to processor debugging resources can be made available through the CPU JTAG port (J12) providing the appropriate connections to the FPGA fabric are in place.

The PPC405 JTAG debug port in the FPGA complies with *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary Scan Architecture*. This standard describes a method for accessing internal chip resources using a four-signal or five-signal interface. The PPC405 JTAG Debug port supports scan-based board testing and is further enhanced to support the attachment of debug tools. These enhancements comply with the IEEE 1149.1 specifications for vendor-specific extensions and are compatible with standard JTAG hardware for boundary-scan system testing.

The PPC405 JTAG debug port supports the four required JTAG signals: TCK, TMS, TDI, and TDO. It also implements the optional TRST signal. The frequency of the JTAG clock signal can range from 0 MHz (DC) to one-half of the processor clock frequency. The JTAG debug port logic is reset at the same time the system is reset, using TRST. When TRST is asserted, the JTAG TAP controller returns to the test-logic reset state.

Refer to the *PowerPC 405 Processor Block Reference Guide* for more information on the JTAG debug port signals. Information on JTAG is found in the IEEE standard 1149.1-1990.

Figure 2-9 shows a 38-pin Mictor connector that combines the CPU Trace and the CPU Debug interfaces for high-speed, controlled-impedance signaling. For more information on starting and stopping the processor, single-stepping instruction execution on the trace-debug capabilities, how trace-debug works, and how to connect an external trace tool, see the *RISCWatch Debugger User's Guide*.

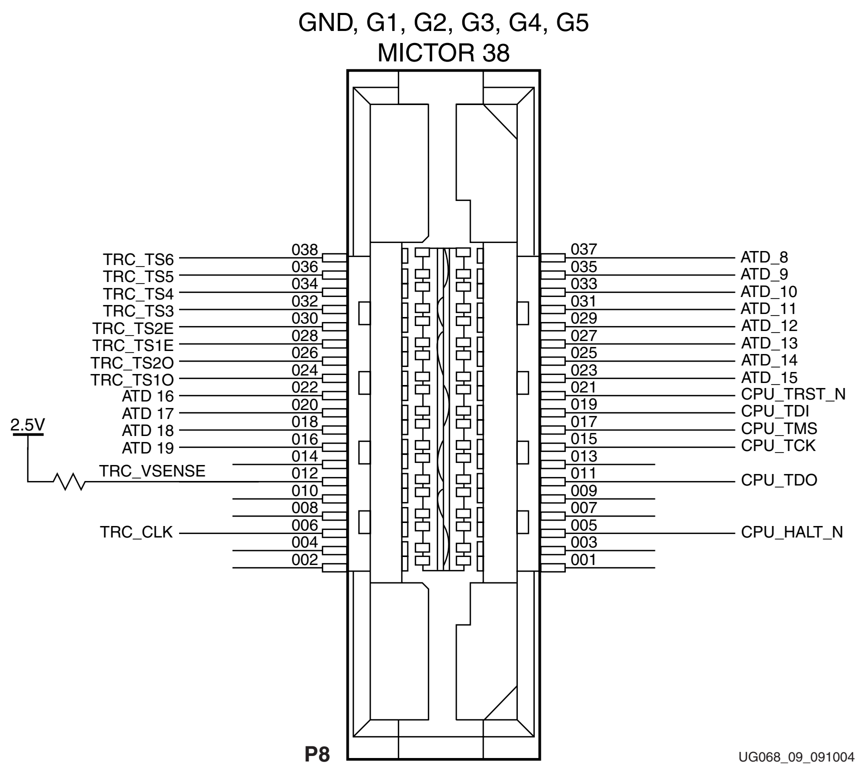

Figure 2-9: **Combined Trace/Debug Connector Pinout**

CPU JTAG Header Pinout

Figure 2-10 shows J12, the 16-pin header that can be used to debug the software operating in the CPU with debug tools such as Parallel Cable IV or third party tools. Refer to the *PowerPC 405 Processor Block Reference Guide* for more information on the JTAG debug port signals.

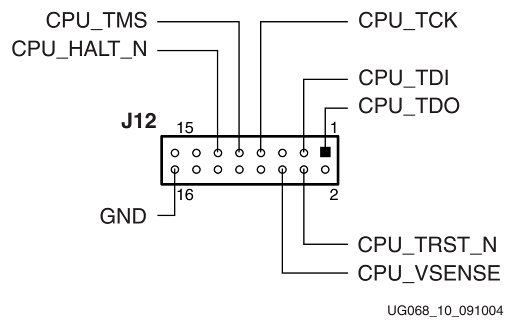

Figure 2-10: **CPU JTAG Header (J12)**

CPU JTAG Connection to XC2VP30

The connection between the CPU JTAG header (J12) and the XC2VP30 are shown in Table 2-10. These are attached to the PPC405 JTAG debug resources using normal FPGA routing resources. The JTAG debug resources are not hard-wired to particular pins, and are available for attachment in the FPGA fabric, making it possible to route these signals to whichever FPGA pins the user prefers.

Table 2-10: **CPU JTAG Connection to XC2VP30**

Pin Name	XC2VP30 Pin (U37)	Connector Pin (J12)
TDO	AH9	1
TDI	AJ9	3
TRST_N	AE12	4
TCK	AC13	7
TMS	AD13	9
HALT_N	AE11	11

PCI Bus

The ML310 board design provides the XC2VP30 access to two 33 MHz/32-bit PCI buses, a primary 3.3V PCI bus and a secondary 5.0V PCI bus. The FPGA is directly connected to the primary 3.3V PCI bus while the 5.0V PCI bus is connected to the primary PCI bus via a PCI-to-PCI bridge. There are several PCI devices available on the PCI buses as well as four PCI add-in card slots. All PCI bus signals driven by the XC2VP30 comply with the I/O requirements specified in the *PCI Local Bus Specification, Revision 2.2*.

The majority of the ML310 features are accessed over the 33 MHz/32-bit PCI bus. The Virtex-II Pro PPC405 processors can gain access to the primary PCI bus through the EDK PCI Host Bridge IP. All PCI configuration and control can be performed via a PCI Host Bridge implemented in the FPGA fabric. The primary PCI bus is wired so that the FPGA fabric must be used to provide PCI bus arbitration logic. EDK also provides PCI Arbiter IP.

Please see the EDK *Processor IP User Guide* for more information about the EDK IP mentioned in this section.

The FPGA is responsible generating the PCI RST signal as well as the PCI CLK signal. The FPGA fabric is used to generate six PCI clocks that drive each of the PCI devices/slots shown in the Figure 2-11, page 35. All six PCI clock outputs are length matched. Since the FPGA generates all PCI clocks, the downstream PCI devices have no clock input prior to or during FPGA configuration; therefore, PCI Reset should be deasserted after the PCI CLK has stabilized. Please review the *PCI Local Bus Specification, Revision 2.2* for more detailed information.

The onboard 33 MHz, 32-bit PCI bus is connected to three fixed PCI devices, listed below, that are part of the ML310 board.

- Texas Instruments, TI2250, PCI-to-PCI bridge
- Intel, GD82559, 10/100 PCI Ethernet NIC
- Ali, M1535D+, PCI South Bridge

These devices are described in the following sections as well in their data sheets on the ML310 documentation CD.

In addition to the three fixed PCI devices, there are four 33 MHz, 32-bit PCI slots available for use. For more information on the PCI slot pinouts, refer to the *PCI Local Bus Specification, Revision 2.2* and the ML310 schematics.

- Two 3.3V keyed PCI add-in card slots (P5 and P3)
- Two 5.0V keyed PCI add-in card slots (P6 and P4)

Figure 2-11, page 35 shows the connectivity of the PCI bus and PCI devices. For more information on the PCI slot pinouts, refer to the PCI 2.2 Specification or review the ML310 schematics.

Note: The 5.0V PCI slots differ from the 3.3V slots. See the *Important Instructions* sheet (PN 0402263) packaged with the ML310 kit before using Universal PCI add-in cards with the ML310 board.

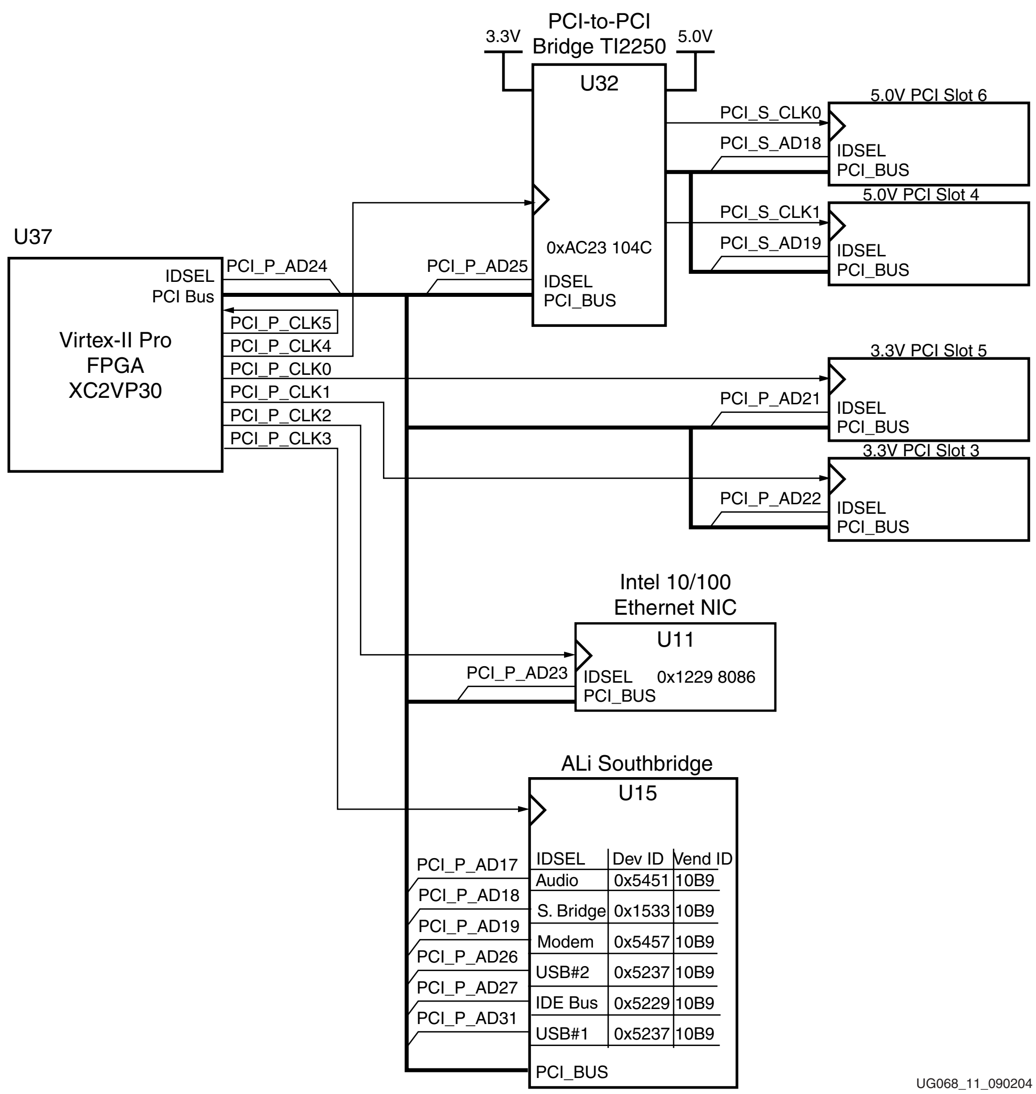

Figure 2-11: **PCI Bus and Device Connectivity**

Table 2-11 shows the connections for the PCI controller.

Table 2-11: **PCI Controller Connections**

UCF Signal Name	XC2VP30 (U37) Pin	Description
PCI_CLK0	T2	PCI_P_CLK0
PCI_CLK1	R2	PCI_P_CLK1
PCI_CLK2	R5	PCI_P_CLK2
PCI_CLK3	R6	PCI_P_CLK3
PCI_CLK4	R3	PCI_P_CLK4
PCI_CLK5	R4	PCI_P_CLK5
PCI_CLK5_FB	C15	PCI_P_CLK5

Table 2-11: **PCI Controller Connections *(Continued)***

UCF Signal Name	XC2VP30 (U37) Pin	Description
PCI_INTA	L5	PCI Interrupt Signals
PCI_INTB	N2	
PCI_INTC	M2	
PCI_INTD	R9	
PCI_INTE	P9	
PCI_INTF	M3	
PCI_REQ0_N	P1	PCI Request Signals
PCI_REQ1_N	N1	
PCI_REQ2_N	P7	
PCI_REQ3_N	P8	
PCI_REQ4_N	N3	
PCI_GNT0_N	P2	PCI Grant Signals
PCI_GNT1_N	P3	
PCI_GNT2_N	R7	
PCI_GNT3_N	R8	
PCI_GNT4_N	P4	
PCI_CBE[0]	J2	PCI Byte Enable Signals
PCI_CBE[1]	H2	
PCI_CBE[2]	M7	
PCI_CBE[3]	M8	
PCI_FRAME_N	K6	PCI Control Signals
PCI_IRDY_N	K1	
PCI_TRDY_N	J1	
PCI_STOP_N	M5	
PCI_DEVSEL_N	M6	
PCI_PERR_N	J3	
PCI_SERR_N	J4	
PCI_LOCK	L2	
PCI_IDSEL	K2	
PCI_REQ64_N*	F8	# PM_IO_3V_1
PCI_ACK64_N*	E8	# PM_IO_3V_2

Table 2-11: **PCI Controller Connections *(Continued)***

UCF Signal Name	XC2VP30 (U37) Pin	Description
PCI_AD[0]	G5	PCI Address/Data Lines
PCI_AD[1]	G6	
PCI_AD[2]	D5	
PCI_AD[3]	C5	
PCI_AD[4]	C1	
PCI_AD[5]	C2	
PCI_AD[6]	J7	
PCI_AD[7]	J8	
PCI_AD[8]	D3	
PCI_AD[9]	C4	
PCI_AD[10]	D1	
PCI_AD[11]	D2	
PCI_AD[12]	H5	
PCI_AD[13]	H6	
PCI_AD[14]	E3	
PCI_AD[15]	E4	
PCI_AD[16]	E1	
PCI_AD[17]	E2	
PCI_AD[18]	K7	
PCI_AD[19]	K8	
PCI_AD[20]	F3	
PCI_AD[21]	F4	
PCI_AD[22]	F1	
PCI_AD[23]	F2	
PCI_AD[24]	J5	
PCI_AD[25]	J6	
PCI_AD[26]	G3	
PCI_AD[27]	G4	
PCI_AD[28]	G1	
PCI_AD[29]	G2	
PCI_AD[30]	L7	
PCI_AD[31]	L8	
PCI_PAR	H3	PCI_P_PAR
PCI_RST_N	N8	PCI_P_RST_N

*** Note:**
These signals are connected, but are not required for 32 bit only PCI systems.

Table 2-12 shows how the primary PCI bus interrupts are connected on the ML310 board along with information for each device.

Table 2-12: **3.3V Primary PCI Bus Information**

Device Name	Dev. ID	Vend. ID	Bus	DEV	IDSEL	REQ	FPGA PCI CLK	PCI Device Interrupt	PCI Interrupts on FPGA A	B	C	D	ALI SBR
PCI Slot 5	N/A	N/A	0	5	AD21	0	0		A	B	C	D	-
PCI Slot 3	N/A	N/A	0	6	AD22	1	1		D	A	B	C	-
U11, Enet Mac	0x1229	0x8086	0	7	AD23	2	2		-	-	A	-	-
U15, ALI SB	0x1533	0x10B9	0	2	AD18	3	3		-	-	-	-	(INT, NMI)
U15, ALi Pwr Mgt	0x7101	0x10B9	0	12	AD28	3	3		-	-	-	-	(INT, NMI)
U15, ALI IDE	0x5229	0x10B9	0	11	AD27	3	3		-	-	-	-	(INT, NMI)
U15, ALi Audio	0x5451	0x10B9	0	1	AD17	3	3		-	-	-	-	(INT, NMI)
U15, Ali Modem	0x5457	0x10B9	0	3	AD19	3	3		-	-	-	-	(INT, NMI)
U15, ALi USB#1	0x5237	0x10B9	0	15	AD31	3	3		-	-	-	-	(INT, NMI)
U15, ALi USB#2	0x5237	0x10B9	0	10	AD26	3	3		-	-	-	-	(INT, NMI)
U32, PCI-PCI Brg	0xAC23	0x104C	0	9	AD25	4	4		-	-	-	-	-
U37, XC2VP30	0x0300	0x10EE	0	8	AD24	Int.	5		-	-	-	-	-

Notes:

The PCI ALi South Bridge device uses a separate interrupt line that connects to the FPGA via schematic net SBR_INTR. Anytime an interrupt occurs within the ALi South Bridge, it generates an interrupt on schematic net SBR_INTR.

Table 2-13 shows how the secondary PCI bus interrupts are connected on the ML310 board along with information for each device.

Table 2-13: **5.0V Secondary PCI Bus Information**

Device Name	Dev. ID	Vend. ID	Bus	DEV	IDSEL	REQ	Bridge CLK	PCI Dev. Intr.	PCI Interrupt on FPGA E	F
PCI Slot 6	N/A	N/A	1	2	AD18	0	0		A	B
PCI Slot 4	N/A	N/A	1	3	AD19	1	1		D	A
U32, PCI-PCI Brg	N/A	N/A	N/A	7	N/A	Int.	4		-	-

Notes:

1. PCI Slot 6 INTC connects to PCI Slot 4 INTB.
2. PCI Slot 6 INTD connects to PCI Slot 4 INTC.

ALi South Bridge Interface, M1535D+ (U15)

The ALi M1535D+ South Bridge Super I/O controller (Figure 2-12) augments the ML310 with many of the basic features found on legacy PCs. These basic PC features are only accessible over the PCI bus as this is the only way to access the ALI M1535D+. A brief description of the ALi M1535D+ features employed on the ML310 board follows. Please review the ALi M1535D+ data sheet located on the ML310 documentation CD for more detailed information.

ALi M1535D+ supports the following features:

- 1 parallel and 2 serial ports
- 2 USB ports
- 2 IDE connectors
- GPIO
- SMBus interface
- AC'97 audio codec
- PS/2 keyboard and mouse

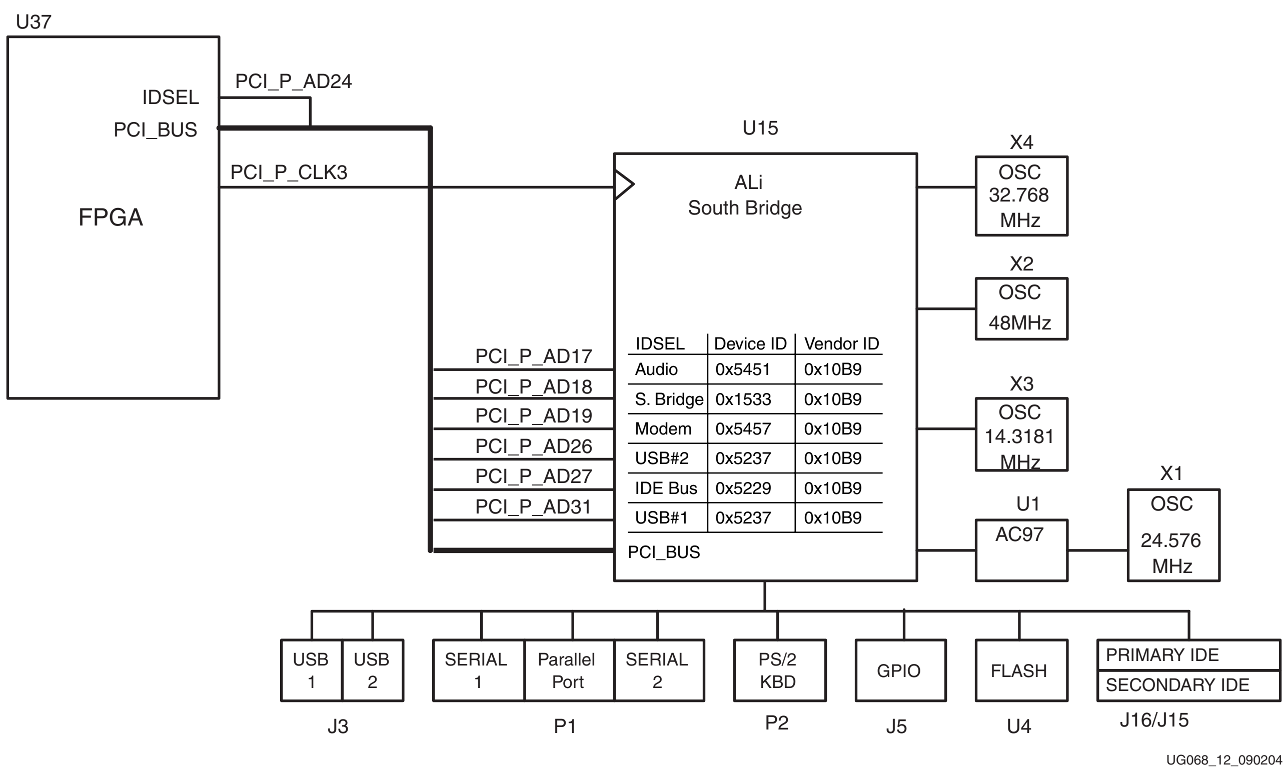

Figure 2-12: **ALi South Bridge Interface, M1535D+ (U15)**

Parallel Port Interface Connector Assembly (P1)

The parallel port interface of the ALi South Bridge is connected to a 25-pin connector, female DB25, which is part of the P1 connector assembly. The ALi M1535D+ supports various parallel port modes such as *standard parallel port* (SPP), *enhanced parallel port* (EPP), and IEEE 1284 compatible ECP. The P1, female DB25, connector pinout is configured as per *IEEE Std. 1284-1994*.

Table 2-14 shows the ALi parallel port connections to P1, DB25.

Table 2-14: **ALi South Bridge Parallel Port pinout P1 (DB25)**

Signal Name	P1 (DB25) Pin Number	Description
STROBE_N	1	Strobe
D0	2	Data Bit 0
D1	3	Data Bit 1
D2	4	Data Bit 2
D3	5	Data Bit 3
D4	6	Data Bit 4
D5	7	Data Bit 5
D6	8	Data Bit 6
D7	9	Data Bit 7
ACK_N	10	Acknowledge
BUSY	11	Busy
PEND	12	Paper End
SELECT	13	Select
AUTOFD_N	14	Autofeed
ERROR_N	15	Error
INIT_N	16	Initialize
SLCTIN_N	17	Select In
GND	18, 19, 20, 21, 22, 23, 24, 25	Ground

Serial Port Interface Connector Assembly (P1)

In addition to the serial port accessible through the XC2VP30 FPGA, the ALi M1535D+ provides access over the PCI bus to two serial ports. The ALi M1535D+ employs 16450/16550 compatible UARTs with send/receive 16-byte FIFOs. The two serial ports are connected to the ALi M1535D+ device with two male DB9 connectors (P1). The DB9 connectors are configured as DTE interfaces and meet the *EIA/TIA-574* standard.

The DB9 male connectors are labeled Serial Port A and B in the ML310 schematics. The DB9 connectors are part of the P1 connector assembly. Serial Port B is located adjacent to the PS/2 connector where COM1 in a legacy PC is traditionally located. The two DB9 serial port connectors are labeled on the ML310 board silkscreen near the P1 connector assembly.

Table 2-15 shows the RS-232 signals connected to the two DB9 connectors, P1 A/B.

Table 2-15: **ALi South Bridge DB9 Serial Port Pinouts (P1)**

Signal Name	P1 (DB9-A/B) Pin Number	Description
DCD	1	Data Carrier Detect
RD	2	Receive Data (a.k.a RxD, Rx)
TD	3	Transmit Data (a.k.a TxD, Tx)
DTR	4	Data Terminal Ready
SGND	5	Ground
DSR	6	Data Set Ready
RTS	7	Request To Send
CTS	8	Clear To Send
RI	9	Ring Indicator

USB Connector Assembly (J3)

The M1535D+ USB is an implementation of the *Universal Serial Bus Specification Version 1.0a* that contains two PCI Host Controllers and an integrated Root Hub. The two USB connectors, A/B, are part of the J3 connector assembly and are USB Type-A plugs.

Table 2-16 shows the ALi USB connections to the two USB Type-A plugs (J3).

Table 2-16: **ALi South Bridge USB Type-A Connector (J3)**

Signal Name	J3 (A/B) Pin Number	Description
USB_VCC	1	USB Power, 5.0V, MOSFET Isolated
USB_DN	2	USB Data -
USB_DP	3	USB Data +
GND	4	Ground

IDE Connectors (J15 and J16)

Supports a 2-channel UltraDMA-133 IDE master controller independently connected to a primary 40-pin IDE connector (J16) and a secondary 40-pin IDE connector (J15).

Table 2-17 shows the ALi Primary and Secondary IDE connections.

Table 2-17: **ALi South Bridge IDE Connectors (J15 and J16)**

J15/J16 Pin Number	Schem Signal	J15/J16 Pin Number	Schem Signal
1	IDE_RESET_N	2	GND
3	IDE_D7	4	IDE_D8
5	IDE_D6	6	IDE_D9
7	IDE_D5	8	IDE_D10
9	IDE_D4	10	IDE_D11
11	IDE_D3	12	IDE_D12
13	IDE_D2	14	IDE_D13
15	IDE_D1	16	IDE_D14
17	IDE_D0	18	IDE_D15
19	GND	20	(KEY)
21	IDE_DMARQ	22	GND
23	IDE_DIOW_N	24	GND
25	IDE_DIOR	26	GND
27	IDE_IORDY	28	CSEL
29	IDE_DMACK_N	30	GND
31	IDE_INTRQ	32	N.C.
33	IDE_A1	34	IDE_PDIAG_N
35	IDE_A0	36	IDE_A2
37	IDE_CS1_N	38	IDE_CS3_N
39	IDE_DASP_N	40	GND

GPIO Connector (J5)

There are 15 GPIO pins connecting the ALi M1535D+ to the 24-pin GPIO header (J5). These can be accessed through the ALi M1535D+ by way of the PCI bus.

Table 2-18 shows the types and number of GPIO signals available to the user from the ALi South Bridge.

Table 2-18: **Type of GPIO Available on Header J5**

ALi GPIO Types	Number Available
Output	5
Input	4
Input/Output	6

Table 2-19 shows the connections from the ALi, M1535D+, GPIO signals available at the GPIO header (J5).

Table 2-19: **GPIO Connections on Header J5**

Schem Net Name	GPIO Header (J5)	M1535D+ (U15)	I/O Type
GPO_35	24	P19	Output
GPO_34	22	P18	Output
GPO_30	20	N18	Output
GPO_29	23	N17	Output
GPO_10	21	T3	Output
GPI_36	7	U8	Input
GPI_34	5	W7	Input
GPI_25	3	E9	Input
GPI_24	1	M17	Input
GPIO_3	15	Y4	Input/Output
GPIO_23	19	U5	Input/Output
GPIO_22	17	U6	Input/Output
GPIO_2	13	W4	Input/Output
GPIO_1	11	V4	Input/Output
GPIO_0	9	Y3	Input/Output

System Management Bus Controller

The SMBus host controller in the M1535D+ supports the ability to communicate with power related devices using the SMBus protocol. It provides quick send byte/receive byte/ write byte/write word/read word/block read/block write command with clock synchronization function as well as 10-bit addressing ability. Please see the "IIC/SMBus Interface" section for more information regarding the devices that are connected to the SMBus.

AC'97 Audio Interface

The ALi South Bridge Super I/O controller has a built-in audio interface that is combined with a standard audio codec (AC'97), LM4550. Features available to the user are as follows:

- AC'97 Codec 2.1 Specification compliant
- Codec variable sample rate support
- 32-voice hardware wave-table synthesis
- 32 independent DMA channels
- 3D positioning sound acceleration
- Legacy Sound Blaster compatible
- FM OPL3 emulation
- MIDI interpretation
- MIDI MPU-401 interface

The ML310 employs a National Semiconductor, LM4550, audio codec combined with the ALi South Bridge AC'97 interface. This interface can be used to play and record audio. The LM4550 has left and right channel line inputs, a microphone input, left and right channel line outputs, and an amplified headphone output suitable for driving an 8Ω load using the LM4880 (U2). The audio jacks are available on the J1 and J2 connector assemblies.

Table 2-20 describes the audio jacks available to the user on the ML310.

Table 2-20: **Audio Jacks (J1 and J2)**

Audio Jack	Signal name	Description
J1 top	AC _AMP_OUTR AC _AMP_OUTL	AC Amplified Output, right and left channels, driven by U2, LM4880
J1 Bottom	AC_MIC_IN	Microphone Input to U1, LM4550
J2 Top	AC _LINE_OUTRAC _LINE_OUTL	AC Line Output, right and left channels, driven by U1, LM4550
J2 Bottom	AC _LINE_INR AC_LINE_INL	AC Line Input, right and left channels, driven by U1, LM4550

PS/2 Keyboard and Mouse Interface Connector (P2)

The ALi M1535D+ has a built-in PS2/AT keyboard and PS/2 mouse controller. The PS/2 keyboard and mouse ports are connected to the ALi M1535D+ through standard DIN connectors contained in the P2 connector assembly. In the event of a short circuit by the keyboard or mouse device, the 5V power provided to these devices is protected by a resettable fuse, F1.

Table 2-21 shows the PS/2 keyboard and mouse connections to the P2 connector assembly.

Table 2-21: **PS/2 Keyboard and Mouse**

Signal Name	Connector (P2)	Description
KDAT	1	Keyboard Data
KCLK	5	Keyboard Clock
MDAT	7	Mouse Data
MCLK	11	Mouse Clock
KVCC, MVCC	4, 10	Fuse protected power to Keyboard and Mouse

Flash ROM (U4)

The ALi South Bridge supports 4 Mb Flash memory interface. The ML310 provides connectivity to an AM29F040B 4 MB (512 K x 8 bit) flash memory (U4) via the ALi M1535D+ ROM interface.

Table 2-22 shows the connections between the ALi M1535D+ (U15) ROM signals to the AM29F040B (U4) flash memory device.

Table 2-22: **ALi M1535D+ Flash Memory Interface**

Schem Net Name	M1535D+ (U15)	AM29F040B (U4)	Description
ROM_WE_N	U14	7	Active-Low Write Enable
ROM_OE_N	T14	32	Active-Low Output Enable
ROM_D7	W19	29	Flash Data
ROM_D6	Y19	28	
ROM_D5	V20	27	
ROM_D4	W20	26	
ROM_D3	Y20	25	
ROM_D2	U18	23	
ROM_D1	U19	22	
ROM_D0	U20	21	

Table 2-22: **ALi M1535D+ Flash Memory Interface *(Continued)***

Schem Net Name	M1535D+ (U15)	AM29F040B (U4)	Description
ROM_A18	T15	9	Flash Addresses
ROM_A17	U15	6	
ROM_A16	V15	10	
ROM_A15	W15	11	
ROM_A14	T16	5	
ROM_A13	U16	4	
ROM_A12	V16	12	
ROM_A11	W16	1	
ROM_A10	Y16	31	
ROM_A9	R17	2	
ROM_A8	T17	3	
ROM_A7	U17	13	
ROM_A6	V17	14	
ROM_A5	W17	15	
ROM_A4	Y17	16	
ROM_A3	V18	17	
ROM_A2	W18	18	
ROM_A1	Y18	19	
ROM_A0	V19	20	

Intel 10/100 Ethernet Controller, GD82559 (U11)

The GD82559 10/100 Mb/s Fast Ethernet controller (Figure 2-13, page 47) with an integrated 10/100 Mb/s physical layer device for PCI board LAN designs is designed for use in network interface cards, PC LAN On Motherboard (LOM) designs, embedded systems, and networking system products. It consists of both the Media Access Controller (MAC) and the physical layer (PHY) interface combined into a single component solution. The GD82559 can operate in either full-duplex or half-duplex mode. The GD82559 also includes an interface to a serial (4-pin) EEPROM and a parallel interface to a 128 kB flash memory. The EEPROM provides power-on initialization for hardware and software configuration parameters.

The ML310 board utilizes the GD82559 10/100 Ethernet capability via FPGA PCI host bridge accesses over the PCI bus. The GD82559 is only accessible over the PCI bus, this includes programming of its power-on initialization EEPROM. The GD82559's EEPROM is pre-programmed on each ML310 with a unique MAC address. The ML310 MAC address is identified by the mylar label near the RJ-45 connector labeled "ETH0 MAC ADDR." Please review the GD82559 data sheet, located on the ML310 documentation CD, for more detailed information.

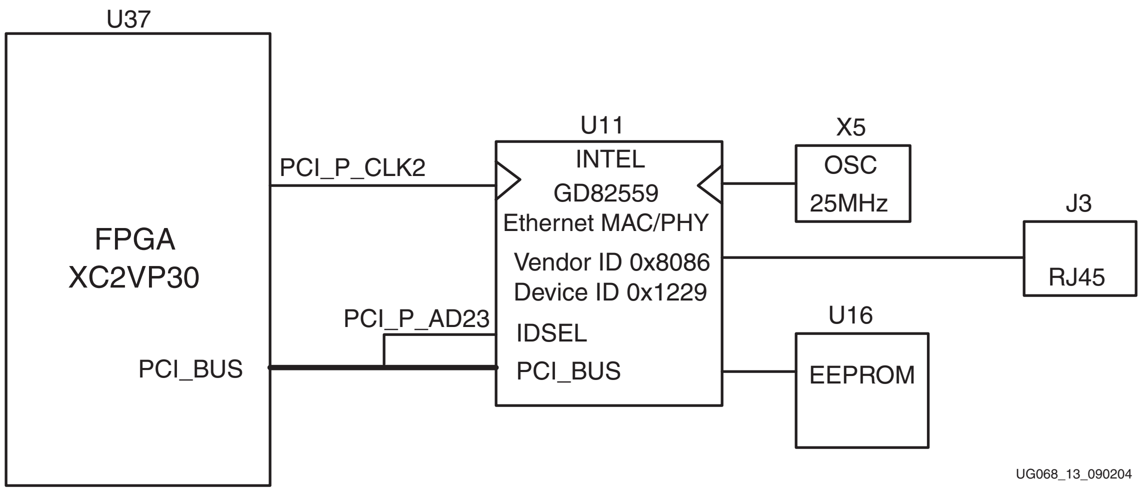

Figure 2-13: **Intel GD82559 Ethernet Controller**

IIC/SMBus Interface

Introduction to IIC/SMBus

The Inter Integrated Circuit (IIC) bus provides the connection from the CPU to peripherals. It is a serial bus with a data signal, SDA, and a clock signal, SCL, both of which are bidirectional. The IIC/SMBus interface serves as an interface to one master device and multiple slave devices. The interface operates in the range of 100 kHz to 400 kHz.

The SMBus also provides connectivity from the CPU to peripherals. The SMBus is also a two wire serial bus through which simple power related devices can communicate with the rest of the system. SMBus uses IIC as its backbone. EDK provides IP that integrates the IIC interface with a microprocessor system. See the EDK *Processor IP User Guide* for more details.

IIC/SMBus Signaling

The IIC bus data and clock signals operate as open-drain. By default, these signals are pulled high to 5V, although some devices support lower voltages. Either the master device or a slave device can drive either of the signals low to transmit data or clock signals.

IIC/SMBus on ML310 Board

Table 2-23 lists the function, part number, and addresses of the IIC devices on the ML310. These devices include EEPROM, temperature sensors, power monitors, and a Real Time Clock.

Table 2-23 shows the FPGA connections to all IIC and SMBus devices.

Table 2-23: **IIC and SMBus Controller Connections**

UCF Signal Name	XC2VP30 Pin (U37)	Schem Signal Name
iic_scl	C13	fpga_scl
iic_sda	J15	fpga_sda
iic_irq_n	E15	iic_irq_n
iic_temp_crit_n*	D15	iic_therm_n

* **Note:** This signal connects to U20 therm_l on the LM87. See data sheet for additional details.

Figure 2-14 shows a block diagram of the FPGA in relation to the SMBus accelerator and the IIC bus.

Note: Either the XC2VP30 or the ALi M1535D+ can master the IIC bus, but not simultaneously.

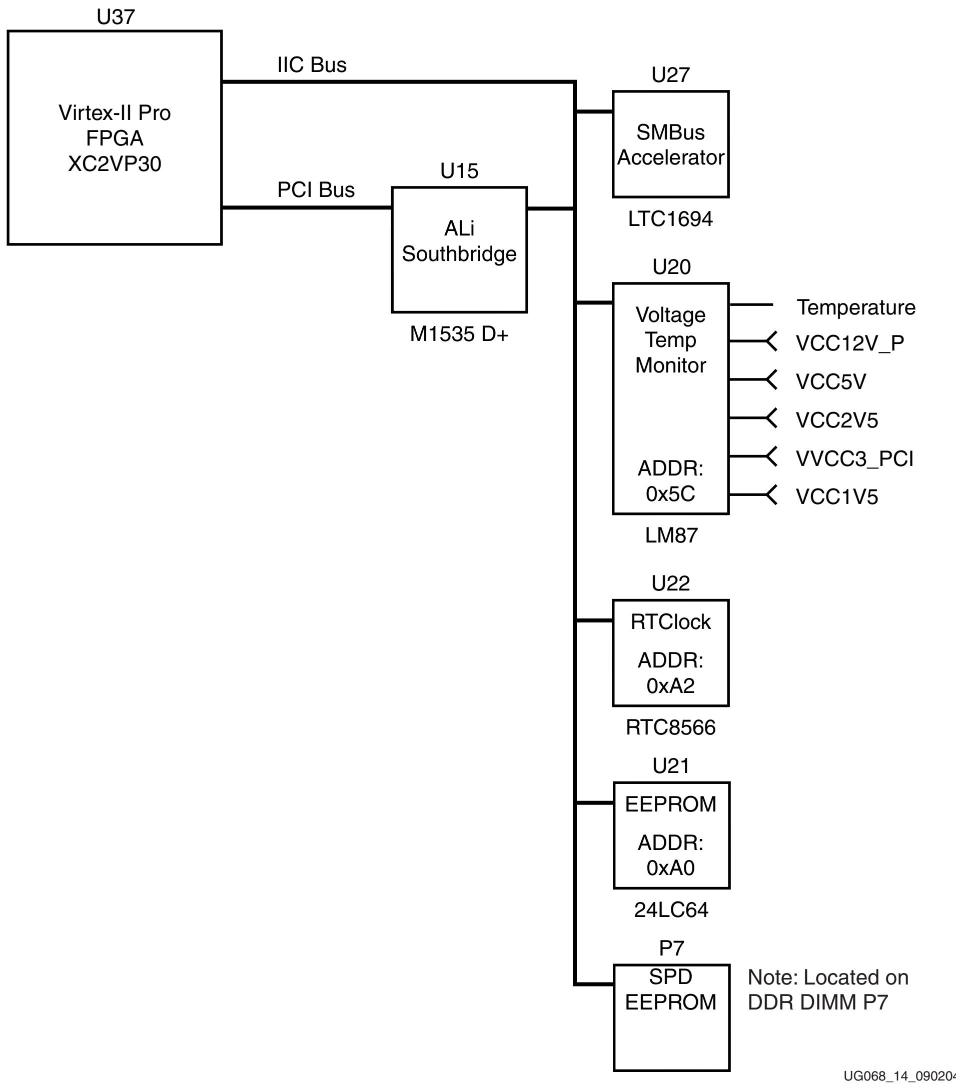

Figure 2-14: **IIC and SMBus Block Diagram**

Table 2-24 lists the IIC devices and their associated addresses.

Table 2-24: **IIC Devices and Addresses**

Device	Reference Designator	Address	Description
LTC1694	U27	N/A	SMBus accelerator that ensures data integrity with multiple devices on the SMBus. Enhances data transmission speed and reliability under all specified SMBus loading conditions and is compatible with the IIC bus.
RTC8564	U22	0xA2	IIC bus interface Real Time Clock module along with an external rechargeable battery and charging circuit.
24LC64	U21	0xA0	EEPROM is a 64 kb electrically erasable PROM.
LM87	U20	0x5C	Voltage/Temperature monitor

Note: The IIC bus can be controlled directly by the FPGA or indirectly by the ALi bridge over the FPGA PCI interface.

Serial Peripheral Interface

Serial Peripheral Interface™ (SPI), is a serial interface much like the IIC bus interface. There are three primary differences; the SPI operates at a higher speed, there are separate transmit and receive data lines, and the device access is chip-select based instead of address based. EDK provides IP that integrates the SPI interface with a microprocessor system. See the EDK *Processor IP User Guide* and the data sheet available on the ML310 documentation CD for more details.

SPI Signaling

There are four main signals used in the SPI interface; Clock, Data In, Data Out, and Chip Select. Signaling rates on the SPI bus range from 1 MHz to 3 MHz, roughly a factor of 10 faster than the IIC bus interface. SPI continues to differ from IIC using active drivers for driving the signal high and low, while IIC only actively drives signals low, relying on pull-up resistors to pull the signals high.

There are four basic signals on the SPI bus:

- **Master Out Slave In (MOSI):** A data line that supplies the output data from the master device that is shifted into a slave device
- **Master In Slave Out (MISO):** A data line that supplies the output data from a slave device that is shifted into the master device
- **Serial Clock (SCK):** A control line driven by the master device to regulate the flow of data and enable a master to transmit data at a variety of baud rates
    - The SCK line must cycle once for each data bit that is transmitted
- **Slave Select (SS):** A control line to dedicated to a specific slave device that allows the master device to turn the slave device on and off

SPI Addressing

The SPI does not use an addressed-based system like the IIC bus interface uses. Instead, devices are selected by dedicated Slave Select signals, comparable to a Chip Select signal. Each SPI slave device needs its own Slave Select signal driven from the SPI master. This increases the total pin count, but decreases overhead and complexity, which increases the available bandwidth and decreases bus contention.

The ML310 employs a single SPI device which is a 25LC640, 64 kb EEPROM.

Figure 2-15 shows the FPGA and the EEPROM connected by the SPI bus.

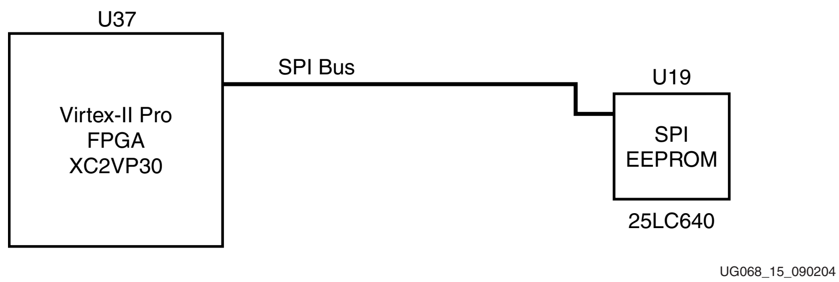

Figure 2-15: **SPI EEPROM Device Interface**

Table 2-25 shows the connections between the IIC/SMBus controller and the FPGA.

Table 2-25: **IIC and SMBus Controller Connections**

UCF Signal Name	XC2VP30 Pin (U37)	Schem Signal Name
spi_miso	AJ10	SPI_DATA_OUT
spi_mosi	AK10	SPI_DATA_IN
spi_sck	AF12	SPI_CLK
spi_ss[0]	AF13	SPI_DATA_CS_N

Pushbuttons, Switches, Front Panel Interface, and Jumpers

Pushbuttons

System ACE Reset Switch (SW1)

SW1 is a manual reset switch for the System ACE CF (U38) device. When SW1 is actuated it drives the PB_SYSTEM_ACE_RESET signal low, which causes the LTC1326 (U31) to generate a 100 µs active-Low pulse. The active-Low output from the LTC1326 drives the reset input of the System ACE CF controller (U38) through the SYSTEMACE_RESET_N signal. When the System ACE CF device is reset, it causes a reconfiguration of the XC2VP30 FPGA. The ACE file used to program the device is selected via SW3 DIP switch settings.

The front panel interface header (J23) can also drive the PB_SYSTEM_ACE_RESET signal. For more details on J23, see the "Front Panel Interface Connector (J23)" section.

CPU Reset Switch (SW2)

SW2 is an manual reset switch for the PPC405 system implemented in the XC2VP30. To use this switch, the user must connect the PB_FPGA_CPU_RESET signal to the PPC405 system within the FPGA fabric. EDK provides IP to perform this task. See the EDK *Processor IP User Guide* for more details.

Provided the user has connected SW2 in the FPGA fabric, when actuated it drives the PB_FPGA_CPU_RESET signal low, causing the LTC1326 (U30) to generate a 100 µs active-Low pulse. The active-Low output of the LTC1326 pin drives the FPGA_CPU_RESET_N signal connected to E16 on the XC2VP30 (U37) FPGA.

In addition to resetting the CPU, SW2 can also perform a System ACE CF reset as described in "System ACE Reset Switch (SW1)," page 51. This can be accomplished by simply holding down the SW2 push button for longer than two seconds. This action performs a CPU reset followed by a System ACE CF reset. Please review the ML310 schematics and the LTC1236 data sheet on the ML310 documentation CD for more details.

The front panel interface header (J23) can also drive the PB_ FPGA_CPU_RESET signal. For more details on J23, please review the "Front Panel Interface Connector (J23)" section.

System ACE Configuration DIP Switch (SW3)

SW3 is a three position dual-inline package (DIP) switch that controls the three configuration address pins on the System ACE CF controller. The addresses, CFGADDR0, CFGADDR1, and CFGADDR2, are marked on SW3 as positions 1, 2, and 3 respectively. SW3 also has an "on" indicator and directional arrow etched onto the plastic housing. An arrow appears on the board silkscreen, as well, to indicate the on position. When any of the three switches are moved to the on position, the associated CFGADDR bit is set to a logic 0. When any of the three switches are moved opposite of the on position (i.e., off), the associated CFGADDR bit is set to a logic 1 via a pull-up resistor.

Figure 2-16, page 53 shows the SW3 DIP switch connections to the System ACE device. One side of the DIP switch is tied to pull-up resistors that are connected to each of the CFGADDR lines while the other side of the DIP switch is connected to ground. The configuration address lines are also connected to the front panel interface. See the "Front Panel Interface Connector (J23)" section for more details. This allows the user to manually select one of eight configurations stored on the CompactFlash card that is connected to the System ACE device. Once the user makes a valid selection on SW3, the user can then depress push button SW1 to command the System ACE device to reset and configure the FPGA using the configuration selected by DIP switch SW3. See the System ACE CF data sheet for more details.

SW3 = 0 0 0 (default)

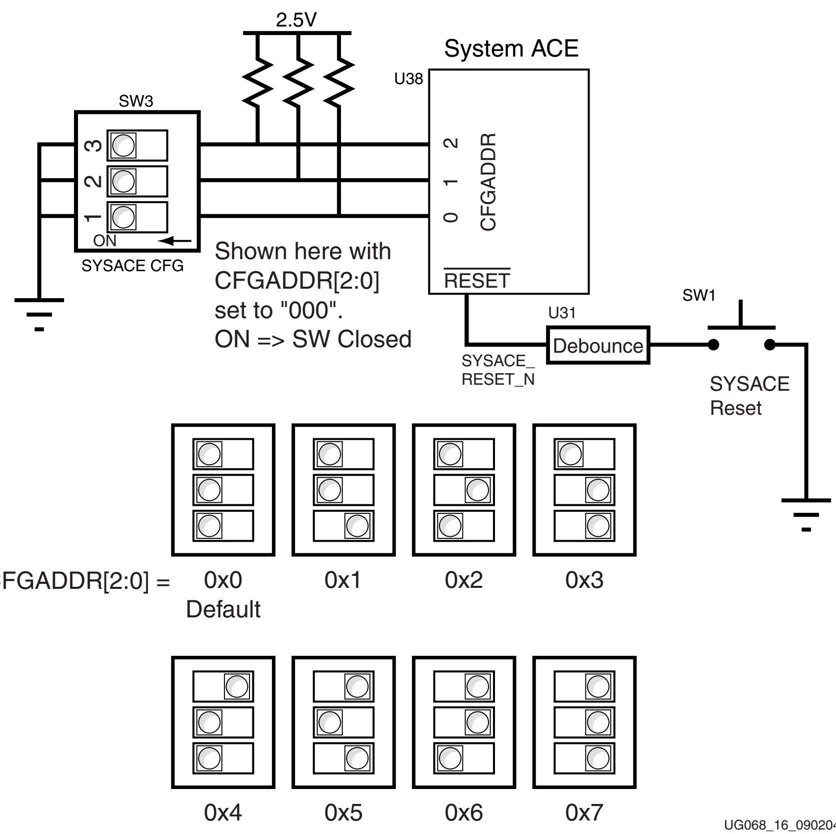

Figure 2-16: **SW3 - SysACE CFG Switch Detail**

Front Panel Interface Connector (J23)

The front panel interface connector (J23) is a 24-pin header that accepts a standard IDC 24 pin connector (0.1 inch pitch). J23 provides an optional means to control and gather status information from the ML310 board if it were to be enclosed similar to that of a desktop PC. The functionality listed below can easily be connected with a custom user-provided cable that connects to user logic designed to control and monitor the functionality available through the front panel interface.

The front panel interface provides the following control capability:

- Power on | off the ML310
  - ML310 board is delivered with a jumper installed on J23
- Eight System ACE configuration selections
  - Connects to the three System ACE configuration address lines
- System ACE Reset
  - Active-Low input (pulsed)
- CPU Reset
  - Active-Low input (pulsed)

The front panel interface provides access to the following status information:

- FPGA configuration DONE output
- IDE disk access output
- ATX power output
- Two FPGA user-defined output signals
- ATX speaker output
- Keyboard inhibit input (active-Low)

Note: All front panel interface outputs, except for the speaker out, can drive LEDs.

Table 2-26 shows the signals available at the front panel interface header (J23).

Table 2-26: **Front Panel Interface Connector (J23)**

J23 Pin	Schem Signal	Description
1	SYACE_CFGA0	Used to select System ACE configuration, CFGADDR0
2	FPGA_USER_LED1	User Defined function, Connects to XC2VP30, U37-AH10, (2.5V bank)
3	SYACE_CFGA1	Used to select System ACE configuration, CFGADDR1
4	FPGA_USER_LED2	User Defined function, Connects to XC2VP30, U37-AC14, (2.5V bank)
5	SYACE_CFGA2	Used to select System ACE configuration, CFGADDR2
6	NC	No Connect
7	LED_DONE_R	Remote FPGA DONE indicator, Tie this pin to Anode of user's LED and Cathode to ground
8	GND	Ground
9	ATX_PWRLED	ATX 3.3V power indicator, Tie this pin to Anode of user's LED and Cathode to ground
10	ATX_SPKR	Used to drive user-provided ATX speaker
11	NC	No Connect
12	NC	No Connect
13	GND	Ground
14	GND	Ground
15	KBINH	Tie this pin to ground to activate Keyboard Inhibit (See ALi M1536D+ data sheet for more details)
16	VCC5V	5V ATX power available to user
17	ATX_IDELED_R	ATX IDE access indicator; Tie this pin to Anode of user's LED and Cathode to ground
18	VCC5V	5V ATX power available to user
19	PWR_SUPPLY_ON	The default factory settings have this pin jumpered to ground to enable the ATX power supply (This pin cannot be controlled by a momentary pulse)

Table 2-26: **Front Panel Interface Connector (J23) *(Continued)***

J23 Pin	Schem Signal	Description
20	GND	Ground
21	PB_SYSACE_RESET	Used to reset System ACE when driven low, as described in "System ACE Reset Switch (SW1)"
22	GND	Ground
23	PB_FPGA_CPU_RESET	Used to reset CPU when driven low, as described in "CPU Reset Switch (SW2)"
24	GND	Ground

Jumper Headers

MGT VTRX Termination Voltage Selection Headers (J10 and J11)

The MGT receive termination voltage, VTRX, on the top and bottom MGTs are selectable through headers J10 (top) and J11 (bottom). The onboard regulated VTRX termination voltage can be configured for AC or DC coupling, 1.8V or 2.5V respectively.

Table 2-27 shows the MGT VTRX voltage selections available on the ML310 board.

Table 2-27: **Jumper Selection for Top and Bottom MGT VTRX Voltages (J10/ J11)**

MGTs	VTRX	Voltage	Jumper (J10)	Jumper (J11)	MGT RX Coupling
All Top	MGT_VTT	1.8V	Shunt 2 - 3	Open	AC
	MGT_AVCC	2.5V	Shunt 1 - 2	Open	DC
All Bottom	MGT_VTT	1.8V	Open	Shunt 2 - 3	AC
	MGT_AVCC	2.5V	Open	Shunt 1- 2	DC
All	MGT_VTT	1.8V	Open	Open	Default
	MGT_AVCC	2.5V	Open	Open	Default

MGT BREF Clock Selection Jumpers (J20 and J21)

One of two onboard LVDS clock sources, X7 or X9, can be selected via jumpers (J20 and J21). The selected LVDS clock source drives both top and bottom BREF Clock input pairs to the XC2VP30 FPGA.

Table 2-28 shows the MGT BREF clock selections available on the ML310 board.

Table 2-28: **Jumper Selection for MGT BREF Clocks (J20/J21)**

BREF Clock Freq.	Jumper (J10)	Jumper (J11)	Description
156.25 MHz	Shunt 1 - 2	Shunt 1 - 2	LVDS oscillator, X7, 156.25 MHz
125.00 MHz	Shunt 2 - 3	Shunt 2 - 3	LVDS oscillator, X9, 125.00 MHz

Notes:

BREF clock pins driven on the XC2VP30 FPGA are:
LVDS_CLKLOC_P (U37-F16/AH16)
LVDS_CLKLOC_N (U37-G16/AJ16)

System ACE Configuration Mode Header (J14)

Selects the System ACE configuration mode behavior after reset or power up.

J14 = Open (default)

- Allows System ACE CF to configure immediately after reset or power up

J14 = Shorted

- Inhibits the System ACE from configuring after reset or power up and can only be commanded by the MPU control to do so.

Note: See "System ACE CF Controller" and the System ACE CF data sheet for more details on the System ACE device operation.

JTAG Source Select Header (J19)

The JTAG source select jumper (J19) enables the use of either the PC4 JTAG connector (J9) or the CPU JTAG (J12) and FPGA JTAG/TRACE (P8) to source the XC2VP30 JTAG pins. This is available for third party tool support. The multiplexing is performed by an external device, 74LVC157A (U39), as shown earlier in Figure 2-6.

Note: This functionality should not be used if the user implements logic that also drives the CPU JTAG connector (J12) or the FPGA JTAG/TRACE connector (P8) as contention may result after the FPGA is configured.

J19 = Open (default, use the J9 PC4 JTAG connector)

ATX Power Distribution and Voltage Regulation

The ML310 board is shipped with a commercially available 250W ATX power supply. All voltages required by the ML310 logic devices are derived from the 5.0V supply, except the +/- 12V supplies, as shown in Figure 2-17. The ML310 ATX power supply can be easily mounted in a standard ATX chassis along with the ML310 board.

An Antec, model SL250S, ATX power supply is delivered with your ML310. The *Antec User's Manual* is provided in the data sheets section on the ML310 documentation CD. Prior to installation, please read the Installation section of the *Antec User's Manual* which describes the red power supply voltage switch setting on your Antec SL250S supply.

> ***Caution!*** Check the red power supply voltage switch setting before installation. It should be the same as your local power voltage (115V for North America, Japan, etc. and 230V for most European countries). Change the voltage setting if necessary. Failure to take this precaution could result in damage to your equipment and could void your warranty.

The different logic devices used on the ML310 board require a variety of voltages. Voltage levels are derived from the 5.0V supply and regulated on the board as shown in Figure 2-17.

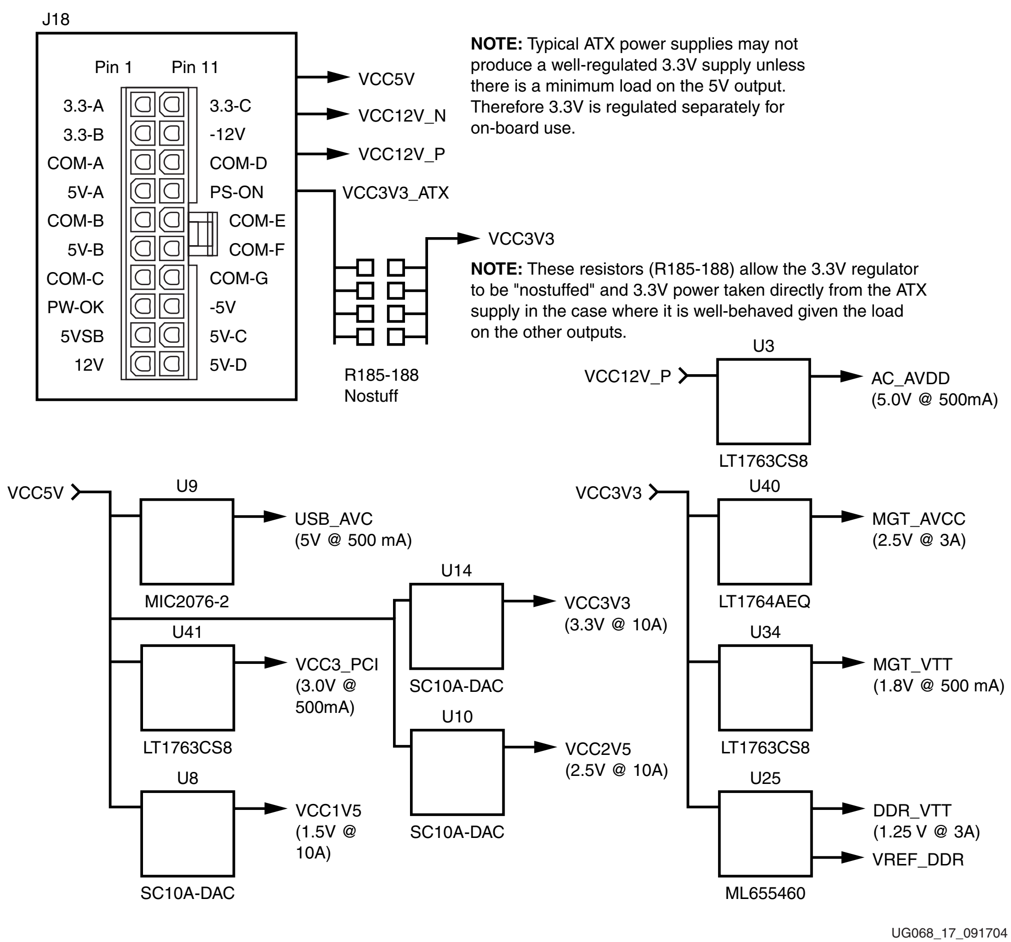

Figure 2-17: **ATX Power Distribution and Voltage Regulation**

Several voltage monitors, MC34161D, monitor all regulated power on the ML310 board. Each voltage monitor connects to power indicator LEDs as shown in Figure 2-18. The indicator LEDs illuminate red if a regulated supply voltage is out of spec, and illuminate green if the regulated supply voltage is nominal. Each regulated supply voltage has a corresponding test point located near its indicator LED. Please review the ML310 schematics and the MC34161D data sheet for more detailed information.

In addition to the MC34161D voltage monitors, the ML310 employs a SMBus device, LM87, which samples several of the same supply voltages when accessed over the System Management Bus. For more information on the SMBus features of the ML310, see the "IIC/SMBus Interface" section.

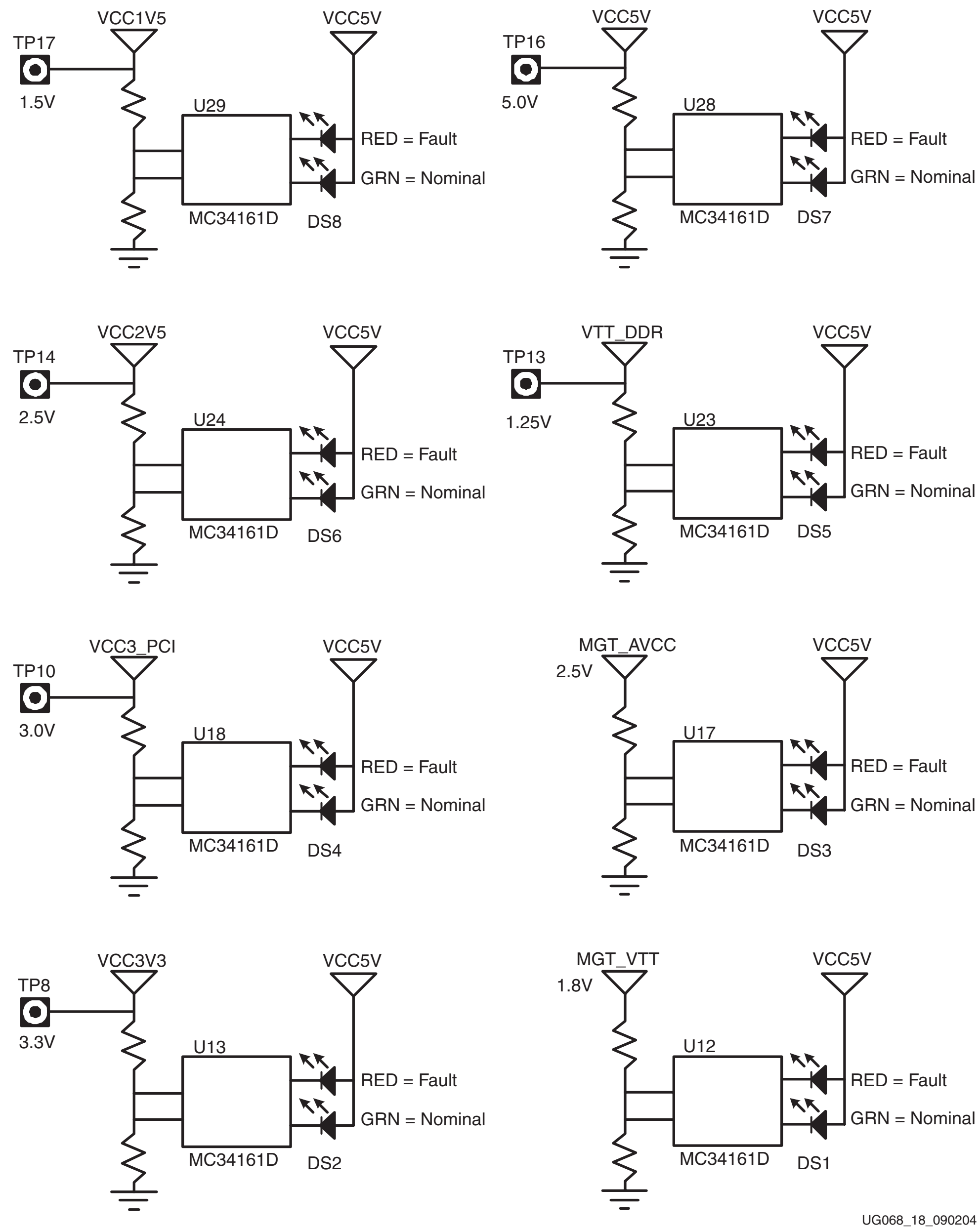

Figure 2-18: **Voltage Monitor**

Table 2-29 shows the various voltage monitor information.

Table 2-29: **Voltage Monitor Information**

Schem Name	Voltage	Testpoint	Indicator LED*	Notes
VCC1V5	1.5V	TP17	DS8	Regulated FPGA core voltage
VCC2V5	2.5V	TP14	DS6	Regulated FPGA/board logic
VCC3_PCI	3.0V	TP10	DS4	Regulated FPGA PCI bank 1-2 voltage
VCC3V3	3.3V	TP8	DS2	Regulated PCI/misc. logic
VCC5V	5.0V	TP16	DS7	From ATX power supply, all regulators derive power
VTT_DDR	1.25V	TP13	DS5	Regulated DDR termination (SSTL2)
MGT_AVCC	2.5V	N/A	DS3	Regulated MGT power
MGT_VTT	1.8V	N/A	DS1	Regulated MGT power
VCC3V3_ATX	3.3V	TP20	N/A	Not used
VCC12V_P	+12V	TP18	N/A	Direct from ATX power supply
VCC12V_N	-12V	TP19	N/A	Direct from ATX power supply

* Green = Voltage Nominal
* Red = Voltage Fault

High-Speed I/O

Xilinx Virtex-II Pro FPGAs offer a variety of high-speed I/O solutions. The ML310 Embedded Development Platform's high-speed I/O is based on the XC2VP30-FF896 FPGA's RocketIO MGT and LVDS capability. The high-speed I/O signals on the FPGA are accessible through two personality module (PM) connectors, PM1 and PM2, on the ML310 board. The ML310 is the host board, functioning as the development platform for Virtex-II Pro FPGA. The PM connectors on the ML310 board provide a means for extending the functionality of the board through high-speed I/O pins. Personality modules connect to the ML310 board using Tyco Z-Dok+ docking connectors, PM1 and PM2. In addition to having differential pairs and shielding ground connections, Z-Dok+ connectors include utility connections for power, ground, and sensing. Tyco Z-Dok+ high-speed connectors are rated to 6.25 Gb/s.

Figure 2-19, page 60 shows a personality module connected to the ML310 board through the PM1 and PM2 connectors. The plug, located on the ML310 board, is referred to as the *host board connector*; the receptacle, located on the personality module, is referred to as the *adapter board connector.*

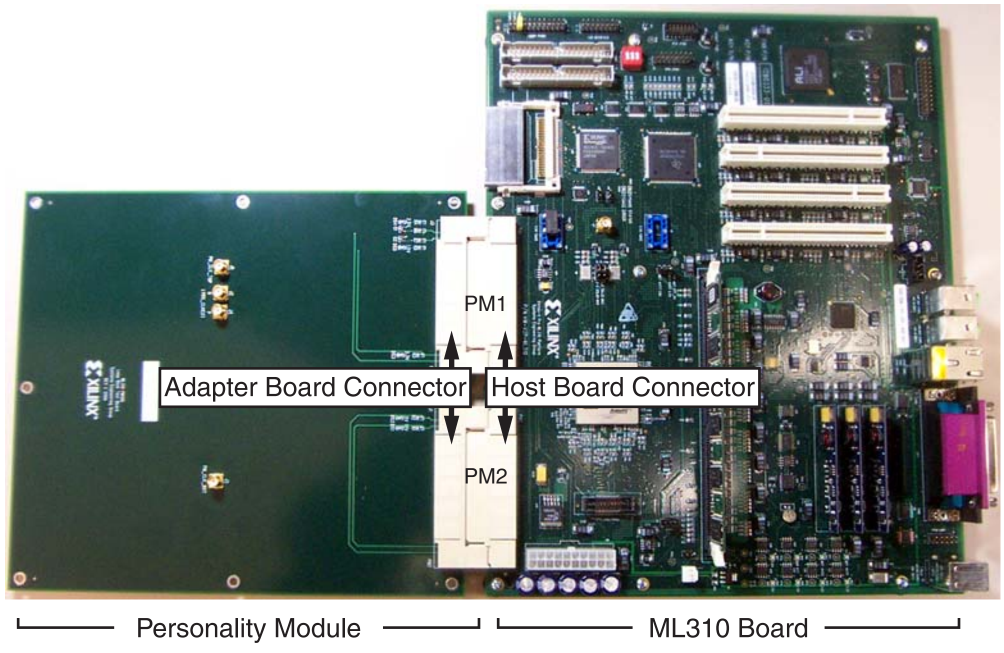

Figure 2-19: **Personality Module Connected to ML310 Board**

ML310 PM Connectors

The ML310 PM connectors are Tyco Z-Dok+ connectors, part number 1367550-5. The "-5" suffix indicates a 40-pair connector. Each connector has 40 differential pairs and several power and ground pins.

Together, the two PM connectors on the ML310 support 158 high-speed I/O pins that can be user defined. The PM1 and PM2 signals are as follows:

- 8 RocketIO MGT pairs (32 pins total)
- 42 LVDS pairs (can be used as 84 single-ended I/O at 2.5V)
- 1 LVDS clock pair
- 38 single-ended I/O
  - 12 at 2.5V
  - 26 at 3.3V
- 2 single-ended 2.5V clocks
- 2 pins not connected

The Tyco data sheet for part number 1367550-5 is available at http://www.z-dok.com/documents/1367550.pdf.

Figure 2-20 shows an edge view of the PM host board connectors on the ML310 board.

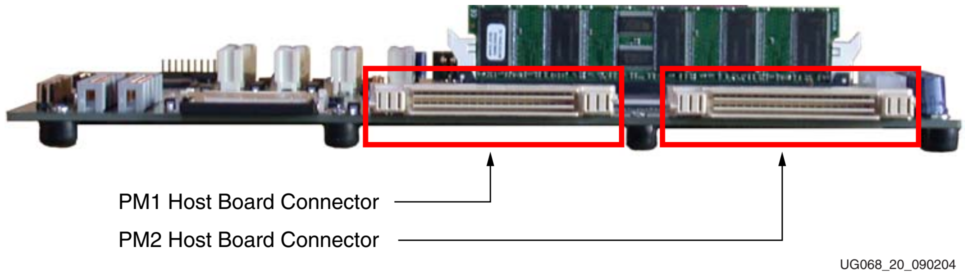

Figure 2-20: **Edge View of Host Board Connectors on ML310**

Each signal pair on the PM1 and PM2 host board connectors has a wide ground pin on the opposite side of the plastic divider, as shown in Figure 2-21. The signal pairs alternate from side to side along the length of the divider. All of the "B" and "E" pins are grounded on the ML310. The "A", "C", "D", and "F" pins are signal pins.

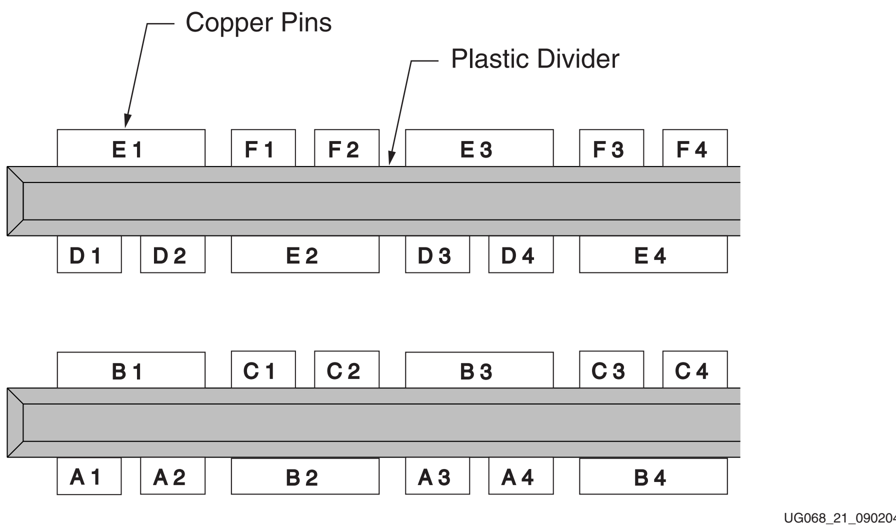

Figure 2-21: **Host Board Connector Pin Detail**

Z-Dok+ Connector Offsets

The Z-Dok+ connectors used on the ML310 board provide four rows of signals pairs. Each row has a particular propagation delay through a mated pair of connectors as shown in Table 2-30.

Table 2-30: **Delay Offsets**

ZDOK+ Connector	Connector Propagation Delay	Physical Length
Row A	145.2 ps	830 mils
Row C	196.8 ps	1125 mils
Row D	213.3 ps	1219 mils
Row F	264.8 ps	1513 mils

Note: Propagation delay, i.e., the delay when traversing through the host board connector and the adapter board connector, was calculated assuming 175 ps/inch. Propagation delay is the total between each male and female connector pair.

All signals with length matching requirements, MGT and LVDS pairs, must include an offset to account for the Z-Dok+ propagation delays. The ML310 board accounts for one-half of the offset, while a user-designed adapter board must account for the other half. The relative offsets for the ML310 host board PM connector are included in Table 2-31. Users are required to compensate for these offsets when designing adapter boards.

Table 2-31: **Relative Offsets from the FPGA to the PM1 and PM2 Connectors**

ZDOK+ Connector	Difference	Offset	Offset/2
Row A	F-A = 1513 - 830	683	342
Row C	F-C = 1513 - 1125	389	194
Row D	F-D = 1513 - 1219	294	147
Row F	F-F = 0 - 0	0	0

Note: All offsets are normalized to row F. The ML310 is designed based on the data in the **Offset/2** column.

PM1 Connector

The PM1 connector on the ML310 board provides the following signals:

- 8 RocketIO 3.125 Gb/s MGTs
- 3 LVDS pairs at 2.5V (can be used as 6 single-ended I/O at 2.5V)
- 1 LVDS clock pair at 2.5V
- 12 single- ended I/O at 2.5V
- 26 single-ended I/O at 3.3V
- 1 single-ended clock at 2.5V
- 1 pin not connected

PM2 Connector

The PM2 connector on the ML310 board provides the following signals:

- 39 LVDS pairs at 2.5V (can be used as 78 single-ended I/O at 2.5V)
- 1 single-ended clock at 2.5V
- 1 pin not connected

Adapter Board PM Connectors

Tyco Z-Dok+ adapter board connectors, part number 1367555-1 are the receptacle connectors on the personality modules that mate to the ML310 Tyco Z-Dok+ host board connectors, part number 1367550-5. The Tyco data sheet for part number 1367555-1 is available at http://www.z-dok.com/documents/1367555.pdf.

On the adapter board connectors, located on the personality module, each signal pair has a pair of ground pins on the opposite side of the open space, as shown in Figure 2-22. The signal pairs alternate from side to side along the length of the open space. All of the "B" and "E" pins are two contacts tied together and grounded on the personality module. The "A", "C", "D", and "F" pins are signal pins.

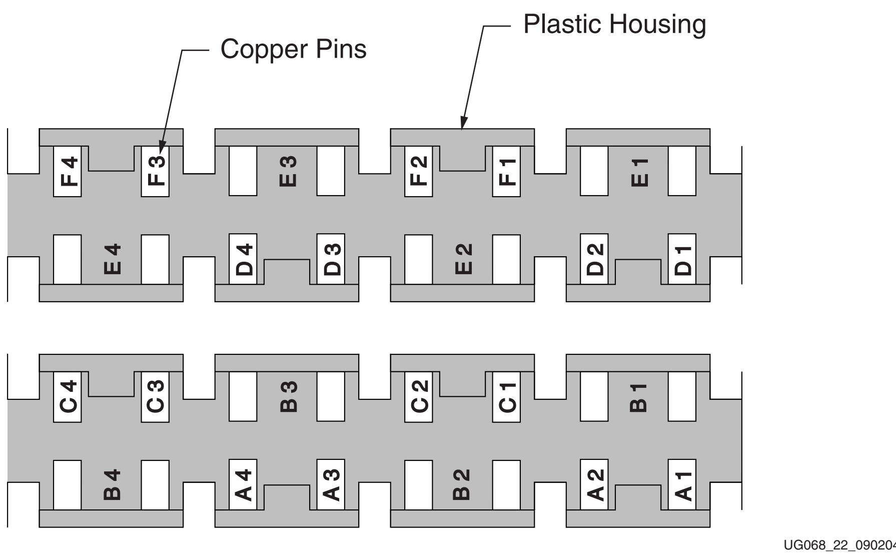

Figure 2-22: **Adapter Board Connector Pin Detail**

Z-DOK+ Utility Pins

Figure 2-23 shows the Z-DOK+ utility pins and numbering for the host board connector, i.e., the PM connector on the ML310.

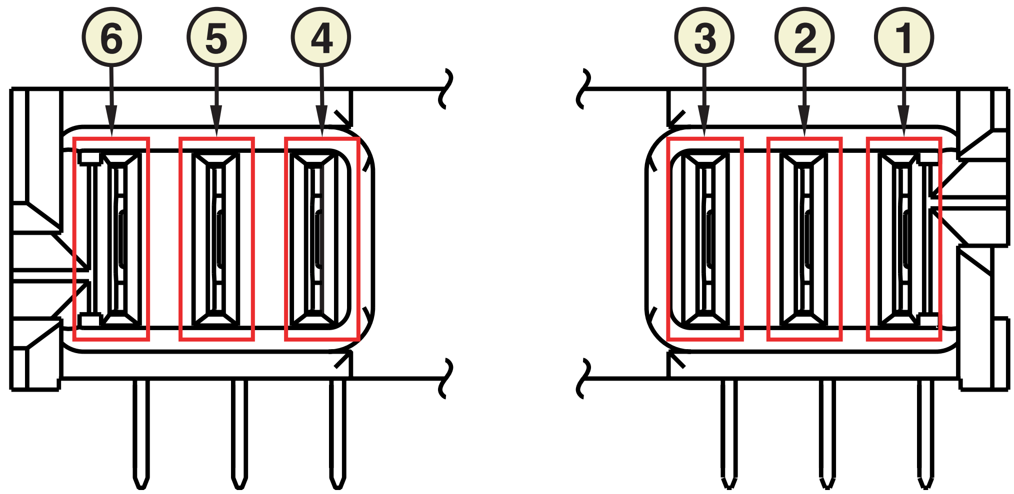

Figure 2-23: **Z-DOK+ Utility Pins (ML310 Side)**

Figure 2-24 shows the Z-DOK+ utility pins and numbering for the adapter board connector.

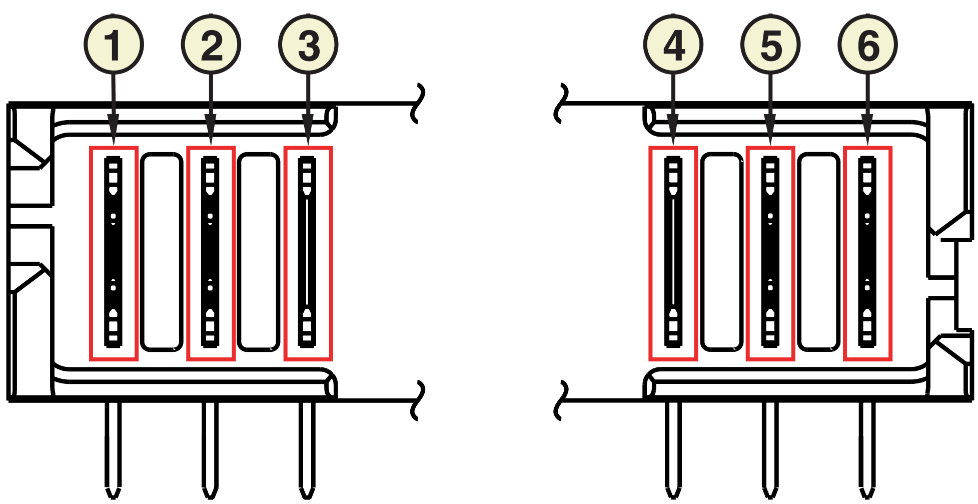

Figure 2-24: **Z-DOK+ Utility Pins (Adapter Side)**

Note: The pins on the adapter board connector are at varying heights, as shown in Table 2-32, page 65 and Table 2-33, page 65.

Contact Order

The Z-Dok+ power and ground pins contact in the following order:

- 1 and 6;
- then 2 and 5;
- then 3 and 4

PM1 Power and Ground

Table 2-32 shows the power and ground pins for the PM1 connector on the ML310.

Table 2-32: **PM1 Power and Ground Pins**

Pin Number	Description	Length	Contact Order
1, 6	Ground	Level 4	First
2, 5	2.5V	Level 3	Second
3	3.3V	Level 2	Third
4	1.5V	Level 2	Third

PM2 Power and Ground

Table 2-33 shows the power and ground pins for the PM2 connector on the ML310.

Table 2-33: **PM2 Power and Ground Pins**

Pin Number	Description	Length	Contact Order
1, 6	Ground	Level 4	First
2, 5	5V	Level 3	Second
3, 4	12V	Level 2	Third

ML310 PM User I/O Pins

PM1 User I/O

The PM1 connector makes the MGT signals from the eight RocketIO MGTs available to the user, along with LVDS pairs and single-ended signals. Table 2-34 shows the pinout for the PM1 connector on the ML310.

Table 2-34: **PM1 Pinout**

PM1 Pin	FPGA Pin	Pin Description	ML310 Schematic Net	FPGA Bank V_{CCO}
A1	H26	IO_L32P_7	PM_IO_94	2.5V
A2	H25	IO_L32N_7	PM_IO_95	2.5V
A3	D26	IO_L03P_7	PM_IO_86	2.5V
A4	C26	IO_L03N_7	PM_IO_87	2.5V
A5	E13	IO_L46N_1	PM_IO_3V_25	3V
A6	E11	IO_L43P_1	PM_IO_3V_18	3V

Table 2-34: **PM1 Pinout *(Continued)***

PM1 Pin	FPGA Pin	Pin Description	ML310 Schematic Net	FPGA Bank V_{CCO}
A7	F10	IO_L07N_1	PM_IO_3V_7	3V
A8	H12	IO_L45P_1	PM_IO_3V_22	3V
A9	C7	IO_L08N_1	PM_IO_3V_9	3V
A10	D10	IO_L37N_1	PM_IO_3V_13	3V
A11	H16	IO_L69P_0	PM_IO_82	2.5V
A12	J16	IO_L69N_0	PM_IO_83	2.5V
A13	A25	RXPPAD4	RXPPAD4_A25	
A14	A24	RXNPAD4	RXNPAD4_A24	
A15	A12	RXPPAD7	RXPPAD7_A12	
A16	A11	RXNPAD7	RXNPAD7_A11	
A17	AK6	TXPPAD16	TXPPAD16_AK6	
A18	AK7	TXNPAD16	TXNPAD16_AK7	
A19	AK19	TXPPAD19	TXPPAD19_AK19	
A20	AK20	TXNPAD19	TXNPAD19_AK20	
C1	D28	IO_L06P_7	PM_IO_90	2.5V
C2	C27	IO_L06N_7	PM_IO_91	2.5V
C3	H11	IO_L39P_1	PM_IO_3V_16	3V
C4	E10	IO_L37P_1	PM_IO_3V_12	3V
C5	F8	IO_L02N_1	PM_IO_3V_1	3V
C6	E9	IO_L03N_1	PM_IO_3V_3	3V
C7	G11	IO_L39N_1	PM_IO_3V_17	3V
C8	G9	IO_L06N_1	PM_IO_3V_5	3V
C9	C18	IO_L68P_0	PM_IO_80	2.5V
C10	D18	IO_L68N_0	PM_IO_81	2.5V
C11	D11	IO_L43N_1	PM_IO_3V_19	3V
C12	E12	IO_L46P_1	PM_IO_3V_24	3V
C13	A18	RXPPAD6	RXPPAD6_A18	
C14	A17	RXNPAD6	RXNPAD6_A17	
C15	A5	RXPPAD9	RXPPAD9_A5	
C16	A4	RXNPAD9	RXNPAD9_A4	
C17	AK13	TXPPAD18	TXPPAD18_AK13	
C18	AK14	TXNPAD18	TXNPAD18_AK14	

Table 2-34: **PM1 Pinout *(Continued)***

PM1 Pin	FPGA Pin	Pin Description	ML310 Schematic Net	FPGA Bank V_{CCO}
C19	AK26	TXPPAD21	TXPPAD21_AK26	
C20	AK27	TXNPAD21	TXNPAD21_AK27	
D1	D30	IO_L31P_7	PM_IO_92	2.5V
D2	D29	IO_L31N_7	PM_IO_93	2.5V
D3	G26	IO_L02P_7	PM_IO_84	2.5V
D4	G25	IO_L02N_7	PM_IO_85	2.5V
D5	A8	IO_L44N_1	PM_IO_3V_21	3V
D6	B8	IO_L44P_1	PM_IO_3V_20	3V
D7	D7	IO_L08P_1	PM_IO_3V_8	3V
D8	F9	IO_L07P_1	PM_IO_3V_6	3V
D9	E8	IO_L03P_1	PM_IO_3V_2	3V
D10	D8	IO_L38P_1	PM_IO_3V_14	3V
D11	D17	IO_L67P_0	PM_IO_78	2.5V
D12	E17	IO_L67N_0	PM_IO_79	2.5V
D13	A27	TXNPAD4	TXNPAD4_A27	
D14	A26	TXPPAD4	TXPPAD4_A26	
D15	A14	TXNPAD7	TXNPAD7_A14	
D16	A13	TXPPAD7	TXPPAD7_A13	
D17	AK4	RXNPAD16	RXNPAD16_AK4	
D18	AK5	RXPPAD16	RXPPAD16_AK5	
D19	AK17	RXNPAD19	RXNPAD19_AK17	
D20	AK18	RXPPAD19	RXPPAD19_AK18	
F1	J24	IO_L05P_7	PM_IO_88	2.5V
F2	J23	IO_L05N_7	PM_IO_89	2.5V
F3	H10	IO_L09P_1	PM_IO_3V_10	3V
F4	H9	IO_L06P_1	PM_IO_3V_4	3V
F5	C8	IO_L38N_1	PM_IO_3V_15	3V
F6	F7	IO_L02P_1	PM_IO_3V_0	3V
F7	G12	IO_L45N_1	PM_IO_3V_23	3V
F8	G10	IO_L09N_1	PM_IO_3V_11	3V
F9	B16	GCLK6S	PM_CLK_TOP	2.5V
F10	NC	NC	NC	NC
F11	F15/AH15	GCLK3P/1S	LVDS_CLKEXT_N	2.5V

Table 2-34: **PM1 Pinout *(Continued)***

PM1 Pin	FPGA Pin	Pin Description	ML310 Schematic Net	FPGA Bank V_{CCO}
A7	F10	IO_L07N_1	PM_IO_3V_7	3V
A8	H12	IO_L45P_1	PM_IO_3V_22	3V
A9	C7	IO_L08N_1	PM_IO_3V_9	3V
A10	D10	IO_L37N_1	PM_IO_3V_13	3V
A11	H16	IO_L69P_0	PM_IO_82	2.5V
A12	J16	IO_L69N_0	PM_IO_83	2.5V
A13	A25	RXPPAD4	RXPPAD4_A25	
A14	A24	RXNPAD4	RXNPAD4_A24	
A15	A12	RXPPAD7	RXPPAD7_A12	
A16	A11	RXNPAD7	RXNPAD7_A11	
A17	AK6	TXPPAD16	TXPPAD16_AK6	
A18	AK7	TXNPAD16	TXNPAD16_AK7	
A19	AK19	TXPPAD19	TXPPAD19_AK19	
A20	AK20	TXNPAD19	TXNPAD19_AK20	
C1	D28	IO_L06P_7	PM_IO_90	2.5V
C2	C27	IO_L06N_7	PM_IO_91	2.5V
C3	H11	IO_L39P_1	PM_IO_3V_16	3V
C4	E10	IO_L37P_1	PM_IO_3V_12	3V
C5	F8	IO_L02N_1	PM_IO_3V_1	3V
C6	E9	IO_L03N_1	PM_IO_3V_3	3V
C7	G11	IO_L39N_1	PM_IO_3V_17	3V
C8	G9	IO_L06N_1	PM_IO_3V_5	3V
C9	C18	IO_L68P_0	PM_IO_80	2.5V
C10	D18	IO_L68N_0	PM_IO_81	2.5V
C11	D11	IO_L43N_1	PM_IO_3V_19	3V
C12	E12	IO_L46P_1	PM_IO_3V_24	3V
C13	A18	RXPPAD6	RXPPAD6_A18	
C14	A17	RXNPAD6	RXNPAD6_A17	
C15	A5	RXPPAD9	RXPPAD9_A5	
C16	A4	RXNPAD9	RXNPAD9_A4	
C17	AK13	TXPPAD18	TXPPAD18_AK13	
C18	AK14	TXNPAD18	TXNPAD18_AK14	

Table 2-34: **PM1 Pinout *(Continued)***

PM1 Pin	FPGA Pin	Pin Description	ML310 Schematic Net	FPGA Bank V_{CCO}
C19	AK26	TXPPAD21	TXPPAD21_AK26	
C20	AK27	TXNPAD21	TXNPAD21_AK27	
D1	D30	IO_L31P_7	PM_IO_92	2.5V
D2	D29	IO_L31N_7	PM_IO_93	2.5V
D3	G26	IO_L02P_7	PM_IO_84	2.5V
D4	G25	IO_L02N_7	PM_IO_85	2.5V
D5	A8	IO_L44N_1	PM_IO_3V_21	3V
D6	B8	IO_L44P_1	PM_IO_3V_20	3V
D7	D7	IO_L08P_1	PM_IO_3V_8	3V
D8	F9	IO_L07P_1	PM_IO_3V_6	3V
D9	E8	IO_L03P_1	PM_IO_3V_2	3V
D10	D8	IO_L38P_1	PM_IO_3V_14	3V
D11	D17	IO_L67P_0	PM_IO_78	2.5V
D12	E17	IO_L67N_0	PM_IO_79	2.5V
D13	A27	TXNPAD4	TXNPAD4_A27	
D14	A26	TXPPAD4	TXPPAD4_A26	
D15	A14	TXNPAD7	TXNPAD7_A14	
D16	A13	TXPPAD7	TXPPAD7_A13	
D17	AK4	RXNPAD16	RXNPAD16_AK4	
D18	AK5	RXPPAD16	RXPPAD16_AK5	
D19	AK17	RXNPAD19	RXNPAD19_AK17	
D20	AK18	RXPPAD19	RXPPAD19_AK18	
F1	J24	IO_L05P_7	PM_IO_88	2.5V
F2	J23	IO_L05N_7	PM_IO_89	2.5V
F3	H10	IO_L09P_1	PM_IO_3V_10	3V
F4	H9	IO_L06P_1	PM_IO_3V_4	3V
F5	C8	IO_L38N_1	PM_IO_3V_15	3V
F6	F7	IO_L02P_1	PM_IO_3V_0	3V
F7	G12	IO_L45N_1	PM_IO_3V_23	3V
F8	G10	IO_L09N_1	PM_IO_3V_11	3V
F9	B16	GCLK6S	PM_CLK_TOP	2.5V
F10	NC	NC	NC	NC
F11	F15/AH15	GCLK3P/1S	LVDS_CLKEXT_N	2.5V

Table 2-34: **PM1 Pinout *(Continued)***

PM1 Pin	FPGA Pin	Pin Description	ML310 Schematic Net	FPGA Bank V_{CCO}
F12	G15/AJ15	GCLK2S/0P	LVDS_CLKEXT_P	2.5V
F13	A20	TXNPAD6	TXNPAD6_A20	
F14	A19	TXPPAD6	TXPPAD6_A19	
F15	A7	TXNPAD9	TXNPAD9_A7	
F16	A6	TXPPAD9	TXPPAD9_A6	
F17	AK11	RXNPAD18	RXNPAD18_AK11	
F18	AK12	RXPPAD18	RXPPAD18_AK12	
F19	AK24	RXNPAD21	RXNPAD21_AK24	
F20	AK25	RXPPAD21	RXPPAD21_AK25	

Notes:

1. LVDS pairs (100 ohm differential impedance) are shown shaded; all other signals are single-ended (50 ohm impedance).
2. LVDS pairs can also be used as single-ended I/O at 2.5V.
3. NC indicates a “no connect” signal.

ML310 PM2 User I/O

The PM2 connector makes most of the LVDS pairs available to the user, along with single-ended signals. Table 2-35 shows the pinout for the PM2 connector on the ML310.

Table 2-35: **PM2 Pinout**

PM2 Pin	FPGA Pin	Pin Description	ML310 Schematic Net	FPGA Bank V_{CCO}
A1	T5	IO_L89N_3	PM_IO_69	2.5V
A2	T6	IO_L89P_3	PM_IO_68	2.5V
A3	T3	IO_L88N_3	PM_IO_67	2.5V
A4	T4	IO_L88P_3	PM_IO_66	2.5V
A5	V3	IO_L58N_3	PM_IO_55	2.5V
A6	V4	IO_L58P_3	PM_IO_54	2.5V
A7	U7	IO_L56N_3	PM_IO_51	2.5V
A8	U8	IO_L56P_3	PM_IO_50	2.5V
A9	V7	IO_L53N_3	PM_IO_45	2.5V
A10	V8	IO_L53P_3	PM_IO_44	2.5V
A11	AC15	IO_L67P_4	PM_IO_72	2.5V
A12	AB15	IO_L67N_4	PM_IO_73	2.5V
A13	AA4	IO_L48P_3	PM_IO_34	2.5V
A14	AA3	IO_L48N_3	PM_IO_35	2.5V
A15	AD2	IO_L42P_3	PM_IO_22	2.5V

Table 2-35: **PM2 Pinout *(Continued)***

PM2 Pin	FPGA Pin	Pin Description	ML310 Schematic Net	FPGA Bank V_{CCO}
A16	AD1	IO_L42N_3	PM_IO_23	2.5V
A17	AG2	IO_L06P_3	PM_IO_6	2.5V
A18	AG1	IO_L06N_3	PM_IO_7	2.5V
A19	AH5	IO_L02P_3	PM_IO_0	2.5V
A20	AG5	IO_L02N_3	PM_IO_1	2.5V
C1	W1	IO_L57N_3	PM_IO_53	2.5V
C2	Y1	IO_L57P_3	PM_IO_52	2.5V
C3	U4	IO_L85N_3	PM_IO_61	2.5V
C4	U5	IO_L85P_3	PM_IO_60	2.5V
C5	W5	IO_L50N_3	PM_IO_39	2.5V
C6	W6	IO_L50P_3	PM_IO_38	2.5V
C7	V5	IO_L55N_3	PM_IO_49	2.5V
C8	V6	IO_L55P_3	PM_IO_48	2.5V
C9	AE14	IO_L68P_4	PM_IO_74	2.5V
C10	AD14	IO_L68N_4	PM_IO_75	2.5V
C11	AB6	IO_L40P_3	PM_IO_20	2.5V
C12	AB5	IO_L40N_3	PM_IO_21	2.5V
C13	AC2	IO_L45P_3	PM_IO_28	2.5V
C14	AB2	IO_L45N_3	PM_IO_29	2.5V
C15	AF2	IO_L36P_3	PM_IO_14	2.5V
C16	AF1	IO_L36N_3	PM_IO_15	2.5V
C17	AH4	IO_L04P_3	PM_IO_4	2.5V
C18	AG3	IO_L04N_3	PM_IO_5	2.5V
C19	AF6	IO_L31P_3	PM_IO_8	2.5V
C20	AE5	IO_L31N_3	PM_IO_9	2.5V
D1	U1	IO_L90N_3	PM_IO_71	2.5V
D2	V1	IO_L90P_3	PM_IO_70	2.5V
D3	T7	IO_L86N_3	PM_IO_63	2.5V
D4	T8	IO_L86P_3	PM_IO_62	2.5V
D5	V2	IO_L60N_3	PM_IO_59	2.5V
D6	W2	IO_L60P_3	PM_IO_58	2.5V
D7	W3	IO_L52N_3	PM_IO_43	2.5V
D8	W4	IO_L52P_3	PM_IO_42	2.5V

Table 2-35: **PM2 Pinout *(Continued)***

PM2 Pin	FPGA Pin	Pin Description	ML310 Schematic Net	FPGA Bank V_{CCO}
D9	T9	IO_L59N_3	PM_IO_57	2.5V
D10	U9	IO_L59P_3	PM_IO_56	2.5V
D11	AG14	IO_L69P_4	PM_IO_76	2.5V
D12	AF14	IO_L69N_4	PM_IO_77	2.5V
D13	AA6	IO_L44P_3	PM_IO_26	2.5V
D14	AA5	IO_L44N_3	PM_IO_27	2.5V
D15	AC4	IO_L43P_3	PM_IO_24	2.5V
D16	AC3	IO_L43N_3	PM_IO_25	2.5V
D17	AE4	IO_L33P_3	PM_IO_10	2.5V
D18	AE3	IO_L33N_3	PM_IO_11	2.5V
D19	AF4	IO_L34P_3	PM_IO_12	2.5V
D20	AF3	IO_L34N_3	PM_IO_13	2.5V
F1	AA1	IO_L51N_3	PM_IO_41	2.5V
F2	AB1	IO_L51P_3	PM_IO_40	2.5V
F3	U2	IO_L87N_3	PM_IO_65	2.5V
F4	U3	IO_L87P_3	PM_IO_64	2.5V
F5	Y2	IO_L54N_3	PM_IO_47	2.5V
F6	AA2	IO_L54P_3	PM_IO_46	2.5V
F7	Y4	IO_L49N_3	PM_IO_37	2.5V
F8	Y5	IO_L49P_3	PM_IO_36	2.5V
F9	NC	NC	NC	2.5V
F10	AG15	IO_L74P_4	PM_CLK_BOT	2.5V
F11	W8	IO_L47P_3	PM_IO_32	2.5V
F12	W7	IO_L47N_3	PM_IO_33	2.5V
F13	AB4	IO_L46P_3	PM_IO_30	2.5V
F14	AB3	IO_L46N_3	PM_IO_31	2.5V
F15	AE2	IO_L39P_3	PM_IO_18	2.5V
F16	AE1	IO_L39N_3	PM_IO_19	2.5V
F17	AH2	IO_L03P_3	PM_IO_2	2.5V
F18	AH1	IO_L03N_3	PM_IO_3	2.5V
F19	AD4	IO_L37P_3	PM_IO_16	2.5V

Table 2-35: **PM2 Pinout *(Continued)***

PM2 Pin	FPGA Pin	Pin Description	ML310 Schematic Net	FPGA Bank V_{CCO}
F20	AD3	IO_L37N_3	PM_IO_17	2.5V

Notes:

1. LVDS pairs (100 ohm differential impedance) are shown shaded; all other signals are single-ended (50 ohm impedance).
2. LVDS pairs can also be used as single-ended I/O at 2.5V.
3. NC indicates a “no connect” signal.