DISCLAIMER
The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available “AS IS” and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx’s limited warranty, please refer to Xilinx’s Terms of Sale which can be viewed at http://www.xilinx.com/legal.htm#tos. IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx’s Terms of Sale which can be viewed at http://www.xilinx.com/legal.htm#tos.

© Copyright 2012–2013 Xilinx, Inc. Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.

Revision History
The following table shows the revision history for this document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>11/07/2012</td>
<td>1.0</td>
<td>Initial Xilinx release.</td>
</tr>
<tr>
<td>11/06/2013</td>
<td>4.0</td>
<td>Updated for Vivado® Design Suite 2013.3. Device number was corrected from XC7V485T to XC7VX485T. Updated most figures in Chapter 1, VC7203 IBERT Getting Started Guide. The ZIP project file name changed to rdf0272-vc7203-ibert-2013-3.zip. In Figure 1-11, Digilent JTAG cable changed to Xilinx TCF agent. Figure 1-30 was renamed Design Sources File Hierarchy. Figure 1-31, Synthesize Out-Of-Context Module was deleted. Updated Appendix A, Additional Resources links.</td>
</tr>
</tbody>
</table>
# Table of Contents

Revision History ................................................................. 2

Chapter 1: VC7203 IBERT Getting Started Guide

Overview .................................................................................. 5
Requirements ........................................................................... 6
Setting Up the VC7203 Board .................................................. 6
Extracting the Project Files ...................................................... 7
Running the GTX IBERT Demonstration ................................. 7
   Connecting the GTX Transceivers and Reference Clocks ....... 8
   Attach the GTX Quad Connector ........................................... 10
   GTX Transceiver Clock Connections .................................... 11
   GTX TX/RX Loopback Connections ..................................... 11
   Configuring the FPGA ............................................................ 13
   Launching the Vivado Design Suite Software ...................... 14
   Starting the SuperClock-2 Module ....................................... 16
   Viewing GTX Transceiver Operation .................................... 23
   Closing the IBERT Demonstration ....................................... 23
SuperClock-2 Frequency Table .............................................. 24
Creating the GTX IBERT Core .............................................. 25

Appendix A: Additional Resources

   Xilinx Resources ................................................................. 41
   Solution Centers ............................................................... 41
   Further Resources ............................................................ 41

Appendix B: Warranty
Overview

This document provides a procedure for setting up the VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board to run the Integrated Bit Error Ratio Test (IBERT) demonstration using the Vivado® Design Suite. The designs that are required to run the IBERT demonstration are stored in a Secure Digital (SD) memory card that is provided with the VC7203 board. The demonstration shows the capabilities of the Virtex-7 XC7VX485T FPGA GTX transceiver.

The VC7203 board is described in detail in VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board User Guide (UG957).

The IBERT demonstrations operate one GTX Quad at a time. The procedure consists of:

1. **Setting Up the VC7203 Board**, page 6
2. **Extracting the Project Files**, page 7
3. **Connecting the GTX Transceivers and Reference Clocks**, page 8
4. **Configuring the FPGA**, page 13
5. **Launching the Vivado Design Suite Software**, page 14
6. **Starting the SuperClock-2 Module**, page 16
7. **Viewing GTX Transceiver Operation**, page 23
8. **Closing the IBERT Demonstration**, page 23
Chapter 1: VC7203 IBERT Getting Started Guide

Requirements

The hardware and software required to run the GTX IBERT demonstrations are:

- VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board including:
  - One SD card containing the IBERT demonstration designs
  - One Samtec BullsEye cable
  - Eight SMA female-to-female (F-F) adapters
  - Six 50Ω SMA terminators
  - GTX transceiver power supply module (installed on board)
  - SuperClock-2 module, Rev 1.0 (installed on board)
  - 12V DC power adapter
  - USB cable, standard-A plug to Micro-B plug
- Host PC with:
  - SD card reader
  - USB ports
  - Xilinx Vivado Design Suite software, version 2013.3

The hardware and software required to rebuild the IBERT demonstration designs are:

- Xilinx Vivado Design Suite version 2013.3
- PC with a version of the Windows operating system supported by Xilinx Vivado Design Suite

Setting Up the VC7203 Board

This section describes how to set up the VC7203 board.

**Caution!** The VC7203 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

When the VC7203 board ships from the factory, it is configured for the GTX IBERT demonstrations described in this document. If the board has been re-configured it must be returned to the default set-up before running the IBERT demonstrations.

1. Move all jumpers and switches to their default positions. The default jumper and switch positions are listed in *VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board User Guide* (UG957).
2. Install the GTX transceiver power module by plugging it into connectors J66 and J97.
3. Install the SuperClock-2 module:
   a. Align the three metal standoffs on the bottom side of the module with the three mounting holes in the SUPERCLOCK-2 MODULE interface of the VC7203 board.
   b. Using three 4-40 x 0.25 inch screws, firmly screw down the module from the bottom of the VC7203 board.
   c. On the SuperClock-2 module, place a jumper across pins 2–3 (2V5) of the CONTROL VOLTAGE header, J18, and place another jumper across Si570 INH header J11.
   d. Screw down a 50Ω SMA terminator onto each of the six unused Si5368 clock output SMA connectors: J7, J8, J12, J15, J16 and J17.
Extracting the Project Files

The Vivado project files required to run the IBERT demonstrations are located in rdf0272-vc7203-ibert-2013-3.zip on the SD card provided with the VC7203 board. This collection is also available online at the Virtex-7 FPGA VC7203 Characterization Kit documentation website.

The ZIP collection also contains two Tcl scripts: add_scm2.tcl and setup_scm2_156_25.tcl, and seven Vivado probe files: vc7203_q113.ltx, vc7203_q114.ltx, vc7203_q115.ltx, vc7203_q116.ltx, vc7203_q117.ltx, vc7203_q118.ltx, and vc7203_q119.ltx. The Tcl scripts are used to help merge the IBERT and SuperClock-2 source code (described in Creating the GTX IBERT Core, page 25) and to set up the SuperClock-2 module to run at 156.25 MHz (described in Launching the Vivado Design Suite Software, page 14). The debug probes are used by Vivado design tools to properly load the SuperClock-2 VIO core.

To copy the files from the Secure Digital memory card:

1. Connect the Secure Digital memory card to the host computer.
3. Unzip the files to a working directory on the host computer.

Running the GTX IBERT Demonstration

The GTX IBERT demonstration operates one GTX Quad at a time. This section describes how to test GTX Quad 115. The remaining GTX Quads are tested following a similar series of steps.
Connecting the GTX Transceivers and Reference Clocks

Figure 1-1 shows the locations for GTX transceiver Quads 113, 114, 115, 116, 117, 118, and 119 on the VC7203 board.

*Note:* Figure 1-1 is for reference only and might not reflect the current revision of the board.

*Figure 1-1: GTX Quad Locations*
All GTX transceiver pins and reference clock pins are routed from the FPGA to a connector pad which interfaces with Samtec BullsEye connectors. Figure 1-2 A shows the connector pad. Figure 1-2 B shows the connector pinout.

![GTX Connector Pad](image1)

![GTX Connector Pinout](image2)

**Figure 1-2:** A – GTX Connector Pad. B – GTX Connector Pinout

The SuperClock-2 module provides LVDS clock outputs for the GTX transceiver reference clocks in the IBERT demonstrations. Figure 1-3 shows the locations of the differential clock SMA connectors on the clock module which can be connected to the reference clock cables.

**Note:** The image in Figure 1-3 is for reference only and might not reflect the current revision of the board.

![SuperClock-2 Module Output Clock SMA Locations](image3)

**Figure 1-3:** SuperClock-2 Module Output Clock SMA Locations

The four SMA pairs labeled CLKOUT provide LVDS clock outputs from the Si5368 clock multiplier/jitter attenuator device on the clock module. The SMA pair labeled Si570_CLK provides LVDS clock output from the Si570 programmable oscillator on the clock module.

**Note:** The Si570 oscillator does not support LVDS output on the Rev B and earlier revisions of the SuperClock-2 module.

For the GTX IBERT demonstration, the output clock frequencies are preset to 156.25 MHz. For more information regarding the SuperClock-2 module, see [HW-CLK-101-SCLK2 SuperClock-2 Module User Guide](http://www.xilinx.com).
Attach the GTX Quad Connector

Before connecting the BullsEye cable assembly to the board, firmly secure the blue elastomer seal provided with the cable assembly to the bottom of the connector housing if it is not already inserted (see Figure 1-4).

Note: Figure 1-4 is for reference only and might not reflect the current version of the connector.

![BullsEye Connector with Elastomer Seal](image1)

Figure 1-4: BullsEye Connector with Elastomer Seal

Attach the Samtec BullsEye connector to GTX Quad 115 (Figure 1-5), aligning the two indexing pins on the bottom of the connector with the guide holes on the board. Hold the connector flush with the board and fasten it by tightening the two captive screws.

![BullsEye Connector Attached to Quad 115](image2)

Figure 1-5: BullsEye Connector Attached to Quad 115
GTX Transceiver Clock Connections

See Figure 1-2, page 9 to identify the P and N coax cables that are connected to the CLK1 reference clock inputs. Connect these cables to the SuperClock-2 module as follows:

- CLK1_P coax cable → SMA connector J5 (CLKOUT1_P) on the SuperClock-2 module
- CLK1_N coax cable → SMA connector J6 (CLKOUT1_N) on the SuperClock-2 module

Note: Any one of the five differential outputs from the SuperClock-2 module can be used to source the GTX reference clock. CLKOUT1_P and CLKOUT1_N are used here as an example.

GTX TX/RX Loopback Connections

See Figure 1-2, page 9 to identify the P and N coax cables that are connected to the four receivers (RX0, RX1, RX2 and RX3) and the four transmitters (TX0, TX1, TX2 and TX3). Use eight SMA female-to-female (F-F) adapters (Figure 1-6), to connect the transmit and receive cables as shown in Figure 1-7 and detailed here:

- TX0_P → SMA F-F Adapter → RX0_P
- TX0_N → SMA F-F Adapter → RX0_N
- TX1_P → SMA F-F Adapter → RX1_P
- TX1_N → SMA F-F Adapter → RX1_N
- TX2_P → SMA F-F Adapter → RX2_P
- TX2_N → SMA F-F Adapter → RX2_N
- TX3_P → SMA F-F Adapter → RX3_P
- TX3_N → SMA F-F Adapter → RX3_N

Note: To ensure good connectivity, it is recommended that the adapters be secured with a wrench; however, do not over tighten the SMAs.
Figure 1-7: **TX-To-RX Loopback Connection Example**

Figure 1-8 shows the VC7203 board with the cable connections required for the Quad 115 GTX IBERT demonstration.

**Figure 1-8:** **Cable Connections for Quad 115 GTX IBERT Demonstration**
Running the GTX IBERT Demonstration

Configuring the FPGA

This section describes how to configure the FPGA using the SD card included with the board. The FPGA can also be configured through the Vivado Design Suite software using the .bit files and .ltx probe files which are available online (as collection rdf0272-vc7203-ibert-2013-3.zip) at the Virtex-7 FPGA VC7203 Characterization Kit documentation website.

To configure from the SD card:

1. Insert the SD card provided with the VC7203 board into the SD card reader slot located on the bottom-side (upper-right corner) of the VC7203 board.
2. Plug the 12V output from the power adapter into connector J2 on the VC7203 board.
3. Connect the host computer to the VC7203 board using a standard-A plug to Micro-B plug USB cable. The standard-A plug connects to a USB port on the host computer and the Micro-B plug connects to U8, the Digilent USB JTAG configuration port on the VC7203 board.
4. Select the GTX IBERT demonstration with the System ACE™ SD controller SYSACE-2 CFG switch, SW8. The setting on this 4-bit DIP switch (Figure 1-9) selects the file used to configure the FPGA. A switch is in the ON position if set to the far right and in the OFF position if set to the far left. For the Quad 115 GTX IBERT demonstration, set ADR2 = ON, ADR1 = OFF, and ADR0 = ON. The MODE bit (switch position 4) is not used and can be set either ON or OFF.
5. Place the main power switch SW1 to the ON position.

There is one IBERT demonstration design for each GTX Quad on the VC7203 board, for a total of seven IBERT designs. An additional design is provided to demonstrate the USB/UART interface (details of this demonstration are described in the README file on the SD card). All eight designs are organized and stored on the SD card as shown in Table 1-1.

Table 1-1: SD Card Contents and Configuration Addresses

<table>
<thead>
<tr>
<th>Demonstration Design</th>
<th>ADR2</th>
<th>ADR1</th>
<th>ADR0</th>
</tr>
</thead>
<tbody>
<tr>
<td>GTX Quad 113</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>GTX Quad 114</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>GTX Quad 115</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>GTX Quad 116</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>GTX Quad 117</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
</tr>
<tr>
<td>GTX Quad 118</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
</tr>
</tbody>
</table>
Launching the Vivado Design Suite Software

1. Start Vivado Design Suite on the host computer and click **Flow > Open Hardware Manager** (highlighted in **Figure 1-10**).

<table>
<thead>
<tr>
<th>Demonstration Design</th>
<th>ADR2</th>
<th>ADR1</th>
<th>ADR0</th>
</tr>
</thead>
<tbody>
<tr>
<td>GTX Quad 119</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>USB/UART</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
</tbody>
</table>
2. In the Hardware Manager window, click **Open a new hardware target** (highlighted in Figure 1-11).

![Figure 1-11: Open a New Hardware Target](image)

3. An Open Hardware Target wizard pops up. Click **Next** on the first window.
4. In the Vivado CSE Server Name window, make sure **localhost:60001** is entered for the Server name. Click **Next** and it opens the server to connect to the Xilinx TCF agent.
5. In the Select Hardware Target window, the \texttt{xilinx\_tcf} cable appears under Type. The JTAG chain contents of the selected cable appears under the Hardware Devices window (Figure 1-12). Select \texttt{xilinx\_tcf} and click \textbf{Next}.

![Select Hardware Target](image)

*Figure 1-12: Select Hardware Target*

6. In the Set Hardware Target Properties window, leave the defaults and click \textbf{Next}. In the Open Hardware Target Summary window, click \textbf{Finish}. The wizard closes and the Vivado tool opens the hardware target.

Starting the SuperClock-2 Module

The IBERT demonstration designs use an integrated VIO core to control the clocks on the SuperClock-2 module. The SuperClock-2 module features two clock-source components: 1) An always-on Si570 crystal oscillator and, 2) an Si5368 jitter-attenuating clock multiplier. Outputs from either device can be used to drive the transceiver reference clocks.
To start the SuperClock-2 module:

1. The Hardware window shows the System ACE and the XC7VX485T device and reports that it is programmed. Select **XC7VX485T_1**. In the Hardware Device Properties window, enter the file path to the Probes file associated with the Q115 IBERT design (**vc7203_q115.ltx**) (Figure 1-13).

![Figure 1-13: Adding the Probes File](image)
2. In the Hardware window, right-click **XC7VX485T_1** and select **Refresh Device** (Figure 1-14).

![Figure 1-14: Refresh Device](image)
3. The Vivado tool now shows the SuperClock-2 VIO core and the IBERT core. To configure the SuperClock-2 module, select **Tools > Run Tcl Script** (Figure 1-15). In the following Run Script window, navigate to the `setup_scm2_156_25.tcl` script in the extracted files and click **OK**.

![Run Tcl Script](image)

*Figure 1-15: Run Tcl Script...*

4. To view the SuperClock 2 settings in the VIO core, select the following signals:

   - `u_scm2/u_vio_sclk2_control/si570_start`
   - `u_scm2/u_vio_sclk2_control/si570_addr[6:0]`
   - `u_scm2/u_vio_sclk2_control/si5368_start`
   - `u_scm2/u_vio_sclk2_control/si5368_addr[6:0]`
Drag these signals from the Debug Probes window to the VIO Probes window (Figure 1-16).

**Note:** The ROM address values for the Si5368 and Si570 devices (that is, si5368_addr[6:0] and si570_addr[6:0]) are preset to 60 to produce an output frequency of 156.250 MHz. Entering a different ROM address changes the reference clock(s) frequency. The complete list of pre-programmed SuperClock-2 frequencies and their associated ROM addresses is provided in Table 1-2, page 24.

**Figure 1-16:** SuperClock-2 Module VIO Core
5. To view the GTX transceiver operation, click Layout > Serial I/O Analyzer. In the Links window, right-click and select **Create Links** or press the **Create Links** button. The **Auto-detect links** button can also be used to have the tools automatically scan for any links that are connected and currently linked (Figure 1-17).

![Serial I/O Analyzer - Create Links...](image)

**Figure 1-17:** Serial I/O Analyzer - Create Links...

6. If **Create Links** was selected, a pop up window displays. In this window you can link any TX to RX GT transceivers. To create links, select the **TX GT** and **RX GT** from the two lists, then press the **Add (+)** button. For this project, connect the following links:

- MGT_X1Y8/TX to MGT_X1Y8/RX
- MGT_X1Y9/TX to MGT_X1Y9/RX
- MGT_X1Y10/TX to MGT_X1Y10/RX
- MGT_X1Y11/TX to MGT_X1Y11/RX
This is shown in Figure 1-18.

![Create Links Window](image_url)

**Figure 1-18:** Create Links Window
Running the GTX IBERT Demonstration

Viewing GTX Transceiver Operation

After completing step 6 in Starting the SuperClock-2 Module, the IBERT demonstration is configured and running. The status and test settings are displayed on the Links tab in the Links window shown in Figure 1-19.

Note the line rate, TX differential output swing, and error count:

- The line rate for all four GTX transceivers is 12.5 Gb/s (see Status in Figure 1-19).
- The GTX transmitter differential output swing is preset to 850 mV.
- Verify that there are no bit errors.

Additional information on the Vivado Design Suite software and IBERT core can be found in Vivado Design Suite User Guide: Programming and Debugging (UG908) and LogiCORE IP Integrated Bit Error Ratio Tester (IBERT) for 7 Series GTX Transceivers Product Guide for Vivado Design Suite (PG132).

Closing the IBERT Demonstration

To stop the IBERT demonstration:

2. Place the main power switch SW1 in the off position.
SuperClock-2 Frequency Table

Table 1-2 lists the addresses for the frequencies that are programmed into the SuperClock-2 read-only-memory (ROM).

Table 1-2: Si570 and Si5368 Frequency Table

<table>
<thead>
<tr>
<th>Address</th>
<th>Protocol</th>
<th>Frequency (MHz)</th>
<th>Address</th>
<th>Protocol</th>
<th>Frequency (MHz)</th>
<th>Address</th>
<th>Protocol</th>
<th>Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>100GE/40GE/10GE</td>
<td>161.130</td>
<td>30</td>
<td>OBSAI</td>
<td>307.200</td>
<td>60</td>
<td>XAUI</td>
<td>156.250</td>
</tr>
<tr>
<td>1</td>
<td>Aurora</td>
<td>81.250</td>
<td>31</td>
<td>OBSAI</td>
<td>614.400</td>
<td>61</td>
<td>XAUI</td>
<td>312.500</td>
</tr>
<tr>
<td>2</td>
<td>Aurora</td>
<td>162.500</td>
<td>32</td>
<td>OC-48</td>
<td>19.440</td>
<td>62</td>
<td>XAUI</td>
<td>625.000</td>
</tr>
<tr>
<td>3</td>
<td>Aurora</td>
<td>325.000</td>
<td>33</td>
<td>OC-48</td>
<td>77.760</td>
<td>63</td>
<td>Generic</td>
<td>66.667</td>
</tr>
<tr>
<td>4</td>
<td>Aurora</td>
<td>650.000</td>
<td>34</td>
<td>OC-48</td>
<td>155.520</td>
<td>64</td>
<td>Generic</td>
<td>133.333</td>
</tr>
<tr>
<td>5</td>
<td>CEI11</td>
<td>173.370</td>
<td>35</td>
<td>OC-48</td>
<td>311.040</td>
<td>65</td>
<td>Generic</td>
<td>166.667</td>
</tr>
<tr>
<td>6</td>
<td>CPRI</td>
<td>61.440</td>
<td>36</td>
<td>OC-48</td>
<td>622.080</td>
<td>66</td>
<td>Generic</td>
<td>266.667</td>
</tr>
<tr>
<td>7</td>
<td>CPRI</td>
<td>122.880</td>
<td>37</td>
<td>OTU-1</td>
<td>166.629</td>
<td>67</td>
<td>Generic</td>
<td>333.333</td>
</tr>
<tr>
<td>8</td>
<td>CPRI</td>
<td>153.630</td>
<td>38</td>
<td>OTU-1</td>
<td>333.257</td>
<td>68</td>
<td>Generic</td>
<td>533.333</td>
</tr>
<tr>
<td>9</td>
<td>CPRI</td>
<td>245.760</td>
<td>39</td>
<td>OTU-1</td>
<td>666.514</td>
<td>69</td>
<td>Generic</td>
<td>644.000</td>
</tr>
<tr>
<td>10</td>
<td>CPRI</td>
<td>491.520</td>
<td>40</td>
<td>OTU-1</td>
<td>666.750</td>
<td>70</td>
<td>Generic</td>
<td>666.667</td>
</tr>
<tr>
<td>11</td>
<td>Display Port</td>
<td>67.500</td>
<td>41</td>
<td>OTU-2</td>
<td>167.330</td>
<td>71</td>
<td>Generic</td>
<td>205.000</td>
</tr>
<tr>
<td>12</td>
<td>Display Port</td>
<td>81.000</td>
<td>42</td>
<td>OTU-2</td>
<td>669.310</td>
<td>72</td>
<td>Generic</td>
<td>210.000</td>
</tr>
<tr>
<td>13</td>
<td>Display Port</td>
<td>135.000</td>
<td>43</td>
<td>OTU-3</td>
<td>168.050</td>
<td>73</td>
<td>Generic</td>
<td>215.000</td>
</tr>
<tr>
<td>14</td>
<td>Display Port</td>
<td>162.000</td>
<td>44</td>
<td>OTU-4</td>
<td>174.690</td>
<td>74</td>
<td>Generic</td>
<td>220.000</td>
</tr>
<tr>
<td>15</td>
<td>Fibrechannel</td>
<td>106.250</td>
<td>45</td>
<td>PCIe</td>
<td>100.000</td>
<td>75</td>
<td>Generic</td>
<td>225.000</td>
</tr>
<tr>
<td>16</td>
<td>Fibrechannel</td>
<td>212.500</td>
<td>46</td>
<td>PCIe</td>
<td>125.000</td>
<td>76</td>
<td>Generic</td>
<td>230.000</td>
</tr>
<tr>
<td>17</td>
<td>Fibrechannel</td>
<td>425.000</td>
<td>47</td>
<td>PCIe</td>
<td>250.000</td>
<td>77</td>
<td>Generic</td>
<td>235.000</td>
</tr>
<tr>
<td>18</td>
<td>GigE</td>
<td>62.500</td>
<td>48</td>
<td>SATA</td>
<td>75.000</td>
<td>78</td>
<td>Generic</td>
<td>240.000</td>
</tr>
<tr>
<td>19</td>
<td>GigE</td>
<td>125.000</td>
<td>49</td>
<td>SATA</td>
<td>150.000</td>
<td>79</td>
<td>Generic</td>
<td>245.000</td>
</tr>
<tr>
<td>20</td>
<td>GigE</td>
<td>250.000</td>
<td>50</td>
<td>SATA</td>
<td>300.000</td>
<td>80</td>
<td>Generic</td>
<td>250.000</td>
</tr>
<tr>
<td>21</td>
<td>GigE</td>
<td>500.000</td>
<td>51</td>
<td>SATA</td>
<td>600.000</td>
<td>81</td>
<td>Generic</td>
<td>255.000</td>
</tr>
<tr>
<td>22</td>
<td>GPON</td>
<td>187.500</td>
<td>52</td>
<td>SDI</td>
<td>74.250</td>
<td>82</td>
<td>Generic</td>
<td>260.000</td>
</tr>
<tr>
<td>23</td>
<td>Interlaken</td>
<td>132.813</td>
<td>53</td>
<td>SDI</td>
<td>148.500</td>
<td>83</td>
<td>Generic</td>
<td>265.000</td>
</tr>
<tr>
<td>24</td>
<td>Interlaken</td>
<td>195.313</td>
<td>54</td>
<td>SDI</td>
<td>297.000</td>
<td>84</td>
<td>Generic</td>
<td>270.000</td>
</tr>
<tr>
<td>25</td>
<td>Interlaken</td>
<td>265.625</td>
<td>55</td>
<td>SDI</td>
<td>594.000</td>
<td>85</td>
<td>Generic</td>
<td>275.000</td>
</tr>
<tr>
<td>26</td>
<td>Interlaken</td>
<td>390.625</td>
<td>56</td>
<td>SMPTE435M</td>
<td>167.063</td>
<td>86</td>
<td>Generic</td>
<td>280.000</td>
</tr>
<tr>
<td>27</td>
<td>Interlaken</td>
<td>531.250</td>
<td>57</td>
<td>SMPTE435M</td>
<td>334.125</td>
<td>87</td>
<td>Generic</td>
<td>285.000</td>
</tr>
<tr>
<td>28</td>
<td>OBSAI</td>
<td>76.800</td>
<td>58</td>
<td>SMPTE435M</td>
<td>668.250</td>
<td>88</td>
<td>Generic</td>
<td>290.000</td>
</tr>
<tr>
<td>29</td>
<td>OBSAI</td>
<td>153.600</td>
<td>59</td>
<td>XAUI</td>
<td>78.125</td>
<td>89</td>
<td>Generic</td>
<td>295.000</td>
</tr>
<tr>
<td>30</td>
<td>Generic</td>
<td>300.000</td>
<td>103</td>
<td>Generic</td>
<td>365.000</td>
<td>116</td>
<td>Generic</td>
<td>430.000</td>
</tr>
<tr>
<td>31</td>
<td>Generic</td>
<td>305.000</td>
<td>104</td>
<td>Generic</td>
<td>370.000</td>
<td>117</td>
<td>Generic</td>
<td>435.000</td>
</tr>
</tbody>
</table>
Creating the GTX IBERT Core

Vivado Design Suite version 2013.3 is required to rebuild the designs shown here.

This section provides a procedure to create a single Quad GTX IBERT core with integrated SuperClock-2 controller. The procedure assumes Quad 113 and 12.5 Gb/s line rate, but cores for any of the GTX Quads with any supported line rate can be created following the same series of steps.

For more details on generating IBERT cores, refer to Vivado Design Suite User Guide: Programming and Debugging (UG908).

1. Start the Vivado Design Suite.

<table>
<thead>
<tr>
<th>Address</th>
<th>Protocol</th>
<th>Frequency (MHz)</th>
<th>Address</th>
<th>Protocol</th>
<th>Frequency (MHz)</th>
<th>Address</th>
<th>Protocol</th>
<th>Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>92</td>
<td>Generic</td>
<td>310.000</td>
<td>105</td>
<td>Generic</td>
<td>375.000</td>
<td>118</td>
<td>Generic</td>
<td>440.000</td>
</tr>
<tr>
<td>93</td>
<td>Generic</td>
<td>315.000</td>
<td>106</td>
<td>Generic</td>
<td>380.000</td>
<td>119</td>
<td>Generic</td>
<td>445.000</td>
</tr>
<tr>
<td>94</td>
<td>Generic</td>
<td>320.000</td>
<td>107</td>
<td>Generic</td>
<td>385.000</td>
<td>120</td>
<td>Generic</td>
<td>450.000</td>
</tr>
<tr>
<td>95</td>
<td>Generic</td>
<td>325.000</td>
<td>108</td>
<td>Generic</td>
<td>390.000</td>
<td>121</td>
<td>Generic</td>
<td>455.000</td>
</tr>
<tr>
<td>96</td>
<td>Generic</td>
<td>330.000</td>
<td>109</td>
<td>Generic</td>
<td>395.000</td>
<td>122</td>
<td>Generic</td>
<td>460.000</td>
</tr>
<tr>
<td>97</td>
<td>Generic</td>
<td>335.000</td>
<td>110</td>
<td>Generic</td>
<td>400.000</td>
<td>123</td>
<td>Generic</td>
<td>465.000</td>
</tr>
<tr>
<td>98</td>
<td>Generic</td>
<td>340.000</td>
<td>111</td>
<td>Generic</td>
<td>405.000</td>
<td>124</td>
<td>Generic</td>
<td>470.000</td>
</tr>
<tr>
<td>99</td>
<td>Generic</td>
<td>345.000</td>
<td>112</td>
<td>Generic</td>
<td>410.000</td>
<td>125</td>
<td>Generic</td>
<td>475.000</td>
</tr>
<tr>
<td>100</td>
<td>Generic</td>
<td>350.000</td>
<td>113</td>
<td>Generic</td>
<td>415.000</td>
<td>126</td>
<td>Generic</td>
<td>480.000</td>
</tr>
<tr>
<td>101</td>
<td>Generic</td>
<td>355.000</td>
<td>114</td>
<td>Generic</td>
<td>420.000</td>
<td>127</td>
<td>Generic</td>
<td>485.000</td>
</tr>
<tr>
<td>102</td>
<td>Generic</td>
<td>360.000</td>
<td>115</td>
<td>Generic</td>
<td>425.000</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 1-2: Si570 and Si5368 Frequency Table (Cont’d)
2. In the Vivado design tools window, click the Manage IP icon (highlighted in Figure 1-20), then select Open IP Catalog.

![Figure 1-20: Initial Window, Vivado Design Suite](image)

3. When the Create a New Customized IP Location dialog window opens (not shown), click Next.
4. In the Manage IP Settings window, select a part by clicking the (...) button next to the Part field. A Select Device window pops up. Use the drop-down menu items to narrow the choices. Select the xc7vx485tffg1761-3 device (Figure 1-21). Click OK.

5. Back on the Manage IP Settings window, select Verilog for Target language, Vivado Simulator for Target simulator, Mixed for Simulator language, and a directory to save
the customized IP (Figure 1-22). Click **Finish**.
6. In the Vivado IP Catalog window, open the **Debug & Verification** folder, then open the **Debug** folder, and double-click **IBERT 7 Series GTX** (Figure 1-23).

![Figure 1-23: IP Catalog](image-url)
7. A Customize IP window opens. In the Protocol Definition tab, change **LineRate (Gbps)** to **12.5**, then use the drop-down to change the **Refclk (MHz)** to **156.250**. Do not change the other defaults (Figure 1-24).

*Figure 1-24: Customize IP - Protocol Definition*
8. In the Protocol Selection tab, select **Custom 1 / 12.5 Gbps** in the drop-down menu under Protocol Selected next to QUAD_113, and select **MGTREFCLK1 113** in the Refclk Selection drop-down menu (Figure 1-25).

![Customize IP - Protocol Selection](image)

**Figure 1-25:** Customize IP - Protocol Selection
9. In the Clock Settings tab, select **DIFF SSTL15** for the I/O Standard, enter **E19** for P Package Pin and **E18** for N Package Pin (the FPGA pins that the system clock connects to), and make sure the Frequency is set to **200.00** (Figure 1-26). Press **OK**. A Generate Output Products window opens. Leave the defaults unchanged, and press **Generate**.

![Figure 1-26: Customize IP - Clock Settings](UG847_c1_26_100813)
10. Back to Manage IP, in the Sources window, right-click the IBERT IP and select **Open IP Example Design** (Figure 1-27). Specify a location to save the design, press **OK**, and the design opens in a new Vivado design tools window.

---

**Figure 1-27:** Open IP Example Design
11. In the new window, select **Tools > Run Tcl Script**. In the Run Script window, navigate to `add_scm2.tcl` in the extracted files and press **OK**. The SuperClock-2 Module Design Sources and Constraints are automatically added to the example design (Figure 1-28).

![Project Manager](image)

**Figure 1-28:** Sources after Running add_scm2.tcl

12. The SuperClock-2 source code now needs to be added to the example ibert wrapper. Double-click `example_ibert_7series_gtx_0` in the Design Sources to open the verilog code. Add the top level ports from `top_scm2.v` to the module declaration and instantiate the `top_scm2` module in the example ibert wrapper (Figure 1-29). Click **File > Save File**.
Creating the GTX IBERT Core

Figure 1-29: SuperClock-2 in the Example IBERT Wrapper
13. In the Sources window, Design Sources should now reflect that the SuperClock-2 module is part of the example IBERT design (Figure 1-30).

![Design Sources File Hierarchy](image)

*Figure 1-30: Design Sources File Hierarchy*

14. Click **Run Synthesis** in the Flow Navigator, which synthesizes the design.
15. When synthesis is done, a Synthesis Complete window pops up. Select **Open Synthesized Design** and click **OK** (Figure 1-31).
16. When the Synthesized Design opens, select `dbg_hub` in the Netlist window, then select the **Debug Core Options** tab in the Cell Properties window and change `C_USER_SCANCHAIN*` to 2 (Figure 1-32). Click File > Save Constraints.

![Debug Core Options for dbg_hub](image)

**Figure 1-32:** Debug Core Options for dbg_hub
17. In the Flow Navigator under Program and Debug, click **Generate Bitstream** (Figure 1-33). A window pops up asking if it is ok to launch implementation. Click **Yes**.

![Flow Navigator Screenshot](image)

**Figure 1-33:** Generate Bitstream

18. When implementation completes, navigate to the project directory and locate the resultant bitstream here: 
   `\ibert_7series_gtx_0\example_project\ibert_7series_gtx_0_example\ibert_7series_gtx_0_example.runs\impl_1\`. 
Appendix A

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

For continual updates, add the Answer Record to your myAlerts.

For definitions and terms, see the Xilinx Glossary.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Further Resources

The most up to date information related to the VC7203 kit and its documentation is available on these websites.

- Virtex-7 FPGA VC7203 Characterization Kit
- Virtex-7 FPGA VC7203 Characterization Kit documentation
- Virtex-7 FPGA VC7203 Characterization Master Answer Record (AR 52383)

These Xilinx documents and sites provide supplemental material useful with this guide:

1. UG957, VC7203 Virtex-7 FPGA GTX Transceiver Characterization Board User Guide
2. UG770, HW-CLK-101-SCLK2 SuperClock-2 Module User Guide
Appendix B

Warranty

THIS LIMITED WARRANTY applies solely to standard hardware development boards and standard hardware programming cables manufactured by or on behalf of Xilinx (“Development Systems”). Subject to the limitations herein, Xilinx warrants that Development Systems, when delivered by Xilinx or its authorized distributor, for ninety (90) days following the delivery date, will be free from defects in material and workmanship and will substantially conform to Xilinx publicly available specifications for such products in effect at the time of delivery. This limited warranty excludes: (i) engineering samples or beta versions of Development Systems (which are provided “AS IS” without warranty); (ii) design defects or errors known as “errata”; (iii) Development Systems procured through unauthorized third parties; and (iv) Development Systems that have been subject to misuse, mishandling, accident, alteration, neglect, unauthorized repair or installation. Furthermore, this limited warranty shall not apply to the use of covered products in an application or environment that is not within Xilinx specifications or in the event of any act, error, neglect or default of Customer. For any breach by Xilinx of this limited warranty, the exclusive remedy of Customer and the sole liability of Xilinx shall be, at the option of Xilinx, to replace or repair the affected products, or to refund to Customer the price of the affected products. The availability of replacement products is subject to product discontinuation policies at Xilinx. Customer may not return product without first obtaining a customer return material authorization (RMA) number from Xilinx.

THE WARRANTIES SET FORTH HEREIN ARE EXCLUSIVE. XILINX DISCLAIMS ALL OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED OR STATUTORY, INCLUDING, WITHOUT LIMITATION, ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT, AND ANY WARRANTY THAT MAY ARISE FROM COURSE OF DEALING, COURSE OF PERFORMANCE, OR USAGE OF TRADE. (2008.10)

Do not throw Xilinx products marked with the “crossed out wheeled bin” in the trash. Directive 2002/96/EC on waste electrical and electronic equipment (WEEE) requires the separate collection of WEEE. Your cooperation is essential in ensuring the proper management of WEEE and the protection of the environment and human health from potential effects arising from the presence of hazardous substances in WEEE. Return the marked products to Xilinx for proper disposal. Further information and instructions for free-of-charge return available at: www.xilinx.com/ehs/weee.htm.