

This document describes known issues for the ML605 evaluation board.

General Issues

A summary of known issues related to Xilinx tools, IP, and other issues related to the ML605 Evaluation Kit is provided by

[AR #34836](#), *Virtex-6 FPGA ML605 Evaluation Kit - Known Issues and Release Notes*.

Revision D ML605 evaluation board assemblies use XC6VLX240T-1FFG1156 devices and are affected by errata depending on assembly number:

- Boards having assembly number 0431540 are affected by the silicon errata associated with Virtex-6[®] FPGA LXT CES devices. See [EN101](#), *Virtex-6 FPGA LX760, LX550T, LX365T, LX240T, LX195T, LX130T, SX475T, and SX315T CES Errata*.
- Boards having assembly number 0431622 are affected by the silicon errata associated with Virtex-6 FPGA LXT production devices. See [EN154](#), *Virtex-6 FPGA -1L Speed Grade LX75T, LX130T, LX195T, LX240T, LX365T, LX550T, LX760, SX315T, and SX475T Production Errata*.

The FMC LVDS clock fan-out ICs U82 and U83 are missing 100 Ω differential termination resistors on the FMC-side pins. These resistors can be installed according to [AR #38786](#), *ML605 Differential termination might be needed on fanout buffer*.

The I²C LPC interface pull-up resistors on nets FMC_LPC_IIC_SDA_LS and FMC_LPC_IIC_SDC_LS that connect to Q26 and Q27 are omitted on revision D ML605 evaluation board assemblies. These pull-up resistors can be installed according to [AR #34385](#), *ML605 IIC pull-ups needed when using FMC card*.

PCB Issues

There are no known issues associated with the ML605 printed circuit board (PCB).

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
10/20/09	1.0	Initial Xilinx release.
10/03/11	2.0	Converted document to the current template. Revised or removed the use of "ML605 printed circuit board" to be more specific when referring to the "ML605 evaluation kit" and the "ML605 evaluation board assembly." Updated document to cover ML605 revision D evaluation boards.

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