Intermittent Synch Word - XC18V00

CA2003-08 (v1.1) March 11, 2004 Customer Advisory

Overview

The purpose of this memo is to inform you that XC18V00 devices with the topmark “ART” are sensitive to noise when operated outside of the data sheet specification.

Description

When operated outside of the data sheet specification (DS026), the following two conditions can cause the internal address counter to be corrupted, thus preventing the FPGA from configuring properly:

1. As specified in the data sheet, an external resistor of 4.7-Kohm (or lower) is required to quickly pull up the FPGA INIT and PROM OE/RESET# signal line. If the FPGA INIT and PROM OE/RESET# signal line rises too slowly, then system noise might corrupt the PROM’s internal address counters, thus keeping the FPGA from configuring properly.
2. As specified in the FPGA data sheet, do not exceed 12-mA sink current on the FPGA DONE pin. Beware of LED driving circuits. Using DONE to drive the LED and the PROM CE# pin directly (un-buffered) exceeds this specification. This also affects the FPGA drive_done option.

Note: the symptoms and fixes are described in detail in errata DS026-E01.

Product Affected

The following parts are affected:

- XC18V512PC20C, XC18V512SO20C, XC18V512VQ44C
- XC18V01PC20C, XC18V01SO20C, XC18V01VQ44C
- XC18V02PC44C, XC18V02VQ44C
- XC18V04PC44C, XC18V04VQ44C

This phenomenon affects only the above part numbers with the topmark “ART” (see examples in Table 1) and specific IDCODES (see Table 2).

Sample topmark for the **44-pin VQFP and PLCC** Packages	Sample topmark for the **20-pin SOIC** Package	Sample topmark for the **20-pin PLCC** Package
		

Table 1 (Examples of Topmarks)

Device	IDCODE
XC18V512	05033093h
XC18V01	05034093h
XC18V02	05035093h
XC18V04	05036093h

Table 2 (IDCODES Affected)

Recommendations

1. Follow the data sheet to ensure that an external 4.7 Kohm (or lower) resistor is connected to the PROM's OE/RESET# pin and the FPGA's INIT pin. Ensure that the FPGA TICCK specification is met (500ns). This translates to a Trise and Tfall time of 500ns for the PROM's OE/RESET# signal.

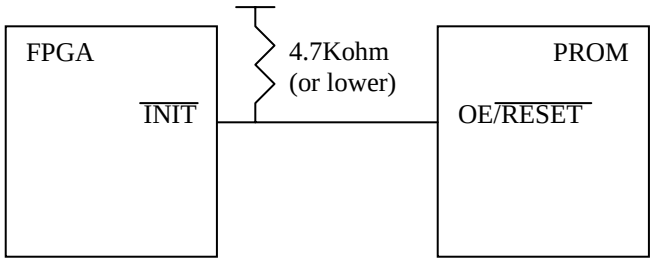

Figure 1 (Recommended Resistor Value)

2. When using FPGA DONE to drive PROM CE# (to reduce standby power), make sure that the signal is within the specification and has a fast rise and fall time. Use an external buffer to drive any LED (Figure 2). If DONE is not used to drive CE#, it can be connected to an LED (Figure 3).

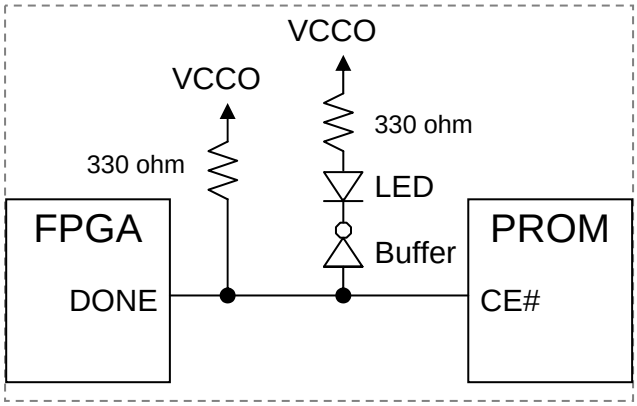

Figure 2 (LED with Buffer Circuit)

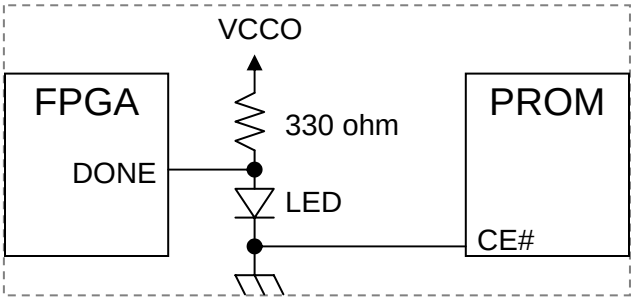

Figure 3 (Un-Buffered LED)

If you have any further questions, please contact your local Xilinx Technical Support.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/16/03	1.0	Initial release.
3/11/04	1.1	Added a reference to an FPGA drive_done option (Description section on page 1) Added a reference to errata DS026-E01 (Description section on page 1) Provided a Trise & Tfall time based on the FPGA TICCK specification (Recommendations section on page 2)