Change to the Maximum CCLK Frequency for Virtex-II SelectMAP mode

PCN2004-03 (v1.2) October 25, 2004 Product/Process Change Notice - FYI

Overview

The purpose of this notification is to communicate a change in the specification of the maximum configuration clock (CCLK) frequency in the SelectMAP mode from 66 MHz to 50 MHz for the Virtex-II™ devices. This change only impacts your design if you are using SelectMAP mode with no handshake for configuration (i.e. your design does not monitor BUSY signal during configuration).

Description

Initially, Xilinx specified in the Virtex-II User Guide (version 1.6.1 and earlier) that the maximum CCLK frequency in all SelectMAP modes was 66 MHz. Based on additional characterization data, Xilinx has changed the maximum CCLK frequency in SelectMAP mode to 50 MHz. **This is a specification change only. There is no change in the silicon or production test program.**

All configuration timing specifications are being moved from the User Guide to the Virtex-II data sheet (Module 3, v3.2 and later).

Product Affected

All Virtex-II devices are affected by this specification change.

Recommendation

In the following cases, no action is required:

a) Your design is not using SelectMAP mode for configuration
b) Your design is using SelectMAP mode with handshake (i.e. monitoring BUSY during configuration)
c) Your design is using SelectMAP mode with no handshake at a CCLK frequency of 50MHz or slower

In the following case, action is required:

a) Your design is using SelectMAP mode with no handshake at a CCLK frequency above 50MHz

For the XC2V40, XC2V80, XC2V250, XC2V500, XC2V1500 and XC2V8000 devices, there is only one option:

1. Reduce CCLK to 50 MHz or below.

For the XC2V1000, XC2V2000, XC2V3000, XC2V4000, and XC2V6000 devices, there are two options:

1. Reduce CCLK to 50 MHz or lower, or
2. If your design does not use CLK2X output as a feedback clock for the DCMs, use SCD0938 to order parts that will support CCLK up to 66 MHz. The SCD code is appended to the standard Xilinx part number for ordering. The SCD number will also be marked on the device. For example: XC2V3000-6FG676C0938.

If your design uses CLK2X output as a feedback clock for the DCMs, your only option is to reduce CCLK to 50 MHz or lower.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
4/12/04	1.0	Initial release.
5/26/04	1.1	Clarified which modes of SelectMAP are impacted by this PCN.
10/25/04	1.2	Revised Module 3 URL to reflect new location.