Bitstream Update Required for Specific Production Spartan-3 FPGAs

XCN05001 (v1.0) January 17, 2005 Quality Alert

Overview

The purpose of this notification is to communicate a required update to the configuration bitstreams for the Spartan-3™ FPGAs. Please update all XC3S50, XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000 FPGA configuration bitstreams using the Xilinx ISE 6.3i, Service Pack 1 or later software release.

The timing and functional operation of the FPGA user application are not affected by this change. No re-simulation or timing analysis of the FPGA user application is required due to this bitstream change.

Description

Spartan-3 block RAM internal timing is controlled by settings in the FPGA configuration bitstream. Through yield analysis, new optimal bitstream settings were identified for specific Spartan-3 device types. These new settings improve the block RAM internal timing margin, which consequently improves overall product yield and availability. **These new settings do not affect any timing in the FPGA application**, only internal timing relationships within the block RAM. The specific improved internal block RAM timing path is the relationship between the write-enable timing and the input latch-enable timing.

These new bitstream settings are now the default settings starting with Xilinx ISE 6.3i, Service Package 1 or later, available for download from the Xilinx web site after September 13, 2004. Specific Spartan-3 FPGA device types, as shown in Table 2, are tested to these new bitstream settings beginning with date code "0433", corresponding to the week beginning August 8, 2004. **Please regenerate any Spartan-3 FPGA configuration bitstreams** created using software versions prior to Xilinx ISE 6.3i development software, Service Pack 1. By updating the bitstream, the application can use any existing or future production Spartan-3 FPGA device. Reference Answer Record 19825 for additional information:

http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=19825

Previous/Updated Bitstream Interaction

Table 1 shows the interaction of both the previous bitstream settings and the new updated bitstream settings for each Spartan-3 FPGA device type. The XC3S200 and XC3S400 were previously released to production and do not require the bitstream update, regardless of the date code marking.

All other devices with markings before date code "0433" can use either the previous or the new updated bitstream settings. Devices other than the XC3S200 and XC3S400 marked with date code "0433" or later require the updated bitstream.

Table 1: **Spartan-3 FPGAs Affected by This Customer Advisory**

Device Type	Date Code	
	Before "0433"	"0433" or Later
XC3S200 XC3S400	Accepts either previous or updated bitstream	Accepts either previous or updated bitstream
XC3S50 XC3S1000 XC3S1500 XC3S2000 XC3S4000 XC3S5000	Accepts either previous or updated bitstream	Requires updated bitstream

The bitstream update does not affect the timing of the user application, only internal timing within the block RAM. The XC3S200, the XC3S400, and the other Spartan-3 FPGAs with date codes prior to "0433" are tested to the previous, overly conservative bitstream settings. These devices accept either the previous or the updated bitstream.

All production Spartan-3 FPGAs, except the XC3S200 and XC3S400, are tested to the new bitstream settings starting with date codes "0433" and later.

Design Software Requirements

The Xilinx ISE 6.3i, Service Pack 1 (SP1) software generates the correct updated bitstreams described in this notice. Xilinx ISE 6.3i, Service Pack 1 (SP1), or later (updates are available at the following web link)

www.xilinx.com/xlnx/xil_sw_updates_home.jsp

Products Affected

This notification only applies to the Spartan-3 FPGAs indicated in Table 2. However, **Xilinx recommends updating the bitstream for all Spartan-3 FPGAs** using the Xilinx ISE 6.3i, Service Pack 1 software or later. Bitstreams for the XC3S200 and XC3S400 are not affected by this change. By updating the bitstream, the application can use any existing or future Spartan-3 FPGA device.

Only designs using block RAM in the XC3S50, XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000 with date codes later than "0433" are affected. The XC3S200 and XC3S400 FPGAs are not affected by this advisory as they were previous released to production, but can be updated without any adverse affect.

Table 2: **Spartan-3 FPGAs Affected by This Customer Advisory**

Device Types:	XC3S50, XC3S1000, XC3S1500, XC3S2000, XC3S4000, XC3S5000
Packages:	All
Speed Grades:	All
Temperature Ranges:	All
Date Codes:	Parts marked with date code "0433" or later (greater). See Figure 1.
Lot Codes:	All

Traceability

Figure 1 shows an example top marking for a Spartan-3 FPGA. The relevant fields to identify an affected device are highlighted and include the **Device Type** and the **Date Code**.

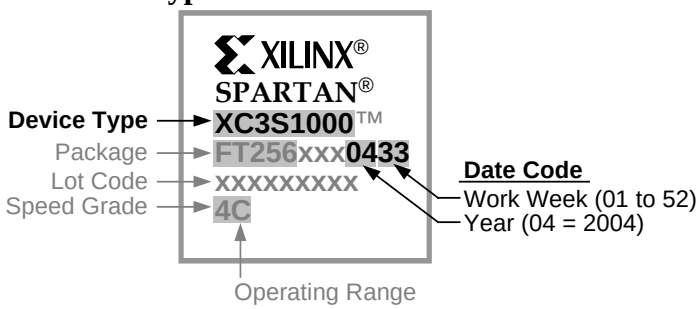

Figure 1: **Example Spartan-3 Package Markings**

Recommendations

Xilinx recommends updating the bitstream for all Spartan-3 FPGAs using the Xilinx ISE 6.3i, Service Pack 1 software or later. By updating the bitstream, the application can use any existing or future Spartan-3 FPGA device.

The update, however, is not absolutely mandated for all applications. Figure 2 diagrams the decision process on whether a bitstream update is required for a specific Spartan-3 FPGA. No update is required for XC3S200 or XC3S400 FPGAs. Similarly, if the FPGA application does not use block RAM, a bitstream update is not required but is recommended for future consistency. Likewise, if the FPGA is not an XC3S200 or XC3S400 but has a date code prior to—*i.e.*, less than—"0433", then an update is recommended, but not required. Finally, all XC3S50, XC3S1000, XC3S1500, XC3S2000, XC3S4000, and XC3S5000 FPGA applications that use block RAM and have or may have a date code of "0433" or later do require the bitstream update.

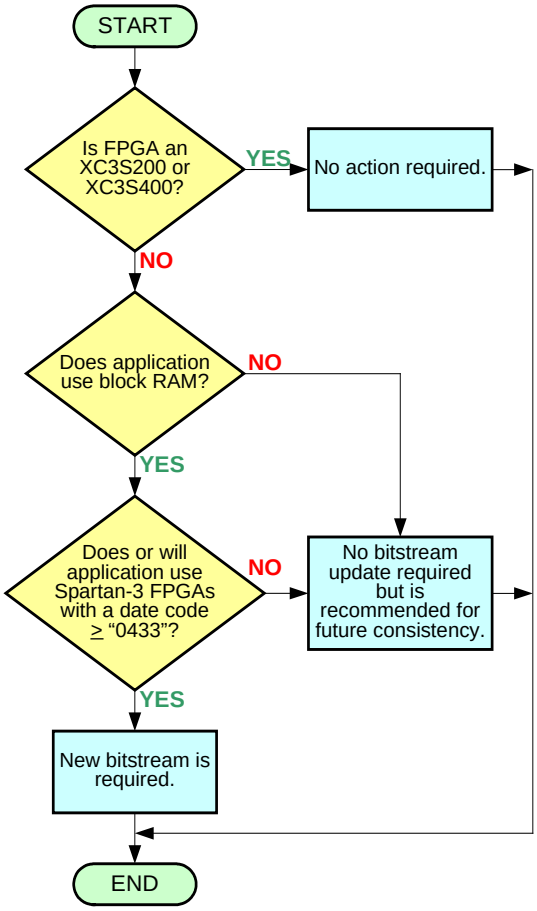

Figure 2: **Spartan-3 Bitstream Update Decision Diagram.**

For additional information or questions, please contact Xilinx Technical Support.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
1/17/05	1.0	Initial release of document.