Spartan™-IIE and Spartan-3 FTG256 Pb-Free Moisture Sensitivity Level Change

XCN06003 (v1.0) January 30, 2006 Quality Alert

Overview

The recent Moisture Sensitivity Level (MSL) quality monitors have shown that certain devices in the Pb-free FTG256 package do not consistently pass Level 3 Pb-free moisture reflow conditions. Certain package substrate lots used in these devices are not passing to Level 3. Therefore, as a temporary precaution, the MSL on these devices is being changed from Level 3 to Level 5 per JEDEC STD-020C.

Description

Moisture-induced delamination failures on certain XC2S50E, XC2S100E, XC2S150E, XC2S200E, XC2S300E, XC3S200, and XC3S1000 lots, all in the FTG256 package, have been observed by Xilinx after Level 3 pre-conditioning monitoring. This monitoring is per JEDEC STD-020C conditions (192 hours of moisture soaking at 30°C / 60% RH followed by 3X IR Reflow at the Pb-free peak reflow temperature of 260°C). These failures are due to delamination of the package in the die attach cavity region (solder mask to gold delamination). Previous Xilinx qualification and reliability monitors on these devices have not exhibited this failure. The possibility of a substrate process excursion is being investigated. As a precaution, until a resolution is found, Xilinx is downgrading these products to Level 5.

If Xilinx Customers take this device out of the moisture barrier bag for the full Level 3 bag open time (168 hours) before board mount, there may be a risk of board mounting failures due to moisture popcorning. Xilinx reliability testing (consisting of Level 3 pre-conditioning + 1000 condition B temperature cycles) has found that the delamination will not worsen after pre-conditioning. Therefore, parts that have already been assembled onto customer boards are not affected by this Quality Alert. Xilinx is also actively working to restore these devices to their previous Level 3 rating. Table 1 shows the date codes estimating when these products will return to being classified as Level 3.

Products Affected

Table 1: **Products Affected**

Device	Package	Family	Estimated Date Code to Revert Back to Level 3
XC2S50E	FTG256	Spartan-IIE	0609
XC2S100E	FTG256	Spartan-IIE	0609
XC2S150E	FTG256	Spartan-IIE	0609
XC2S200E	FTG256	Spartan-IIE	0609
XC2S300E	FTG256	Spartan-IIE	TBD
XC3S200	FTG256	Spartan-3	0609
XC3S1000	FTG256	Spartan-3	0621

Traceability

The date code traceability for conversion back to Level 3 per Table 1 can be found on the package top mark. Figure 1 illustrates an example of the top mark.

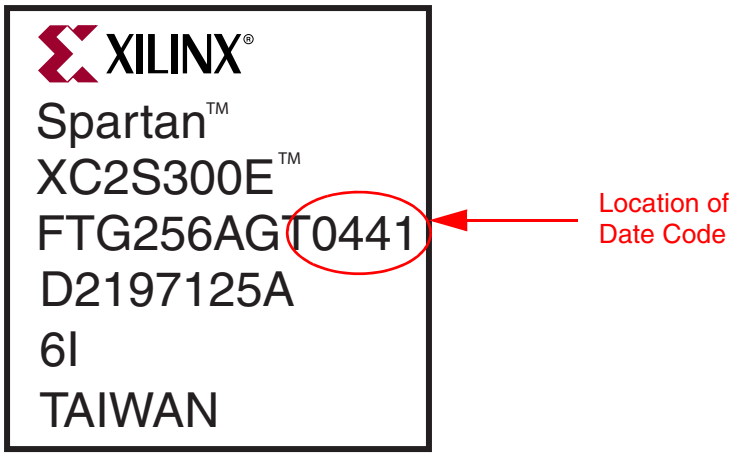

Figure 1: **Example Package Top Mark**

Recommendations

Xilinx recommends the following lot disposition:

1. Mount the devices on PCB boards within 48 hours after moisture barrier bags are opened (refer to JEDEC-STD-020C).
2. If devices are exposed to air for more than 48 hours, bake at 125°C for a minimum of eight hours prior to board mounting.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
1/30/06	1.0	Initial Xilinx release.