7 Series FPGA and Zynq-7000 AP SoC I/O Undershoot Voltage Data Sheet Update

XCN14014 (v1.0) June 2, 2014 **Product Change Notice - For Information Only**

Overview

The purpose of this notification is to inform you of a revision to undershoot threshold for inputs for 1.8V HP I/O, 3.3V HR I/O, PL I/O, and PS I/O banks for all Xilinx® 7 series FPGAs and Zynq®-7000 All Programmable SoCs.

Description

The undershoot and overshoot thresholds for inputs for 1.8V HP I/O, 3.3V HR I/O, PL I/O, and PS I/O banks are described in Note (2) of "**VIN Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks,**" "**VIN Maximum Allowed AC Voltage Overshoot and Undershoot for PL 1.8V HP I/O Banks,**" "**VIN Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks,**" and **"VIN Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O and 3.3V HR I/O Banks"** tables. Undershoot occurs when an input is below the undershoot threshold and overshoot occurs when an input is above the overshoot threshold. For all 7 series FPGAs and Zynq-7000 AP SoC devices, the undershoot threshold for inputs is changing from GND – 0.30V to GND – 0.20V. The note is revised as Table 1 and Table 2 for the affected products:

Table 1: Revision of undershoot threshold for inputs in 1.8V HP I/O, 3.3V HR I/O, PL I/O, and PS I/O banks for Artix®-7, Kintex®-7, Virtex®-7T/-7XT, Zynq-7000 AP SoC (Z-7030, Z-7045, and Z-7100) devices:

Prior Note	Revised Note
The peak voltage of the overshoot or undershoot, and the duration above V_{CCO} + 0.20V or below **GND – 0.30V**, must not exceed the values in this table.	The peak voltage of the overshoot or undershoot, and the duration above V_{CCO} + 0.20V or below **GND – 0.20V**, must not exceed the values in this table.

The revision shown in Table 1 appears in the following data sheets on, or after, June 2, 2014:
DS181, *Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics*
DS182, *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics*
DS183, *Virtex-7 T and XT FPGAs Data Sheet: DC and AC Switching Characteristics*
DS191, *Zynq-7000 All Programmable SoC (Z-7030, Z-7045, and Z-7100): DC and AC Switching Characteristics*

Table 2: Revision of undershoot threshold for inputs in PS I/O and 3.3V HR I/O banks for Zynq-7000 AP SoC (Z-7010, Z-7015, and Z-7020) devices:

Prior Note	Revised Note
The peak voltage of the overshoot or undershoot, and the duration above V_{CCO} + 5% or below **GND – 0.30V**, must not exceed the values in this table.	The peak voltage of the overshoot or undershoot, and the duration above V_{CCO} + 0.20V or below **GND – 0.20V**, must not exceed the values in this table.

The revision shown in Table 2 appears in the following data sheet on, or after, June 2, 2014:
DS187, *Zynq-7000 All Programmable SoC (Z-7010, Z-7015, and Z-7020): DC and AC Switching Characteristics*

Products Affected

This change affects all speed, package, temperature, and SCD variations of the Commercial (C), Industrial (I) grade, Automotive (XA), and Defense-grade (XQ) devices. Affected part numbers are included in the Table 3:

Table 3: **Affected Devices**

Xilinx Product	Affected by This Revision
All Zynq-7000 AP SoCs	Yes
All 7 series FPGAs	Yes

Response

No response is required. For additional information or questions, please contact Xilinx Technical Support.

Important Notice: Xilinx Customer Notifications (XCNs, XDNs, and Quality Alerts) can be delivered via e-mail alerts sent by the Support website (http://www.xilinx.com/support). Register today and personalize your "Documentation and Design Advisory Alerts" area to include Customer Notifications. Xilinx Support provides many benefits, including the ability to receive alerts for new and updated information about specific products, as well as alerts for other publications such as data sheets, errata, application notes, etc. For information on how to sign up, refer to Answer Record 18683: http://www.xilinx.com/support/answers/18683.htm.

Additional Documentation

DS181, *Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics*
http://www.xilinx.com/support/documentation/data_sheets/ds181_Artix_7_Data_Sheet.pdf

DS182, *Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics*
http://www.xilinx.com/support/documentation/data_sheets/ds182_Kintex_7_Data_Sheet.pdf

DS183, *Virtex-7 T and XT FPGAs Data Sheet: DC and AC Switching Characteristics*
http://www.xilinx.com/support/documentation/data_sheets/ds183_Virtex_7_Data_Sheet.pdf

DS187, *Zynq-7000 All Programmable SoC (Z-7010, Z-7015, and Z-7020): DC and AC Switching Characteristics*
http://www.xilinx.com/support/documentation/data_sheets/ds187-XC7Z010-XC7Z020-Data-Sheet.pdf

DS191, *Zynq-7000 All Programmable SoC (Z-7030, Z-7045, and Z-7100): DC and AC Switching Characteristics*
http://www.xilinx.com/support/documentation/data_sheets/ds191-XC7Z030-XC7Z045-data-sheet.pdf

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/02/2014	1.0	Initial release.

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