FAQ: Implications of XCN07026

XTP030 (v1.1) June 15, 2009

Q1. What are the differences between Step 0 and Step 1 devices?

A. There are no functional differences between Step 0 and Step 1 devices. The only change in Step 1 devices is the improvement of CDM ESD performance for GTP I/O pins. Step 1 devices are form, fit, function, and bit-stream compatible with Step 0.

Q2. What is the ESD improvement in Step 1 devices?

A. The ESD and Latch-up data in the current Device Reliability Report (UG116) captures the improvement resulting from this change. The first version of the document to capture this enhancement is v4.3, published on February 6, 2008: http://www.xilinx.com/support/documentation/user_guides/ug116.pdf.

Q3. The XC5VLX220T and XC5VLX330T devices are not listed in the PCN. Are these devices not transitioning to Step 1?

A. The XC5VLX220T and XC5VLX330T devices went to production with Step 1 initially. There is no production Step 0 for these devices.

Q4. Has there been any Step 1 device shipped with the standard ordering part number so far?

A. Except for the XC5VLX220T and XC5VLX330T devices, all orders with standard ordering codes were, and will be shipped with the Step 0 devices until April 30, 2008. After April 30, 2008, orders for standard ordering codes will be shipped with either Step 0 or Step 1 devices (except for XC5VLX220T and XC5VLX330T, which only ship with Step 1 mask sets).

Q5. If I want Step 1 devices alone, what ordering code should be used?

A. Step 1 devices can be ordered by appending “S1” to the end of the standard ordering code. The S1 ordering code also means you will receive a device in a 10-layer package.

Q6. What should CONFIG STEPPING be set to for Step 1 devices?

A. CONFIG STEPPING should be set to 0 (same as for Step 0 devices). If CONFIG STEPPING is not set, the software defaults to 0.

Q7. Can I specify Step 0 devices?

A. No. Xilinx will transition completely to Step 1 devices. There will be no ordering code for Step 0 devices only.

Q8. Why is Xilinx standardizing to 10-layer for Virtex-5 packages with more than 1000 pins?

A. With FPGA I/O interface performance, signal count, and density continuing to increase, signal integrity demands on FPGA packages (especially larger packages) have increased as well. Recognizing these increasing demands, Xilinx has decided to enhance our large (>1000 pins) Virtex®-5 packages with two additional layers to further improve I/O noise margin.

Q9. What are the differences between the 8-layer and 10-layer packages?

A. The 10-layer package has one additional V_{CCO} layer and one additional GND layer. There has been no change to the signal routing, V_{CCINT} or V_{CCAUX} structures in the package. Due to the addition of two layers, the 10-layer substrate thickness is increased by 0.1mm. Both the 8-layer and 10-layer meet the maximum package outline height specification.

Q10. What is the effect in performance, power, or thermal characteristics?

A. There is no negative impact to any of these characteristics.

Q11. The migration from 8-layer to 10-layer packages must result in different package pin delay and skew figures. How is the package skew affected in the new packages?

A. There is no pin delay impact; consequently, there is no additional skew due to the package layer count change. The conversion from 8-layer to 10-layer did not involve any I/O signal routing changes, because the two added layers are power/ground plane layers. I/O signal routing lengths and pin delay remain the same as before.

Q12. Do you have the qualification data for the new package?

A. The qualification report (RPT091) for the new 10-layer flip-chip package substrate for Virtex-5 is available at: Qualification of 10-Layer Flip-Chip Package Substrate for Virtex-5 (RPT091)

Q13. The LX220T and LX330T have packages with more than 1000 pins, but they are not listed in the PCNs. Are they not transitioning to 10-layer packages?

A. The LX220T and LX330T were qualified with both 8-layer and 10-layer packages before going into production. Those devices are shipping with either the 8-layer or 10-layer packages since their Production release in October 2007.

Q14. Is there any associated or increased risk in continuing to use the 8-layer package in Production designs?

A. No. All Virtex-5 packages have been carefully designed to reduce cost and complexity for the user, while still delivering excellent electrical properties. For example, the 8-layer (and 10-layer) packages include a wideband decoupling network and group power pins in clusters to ease board-level power distribution. Previous device families (Virtex-4, Virtex-II Pro, etc.) required an extensive PCB decoupling network as package capacitors could only cover a limited frequency range. Virtex-5 is the first device family that contains a wideband decoupling network inside the package. Since only bulk low-frequency capacitors are required at the PCB level, there are fewer PCB decoupling capacitors, with little restriction on capacitor placement and performance. The Virtex-5 pin-out was carefully designed to cluster similar supply pins into consolidated groups. This makes it possible to reach the vias of all power pins of a given supply with only a small V_{CC} planelet. The shapes of these planelets can fit into one another, which was not possible in older device families. What would have required 3 V_{CC} layers in another device can be done with only 1 or 2 V_{CC} layers in a Virtex-5 package.

Q15. Do I have the option to order 8-layer packages only?

A. No. After April 30, 2008, Xilinx will ship either 8-layer or 10-layer packages. There will be no separate ordering code for 8-layer packages.

Q16. Do I need to specifically order 10-layer packages alone?

A. No. Xilinx expects that the current packages would work well for most applications. The new 10-layer packages only benefit limited applications where extra noise margin is required. The qualification report on the new 10-layer package is available at: Qualification of 10-Layer Flip-Chip Package Substrate for Virtex-5 (RPT091).

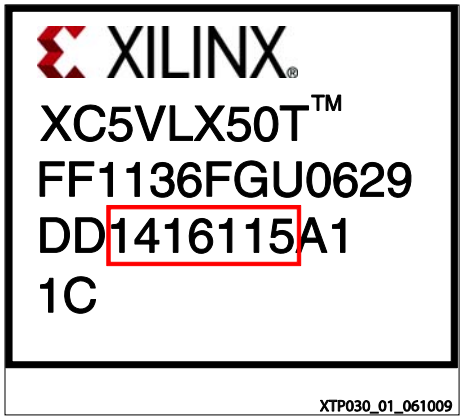
Q17. Has there been any 10-layer devices shipped with the standard ordering part number so far?

A. Except for the LX220T and LX330T devices, all orders for standard ordering parts are shipped using 8-layer packages until April 30, 2008. After April 30, 2008 (following the XCN07026 transition period), orders for standard ordering parts will be shipped with either 8-layer or 10-layer packages. For LXT and SXT devices, orders for standard ordering parts may also be shipped with Step 0 or Step 1 mask set (see XCN07026).

Q18. How do I know whether I have the new 10-layer package?

A. If you ordered a Step 1 device (ordering code “S1” appended to the end of the standard ordering part number), you have a device with a 10 layer package.

B. If you are unsure of the ordering code, to trace the packages in your possession, please contact Xilinx Customer Service at csgroup@xilinx.com, and provide the 7- digit Lot ID (see example top mark below). Xilinx Customer Service can identify if the order was shipped with 8-layer or 10-layer packages.



Q19. I would like to understand whether or not my existing application will benefit from moving to the 10-layer package. Whom should I contact for additional information regarding the 10-layer package construction?

A. For assistance in evaluating the effects of using the 10-layer package in your application, contact Xilinx Technical Support.

Revision History

Date	Version	Revision
03/11/08	1.0	Initial release.
06/15/09	1.1	Edits to ensure these FAQs only refer to XCN07026. Added additional Q8 to Q19 in the document. Corrected the image to include new logo and document date. Added the correct trademark symbol for Virtex-5 in the document. Revised links to RPT091 (links to secure URL) in the document

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