QPro XQR17V16 Radiation Hardened 16Mbit QML Configuration PROM

DS126 (v2.0) July 12, 2018 **Product Specification**

Features

- Latch-Up Immune to LET >120 MeV/cm2/mg
- Guaranteed TID of 50 kRad(Si) per spec 1019.5
- Fabricated on Epitaxial Substrate
- 16Mbit storage capacity
- Guaranteed operation over full military temperature range: –55°C to +125°C
- One-time programmable (OTP) read-only memory designed to store configuration bitstreams of Xilinx FPGA devices
- Dual configuration modes
  - Serial configuration (up to 33 Mb/s)
  - Parallel (up to 264 Mb/s at 33 MHz)
- Simple interface to the Xilinx QPro FPGAs
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- Low-power CMOS floating-gate process
- 3.3V supply voltage
- Available in ceramic CK44 packages(1)
- Programming support by leading programmer manufacturers
- Design support using the ISE Foundation or ISE WebPACK software packages
- Guaranteed 20 year life data retention

Description

Xilinx introduces the high-density QPro™ XQR17V16 series Radiation Hardened QML configuration PROMs which provide an easy-to-use, cost-effective method for storing large Xilinx FPGA configuration bitstreams. The XQR17V16 is a 3.3V device with a storage capacity of 16 Mb and can operate in either a serial or byte-wide mode. See Figure 1 for simplified block diagram of the XQR17V16 device architecture.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after the rising clock edge, data appears on the PROM DATA output pin that is connected to the FPGA DIN pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the PROM. When the FPGA is in Slave Serial mode, the PROM and the FPGA must both be clocked by an incoming signal.

When the FPGA is in Master SelectMAP mode, it generates the configuration clock that drives the PROM and the FPGA. After the rising CCLK edge, data is available on the PROMs DATA (D0-D7) pins. The data will be clocked into the FPGA on the following rising edge of the CCLK. When the FPGA is in Slave SelectMAP mode, the PROM and the FPGA must both be clocked by an incoming signal. A free-running oscillator can be used to drive the CCLK. See Figure 2.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all PROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, either the Xilinx ISE Foundation or ISE WebPACK software compiles the FPGA design file into a standard Hex format, which is then transferred to most commercial PROM programmers.

1. Specific part number and package combinations have been discontinued. Refer to XCN07002 and XCN16002. The CK44 package replaces the CC44 package.

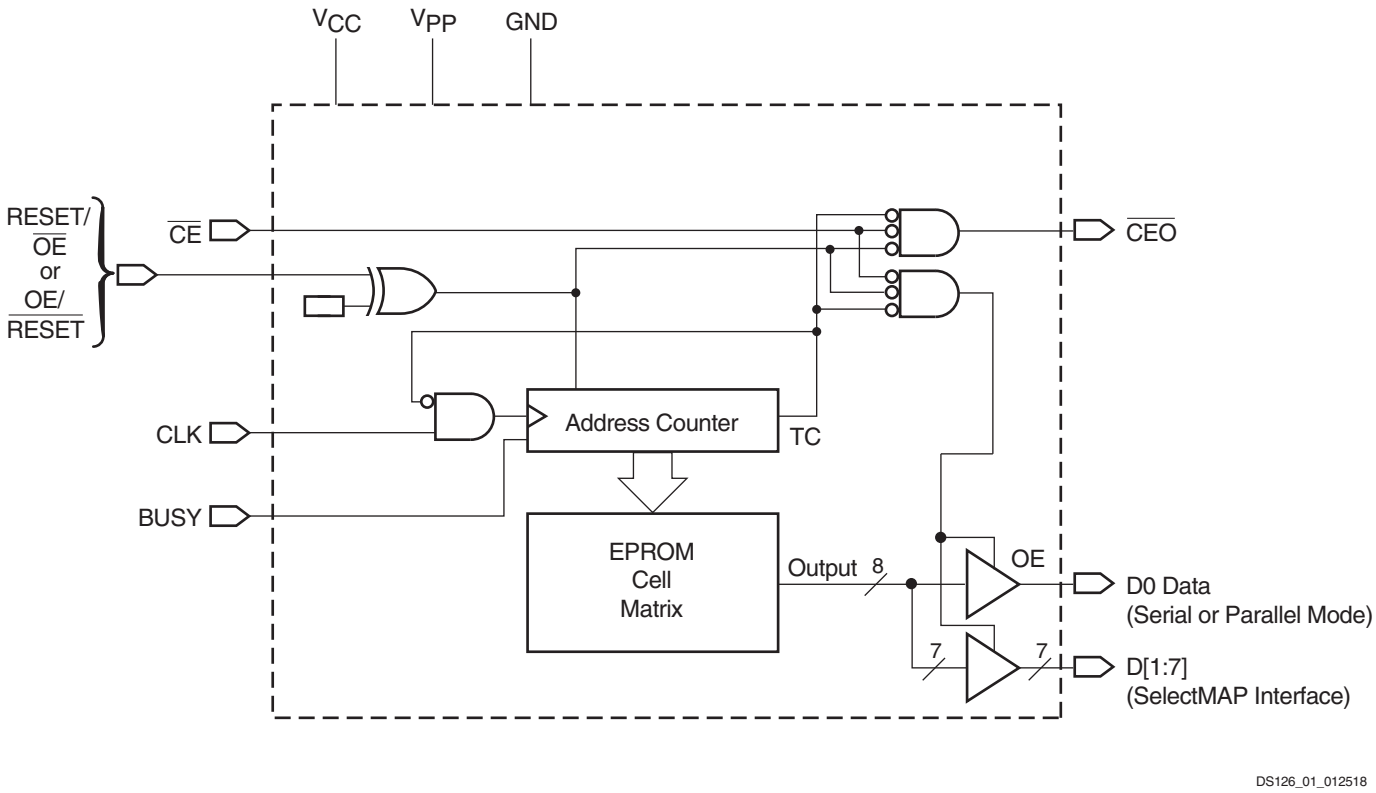


Figure 1: **Simplified Block Diagram for XQR17V16 (does not show programming circuit)**

Pin Description

DATA[0:7]

Data output is in a high-impedance state when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the D0 pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.

CLK

Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.

RESET/$\overline{OE}$

When High, this input holds the address counter reset and puts the DATA output in a high-impedance state. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at "0", and puts the DATA output in a high-impedance state. The device default is active-High RESET, but the preferred option is active-Low $\overline{RESET}$, because it can be connected to the FPGAs INIT pin and a pullup resistor.

The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 Programmer. Third-party programmers have different methods to invert this pin.

$\overline{CE}$

When High, this pin disables the internal address counter, puts the DATA output in a high-impedance state, and forces the device into low-I_{CC} standby mode.

$\overline{CEO}$

Chip Enable output is connected to the $\overline{CE}$ input of the next PROM in the daisy chain. This output is Low when the $\overline{CE}$ and $\overline{OE}$ inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. In other words: when the PROM has been read, $\overline{CEO}$ will follow $\overline{CE}$ as long as $\overline{OE}$ is active. When blah goes inactive, $\overline{CEO}$ stays High until the PROM is reset. Note that $\overline{OE}$ can be programmed to be either active-High, or active-Low.

BUSY

If the BUSY pin is floating, the user must program the BUSY bit, which will cause the BUSY pin to be internally tied to a pull-down resistor. When asserted High, output data is held, and when the BUSY pin goes Low, data output will resume.

V_{PP}

Programming voltage. No overshoot above the specified maximum voltage is permitted on this pin. For normal read operation, this pin must be connected to V_{CC}. Failure to do so can lead to unpredictable, temperature-dependent operation and severe problems in circuit debugging. Do not leave the V_{PP} floating!

V_{CC} and GND

Positive supply and ground pins.

PROM Pinouts for XQR17V16

(Pins not listed are “no connect”)

Table 1: **Pinouts for XQR17V16(1)**

Pin Name	44-pin CLCC (CK44)
BUSY	30
D0	2
D1	35
D2	4
D3	33
D4	15
D5	31
D6	20
D7	25
CLK	5
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	19
$\overline{CE}$	21
GND	3, 12, 24, 34, 43
$\overline{CEO}$	27
V_{PP}	41
V_{CC}	14, 22, 23, 32, 42, 44

Notes:

1. Specific part number and package combinations have been discontinued. Refer to XCN07002 and XCN16002.

Capacity

Table 2: **Device Capacities(1)**

Devices	Configuration Bits
XQR17V16	16,777,216

Notes:

1. Specific part number and package combinations have been discontinued. Refer to XCN07002 and XCN16002.

Controlling PROMs

Connecting the FPGA device with the PROM.

- The DATA output(s) of the PROM(s) drives the D_{IN} input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s).
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The $\overline{RESET}$/OE input of all PROMs is best driven by the $\overline{INIT}$ output of the lead FPGA device. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch.
- The PROM $\overline{CE}$ input is best connected to the FPGA DONE pin(s) and a pullup resistor. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 15 mA maximum.
- SelectMAP mode is similar to Slave Serial mode. The DATA is clocked out of the PROM one byte per CCLK instead of one bit per CCLK cycle. See FPGA data sheets for special configuration requirements.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. The Xilinx PROMs have been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only one serial data line, two control lines, and one clock line are required to configure an FPGA. Data from the PROM is read sequentially, accessed via the internal address and bit counters, which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function DIN pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. The Xilinx FPGA families take care of this automatically with an on-chip default pull-up/down resistor or keeper circuit.

Cascading Configuration PROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded PROMs provide additional memory. After the last bit from the first PROM is read, the next clock signal to the PROM asserts its $\overline{CEO}$ output Low and disables its DATA line. The second PROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 2.

After configuration is complete, the address counters of all cascaded PROMs are reset if the FPGA $\overline{PROGRAM}$ pin goes Low, assuming the PROM reset polarity option has been inverted.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

Programming

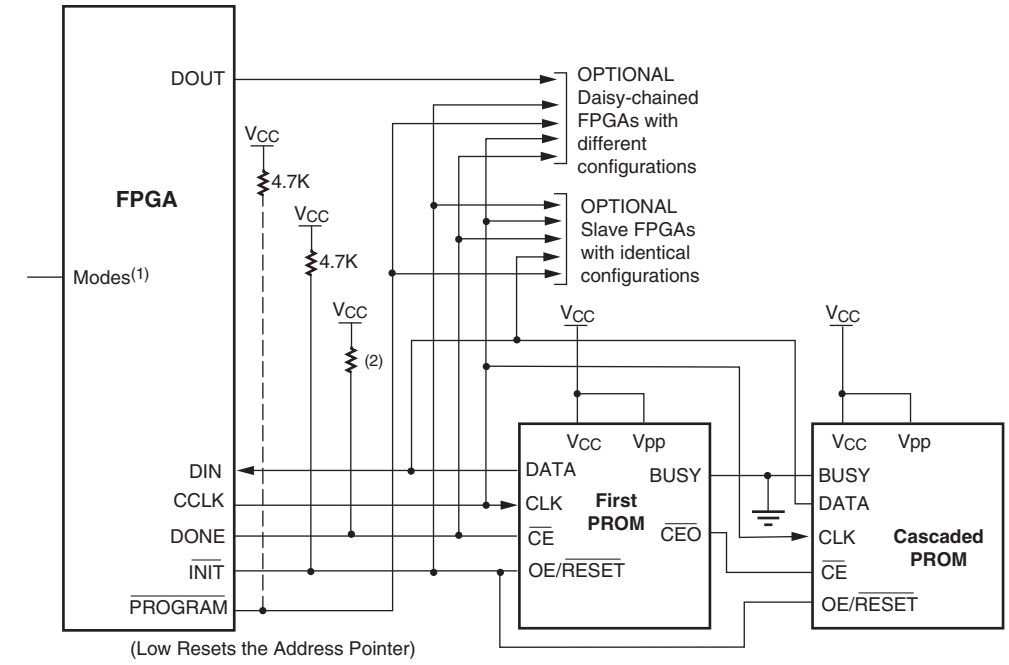
The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

Table 3: **Truth Table for XQR17V16 Control Inputs**

Control Inputs		Internal Address	Outputs		
RESET(1)	**$\overline{CE}$**		**DATA**	**$\overline{CEO}$**	**I_{CC}**
Inactive	Low	If address ≤ TC(2): increment If address > TC(2): don't change	Active High-Z	High Low	Active Reduced
Active	Low	Held reset	High-Z	High	Active
Inactive	High	Not changing	High-Z	High	Standby
Active	High	Held reset	High-Z	High	Standby

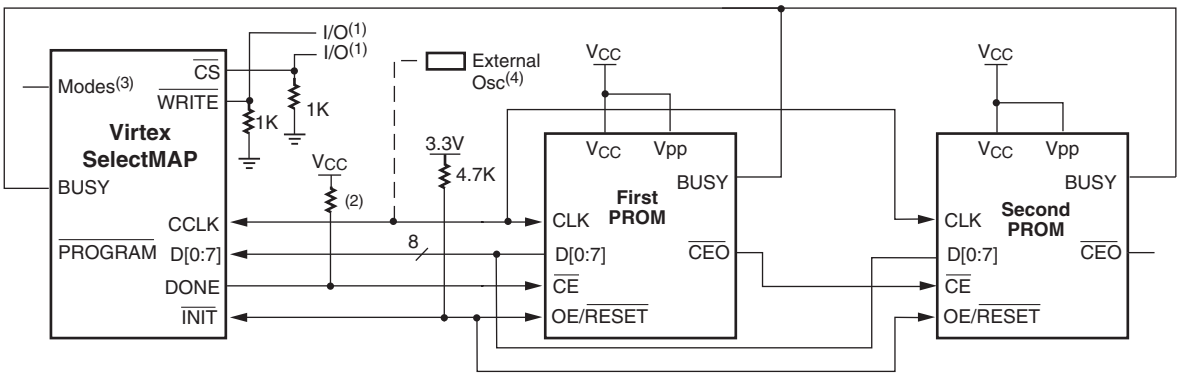
Notes:

1. The XQR17V16 RESET input has programmable polarity
2. TC = terminal count, highest address value.



(1) For Mode pin connections, refer to the appropriate FPGA data sheet.
(2) For specific DONE resistor recommendations, refer to the appropriate FPGA data sheet.

Master Serial Mode



(1) CS and WRITE must be pulled down to be used as I/O. One option is shown.
(2) For specific DONE resistor recommendations, refer to the appropriate FPGA data sheet.
(3) For Mode pin connections, refer to the appropriate FPGA data sheet.
(4) External oscillator required for FPGA slave SelectMAP modes.

Virtex SelectMAP Mode, XQR17V16 only.

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Figure 2: **(a) Master Serial Mode (b) Virtex SelectMAP Mode (dotted lines indicate optional connection)**

Radiation Tolerances

Table 4: **Guaranteed Radiation Tolerance Specifications**

Symbol	Description	Min	Max	Units
TID	Total Ionizing Dose: For data retention and data output port read (configuration) operations	–	50	krad (Si)
SEL	Single Event Latch-Up. (No latch-up observed for LET > 120 MeV-mg/cm^2)	–	0	cm^2
SEU	Static Memory Cell Saturation Bit Cross-Section (No upset observed for LET > 120 MeV-mg/cm^2)	–	0	cm^2

Notes:

1. For more information on dynamic SEU error rates, see the Single Event Upsets page.

Absolute Maximum Ratings

Table 5: **Absolute Maximum Ratings(1)**

Symbol	Description	Conditions	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{PP}	Supply voltage relative to GND	–0.5 to +12.5	V
V_{IN}	Input voltage relative to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to High-Z output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in.)	+260	°C
T_J	Junction temperature	+150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions (3.3V Supply)

Table 6: **Operating Conditions (3.3V Supply)**

Symbol	Description	Min	Max	Units
V_{CC}(1)	Supply voltage relative to GND (T_C = –55°C to +125°C)	3.0	3.6	V
T_{VCC}(2)	V_{CC} rise time from 0V to nominal voltage	1.0	50	ms

Notes:

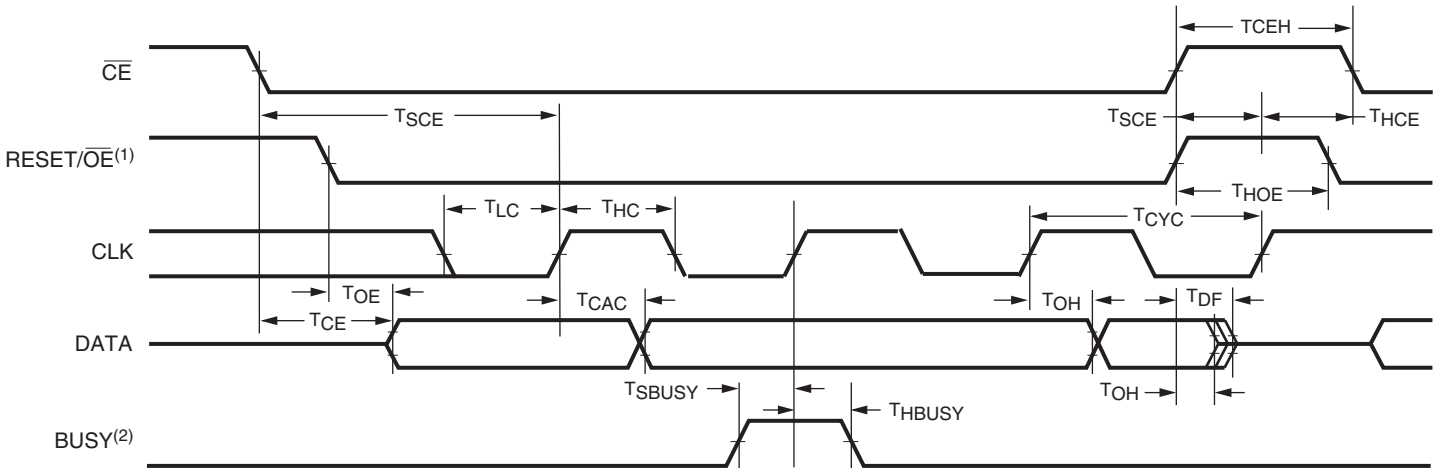
1. During normal read operation V_{PP} ***must*** be connected to V_{CC}.
2. At power up, the device requires the V_{CC} power supply to monotonically rise from 0V to nominal voltage within the specified V_{CC} rise time. If the power supply cannot meet this requirement, then the device may not power-on-reset properly.
3. Specific part number and package combinations have been discontinued. Refer to XCN07002 and XCN16002.

DC Characteristics Over Operating Conditions

Table 7: **DC Characteristics Over Operating Conditions**

Symbol	Description	Min	Max	Units
V_{IH}	High-level input voltage	2	V_{CC}	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –3 mA)	2.4	–	V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)	–	0.4	V
I_{CCA}	Supply current, active mode (at maximum frequency)	–	100	mA
I_{CCS}	Supply current, standby mode	–	1	mA
I_L	Input or output leakage current	–10	10	µA
C_{IN}	Input capacitance (V_{IN} = GND, f = 1.0 MHz)	–	15	pF
C_{OUT}	Output capacitance (V_{IN} = GND, f = 1.0 MHz)	–	15	pF

AC Characteristics over Operating Condition for XQR17V16



Note:
1 The XQR17V16 RESET/OE input polarity is programmable. The RESET/OE input is shown in the timing diagram with active-high RESET polarity. Timing specifications are identical for both polarity settings.
2. If BUSY is inactive (Low) during a rising CLK edge, then new DATA appears at time T_{CAC} after the rising CLK edge. If BUSY is active (High) during a rising CLK edge, then there is no corresponding change to DATA.

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Figure 3: **Timing Diagram for AC Characteristics over Operating Conditions for XQR17V16**

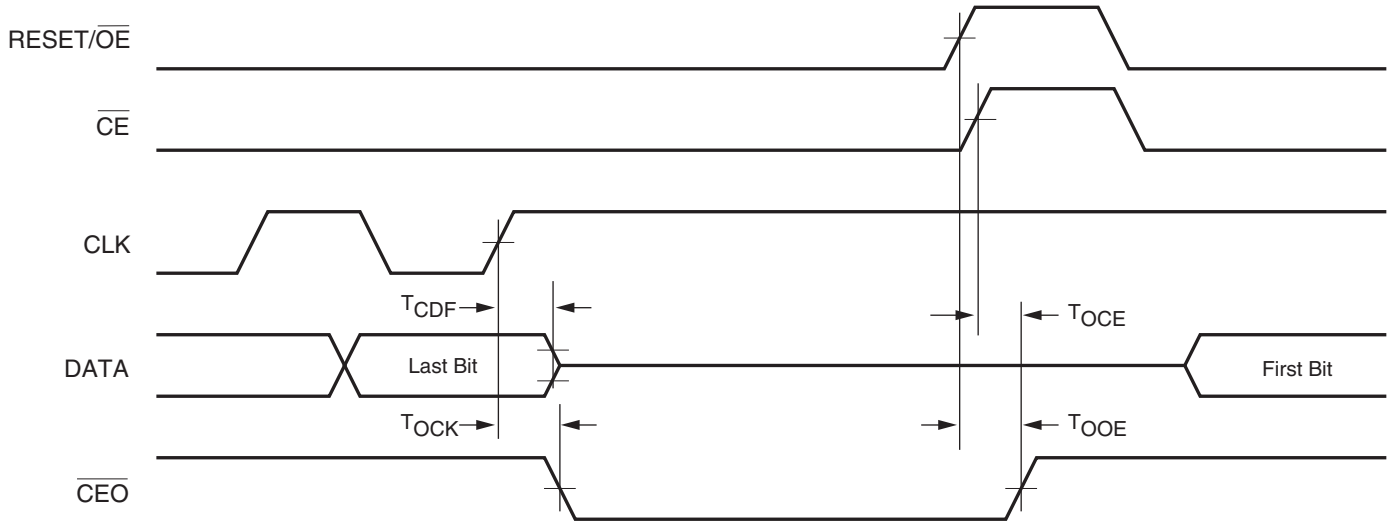
Table 8: **Description of Timing Diagram Symbols**

Symbol	Description	Min	Max	Units
T_{OE}	$\overline{OE}$ to data delay	–	15	ns
T_{CE}	$\overline{CE}$ to data delay	–	20	ns
T_{CAC}	CLK to data delay(2)	–	20	ns
T_{DF}	$\overline{CE}$ or $\overline{OE}$ to data float delay(3,4)	–	35	ns
T_{OH}	Data hold from $\overline{CE}$, $\overline{OE}$, or CLK(4)	0	–	ns
T_{CYC}	Clock periods	50	–	ns
T_{LC}	CLK Low time(4)	25	–	ns
T_{HC}	CLK High time(4)	25	–	ns
T_{SCE}	$\overline{CE}$ setup time to CLK (to guarantee proper counting)	25	–	ns
T_{HCE}	$\overline{CE}$ hold time to CLK (to guarantee proper counting)	0	–	ns
T_{HOE}	$\overline{OE}$ hold time (guarantees counters are reset)	25	–	ns
T_{SBUSY}	BUSY setup time	5	–	ns
T_{HBUSY}	BUSY hold time	5	–	ns
T_{CEH}	$\overline{CE}$ High time (guarantees counters are reset)	20	–	ns

Notes:

1. AC test load = 50 pF.
2. When BUSY = 0.
3. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
4. Guaranteed by design, not tested.
5. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
6. If T_{CEH} High, 2 µs, T_{CE} = 2 µs.
7. If T_{HOE} High, 2 µs, T_{OE} = 2 µs.

AC Characteristics over Operating Condition When Cascading



Notes:
1 The XQR17V16 RESET/OE input polarity is programmable. The RESET/OE input is shown in the timing diagram with active-high RESET polarity. Timing specifications are identical for both polarity settings.
2 The diagram shows timing of the First Bit and Last Bit for one PROM with respect to signals involved in a cascaded situation. The diagram does not show timing of data as one PROM transfers control to the next PROM. The shown timing information must be applied appropriately to each PROM in a cascaded situation to understand the timing of data during the transfer of control from one PROM to the next.

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Figure 4: **Timing Diagram of AC Characteristics over Operating Condition When Cascading**

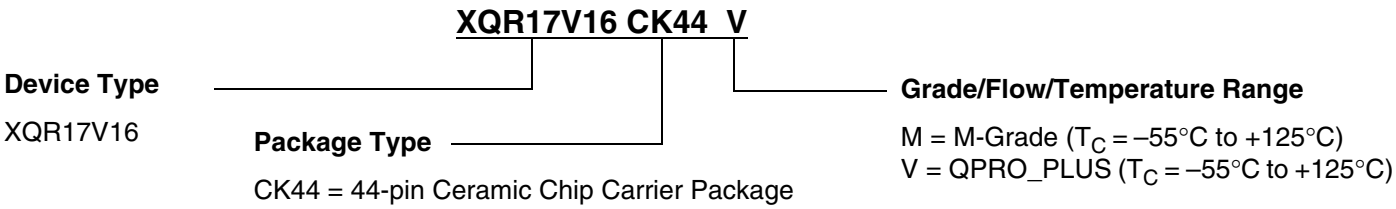
Table 9: **Description of Timing Diagram Symbols (When Cascading)**

Symbol	Description	Min	Max	Units
T_{CDF}	CLK to data float delay(2,3)	–	50	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3)	–	30	ns
T_{OCE}	CE to $\overline{CEO}$ delay(3)	–	35	ns
T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ delay(3)	–	30	ns

Notes:

1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.

Ordering Information



Valid Ordering Combinations

Table 10: **Valid Ordering Combinations**

M Grade	V Grade
XQR17V16CK44M	XQR17V16CK44V

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/12/2018	2.0	Updated to remove the discontinued VQ44 plastic package per XCN07002. Removed the discontinued CC44 ceramic package and added the CK44 package per XCN16002. For clarity, added T_{CEH} to Figure 3 and Notes 1 and 2. Added T_{CEH} and Notes 6 and 7 to Table 8. For clarity, added Notes 1 and 2 to Table 4. Removed the *Device Ordering Options* section and combined the information into the Ordering Information section. Updated the Notice of Disclaimer.
12/15/2003	1.0	Initial Xilinx release.

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