Radiation-Hardened, Space-Grade Virtex-5QV FPGA Data Sheet: DC and AC Switching Characteristics

DS692 (v1.3.1) January 16, 2015

Product Specification

Virtex-5QV FPGA Electrical Characteristics

Radiation-hardened Virtex®-5QV FPGAs are available in the -1 speed grade only. Virtex-5QV FPGA DC and AC characteristics are specified for military temperatures.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical conditions.

This Virtex-5QV FPGA data sheet, part of an overall set of documentation on the Virtex-5 family of FPGAs, is available on the Xilinx website:

- DS192, *Radiation-Hardened, Space-Grade Virtex-5QV Device Overview*
- UG520, *Virtex-5QV FPGA Packaging and Pinout Specification*
- UG190, *Virtex-5 FPGA User Guide*
- UG191, *Virtex-5 FPGA Configuration Guide*
- UG193, *Virtex-5 FPGA XtremeDSP™ Design*
- UG198, *Virtex-5 FPGA RocketIO™ GTX Transceiver User Guide*
- UG194, *Virtex-5 FPGA Tri-Mode Ethernet Media Access Controller User Guide*
- UG197, *Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express® Designs*
- UG203, *Virtex-5 FPGA PCB Designer's Guide*

Virtex-5QV FPGA DC Characteristics

Table 1: **Absolute Maximum Ratings**

Symbol	Description	Value	Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.1	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.75	V
V_{BATT}	Key memory battery backup supply	–0.5 to 4.05	V
V_{REF}	Input reference voltage	–0.5 to 3.75	V
V_{IN}	3.3V I/O input voltage relative to GND(2) (user and dedicated I/Os)	–0.75 to 4.05	V
	2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)	–0.75 to V_{CCO} + 0.5	V
I_{IN}	Current applied to an I/O pin, powered or unpowered	±100	mA
	Total current applied to all I/O pins, powered or unpowered	±100	mA
V_{TS}	Voltage applied to 3-state 3.3V output(2) (user and dedicated I/Os)	–0.75 to 4.05	V
	Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os)	–0.75 to V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C
T_{SOL}	Maximum soldering temperature(3)	+220	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For 3.3V I/O operation, refer to UG190: Virtex-5 FPGA User Guide, Chapter 6, 3.3V I/O Design Guidelines.
3. For thermal considerations, refer to UG520: Virtex-5QV FPGA Packaging and Pinout Specification.
4. 3.3V I/O absolute maximum limit applied to DC and AC signals.

Table 2: **Recommended Operating Conditions**

Symbol	Description	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND	0.95	1.05	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	2.375	2.625	V
V_{CCO}	Supply voltage relative to GND	1.14	3.45	V
V_{IN}	3.3V supply voltage relative to GND	GND – 0.20	3.45	V
	2.5V and below supply voltage relative to GND	GND – 0.20	V_{CCO} + 0.2	V
I_{IN}(1)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	10	mA
V_{BATT}	Battery voltage relative to GND	1.0	3.6	V
T_j	Operating junction temperature	–55	+125	°C

Notes:
1. A total of 100 mA per bank should not be exceeded.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ(1)	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	20	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	20	µA
C_{IN}	Input capacitance (sample-tested)	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V	20	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	10	–	90	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 2.5V	5	–	110	µA
I_{BATT}(2)	Battery supply current	–	–	150	nA
n	Temperature diode ideality factor	–	1.0002	–	n
r	Series resistance	–	5.0	–	Ω

Notes:
1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst-case process at 25°C.

Important Note

Typical values for quiescent supply current are now specified at nominal voltage, 125°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at T_j = 125°C because the majority of designs operate near the high end of the temperature range. Data sheets for older products (e.g., Virtex-4QV devices) still specify typical quiescent supply current at T_j = 25°C. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified in Table 4.

Table 4: **Typical Quiescent Supply Current**

Symbol	Description	Device	Typical(1)(2)(3)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XQR5VFX130	6344(4)	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XQR5VFX130	12	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XQR5VFX130	304	mA

Notes:
1. Typical values are specified at nominal voltage, 125°C junction temperatures (T_j).
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-stated and floating.
3. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the Xilinx Power tool.
4. Maximum I_{CCINTQ} is 8A, specified at maximum V_{CCINT} and 125°C junction temperature (T_j).

Power-On Power Supply Requirements

Xilinx® FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The required power-on sequence is V_{CCINT}, V_{CCAUX}, and V_{CCO}. The I/O remains 3-stated through power-on if the required power-on sequence is followed. Xilinx does not specify the current or I/O behavior for other power-on sequences.

Table 5 shows the minimum current required by the Virtex-5QV device for proper power-on and configuration.

If the current minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

The FPGA must be configured after V_{CCINT} is applied.

Once initialized and configured, use the Xilinx Power tools to estimate current drain on these supplies.

The required power-down sequence is V_{CCO}, V_{CCAUX}, and V_{CCINT}.

Table 5: **Power-On Current for the Virtex-5QV Device**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	Units
XQR5VFX130	See I_{CCINTQ} in Table 4	I_{CCAUXQ} + 40	I_{CCOQ} + 80	mA

Table 6: **Power Supply Ramp Time**

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 7: **SelectIO DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL	–0.3	0.8	2.0	3.45	0.4	2.4	Note (2)	Note (2)
LVCMOS33, LVDCI33	–0.3	0.8	2.0	3.45	0.4	V_{CCO} – 0.4	Note (2)	Note (2)
LVCMOS25, LVDCI25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note (2)	Note (2)
LVCMOS18, LVDCI18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.45	V_{CCO} – 0.45	Note (3)	Note (3)
LVCMOS15, LVDCI15	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note (3)	Note (3)
LVCMOS12	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note (4)	Note (4)
PCI33_3(5)	–0.2	30% V_{CCO}	60% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	Note (5)	Note (5)
PCI66_3(5)	–0.2	30% V_{CCO}	60% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	Note (5)	Note (5)
PCI-X(5)	–0.2	35% V_{CCO}	60% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	Note (5)	Note (5)
GTLP	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	–	0.6	N/A	36	N/A
GTL	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	–	0.4	N/A	32	N/A
HSTL I_12	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I(6)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(6)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
HSTL III(6)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	24	–8
HSTL IV(6)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	48	–8
DIFF HSTL I(6)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
DIFF HSTL II(6)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
DIFF SSTL2 I	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL2 II	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 I	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–

Notes:

1. Tested according to relevant specifications.
2. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
3. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
4. Supported drive strengths of 2, 4, 6, or 8 mA.
5. For more information on PCI33_3, PCI66_3, and PCI-X, refer to **UG190**: *Virtex-5 FPGA User Guide, Chapter 6, 3.3V I/O Design Guidelines*.
6. Applies to both 1.5V and 1.8V HSTL.

HT DC Specifications (HT_25)

Table 8: **HT DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	495	600	850	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15	–	15	mV
V_{OCM}	Output Common Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	495	600	715	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		–15	–	15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15	–	15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15	–	15	mV

LVDS DC Specifications (LVDS_25)

Table 9: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.500	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	350	–	820	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.500	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High (Q – $\overline{Q}$), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

GTX_DUAL Tile Specifications

GTX_DUAL Tile DC Characteristics

Table 11: **Absolute Maximum Ratings for GTX_DUAL Tiles**

Symbol	Description	Value	Units
MGTAVCCPLL	Analog supply voltage for the GTX_DUAL shared PLL relative to GND	–0.5 to 1.1	V
MGTAVTTTX	Analog supply voltage for the GTX_DUAL transmitters relative to GND	–0.5 to 1.32	V
MGTAVTTRX	Analog supply voltage for the GTX_DUAL receivers relative to GND	–0.5 to 1.32	V
MGTAVCC	Analog supply voltage for the GTX_DUAL common circuits relative to GND	–0.5 to 1.1	V
MGTAVTTRXC	Analog supply voltage for the resistor calibration circuit of the GTX_DUAL column	–0.5 to 1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 12: **Recommended Operating Conditions for GTX_DUAL Tiles(1)(2)**

Symbol	Description	Min	Max	Units
MGTAVCCPLL	Analog supply voltage for the GTX_DUAL shared PLL relative to GND	0.95	1.05	V
MGTAVTTTX	Analog supply voltage for the GTX_DUAL transmitters relative to GND	1.14	1.26	V
MGTAVTTRX	Analog supply voltage for the GTX_DUAL receivers relative to GND	1.14	1.26	V
MGTAVCC	Analog supply voltage for the GTX_DUAL common circuits relative to GND	0.95	1.05	V
MGTAVTTRXC	Analog supply voltage for the resistor calibration circuit of the GTX_DUAL column	1.14	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in UG198: *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*.
2. Voltages are specified for the temperature range of T_j = –55°C to +125°C.

Table 13: **DC Characteristics Over Recommended Operating Conditions for GTX_DUAL Tiles(1)**

Symbol	Description	Typ(4)	Units
$I_{MGTAVTTTX}$	GTX_DUAL tile transmitter termination supply current(2)	43.3	mA
$I_{MGTAVCCPLL}$	GTX_DUAL tile shared PLL supply current	38.0	mA
$I_{MGTAVTTRXC}$	GTX_DUAL tile resistor termination calibration supply current	0.1	mA
$I_{MGTAVTTRX}$	GTX_DUAL tile receiver termination supply current(3)	40.3	mA
$I_{MGTAVCC}$	GTX_DUAL tile internal analog supply current	80.5	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	59.0 ± 1% tolerance	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.2 Gb/s line rate.
2. I_{CC} numbers are given per GTX_DUAL tile with both GTX transceivers operating with default settings.
3. AC coupled TX/RX link.
4. Values for currents other than the values specified in this table can be obtained by using the Xilinx Power Estimator (XPE) tool.

Table 14: **GTX_DUAL Tile Quiescent Supply Current**

Symbol	Description	Typ(1)	Units
$I_{AVTTTXQ}$	Quiescent MGTAVTTTX (transmitter termination) supply current	8.2	mA
$I_{AVCCPLLQ}$	Quiescent MGTAVCCPLL (PLL) supply current	0.8	mA
$I_{AVTTRXQ}$	Quiescent MGTAVTTRX (receiver termination) supply current. Includes MGTAVTTRXCQ.	1.2	mA
I_{AVCCQ}	Quiescent MGTAVCC (analog) supply current	9.0	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Device powered and unconfigured.
3. Currents for conditions other than values specified in this table can be obtained by using the Xilinx Power Estimator (XPE) tool.
4. GTX_DUAL tile quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of GTX_DUAL tiles used.

GTX_DUAL Tile DC Input and Output Levels

Table 15 summarizes the DC output specifications of the GTX_DUAL tiles in Virtex-5QV FPGAs. Figure 1 shows the single-ended output voltage swing. Figure 2 shows the peak-to-peak differential output voltage.

Consult UG198: *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* for further details.

Table 15: **GTX_DUAL Tile DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled ≤ 4.25 Gb/s	200	–	1800	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTTRX = 1.2V	–400	–	MGTAVTTRX +400 up to 1320	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTTRX = 1.2V	–	800	–	mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	TXBUFDIFFCTRL = `111`	–	–	1400	mV
V_{SEOUT}	Single-ended output voltage swing(1)	TXBUFDIFFCTRL = `111`	–	–	700	mV
V_{CMOUT}	Common mode output voltage	Equation based MGTAVTTTX = 1.2V	1200 – DV_{PPOUT}/2			mV
R_{IN}	Differential input resistance		85	100	120	Ω
R_{OUT}	Differential output resistance		85	100	120	Ω
T_{OSKEW}	Transmitter output skew		–	2	8	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		75	100	200	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG198: *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* and can result in values lower than reported in this table.
2. Values outside of this range can be used as appropriate to conform to specific protocols and standards.

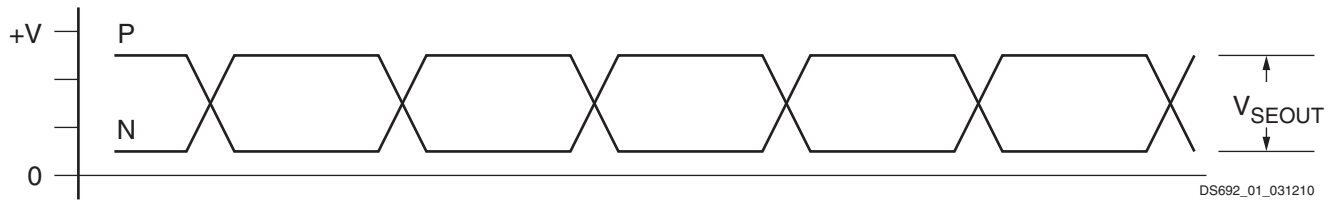

Figure 1: **Single-Ended Output Voltage Swing**

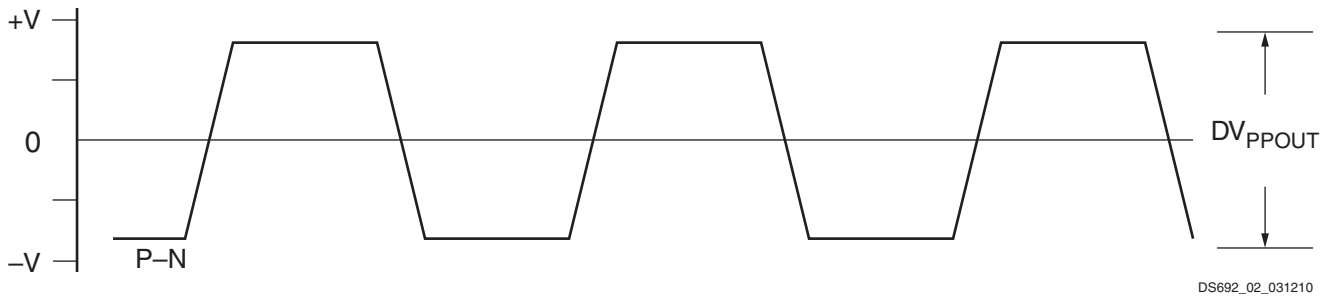

Figure 2: **Peak-to-Peak Differential Output Voltage**

Table 16 summarizes the DC specifications of the clock input of the GTX_DUAL tile. Figure 3 shows the single-ended input voltage swing. Figure 4 shows the peak-to-peak differential clock input voltage swing. Consult UG198: *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* for further details.

Table 16: **GTX_DUAL Tile Clock DC Input Level Specification(1)**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	210	800	2000	mV
V_{ISE}	Single-ended input voltage	105	400	1000	mV
R_{IN}	Differential input resistance	90	105	130	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

Notes:

1. V_{MIN} = 0V and V_{MAX} = 1200 mV.

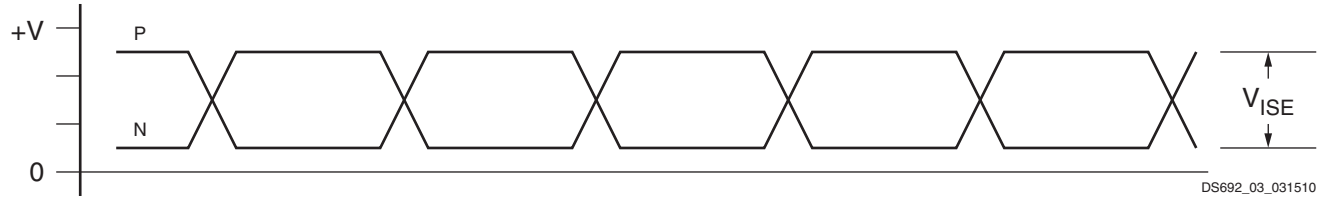

Figure 3: **Single-Ended Clock Input Voltage Swing Peak-to-Peak**

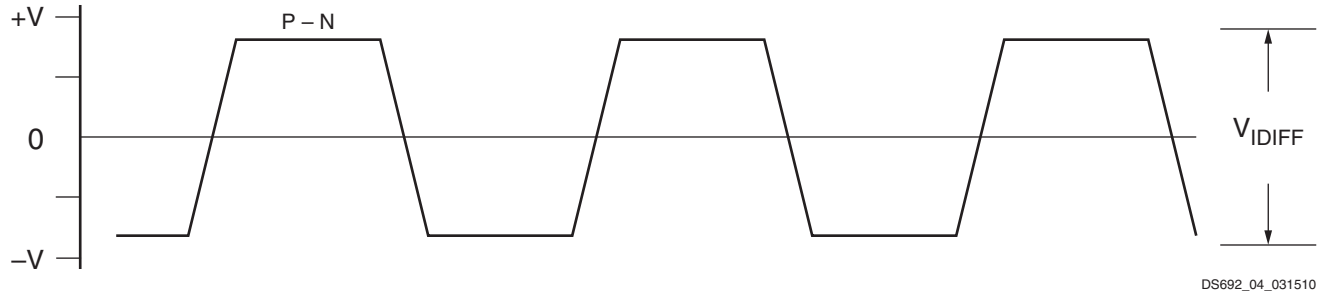

Figure 4: **Differential Clock Input Voltage Swing Peak-to-Peak**

GTX_DUAL Tile Switching Characteristics

Consult UG198: *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* for further information.

Table 17: **GTX_DUAL Tile Performance**

Symbol	Description	Value	Units
F_{GTXMAX}	Maximum GTX transceiver data rate	4.25	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	3.25	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.48	GHz

Table 18: **Dynamic Reconfiguration Port (DRP) in the GTX_DUAL Tile Switching Characteristics**

Symbol	Description	Value	Units
$F_{GTXDRPCLK}$	GTX DCLK (DRP clock) maximum frequency	150	MHz

Table 19: **GTX_DUAL Tile Reference Clock Switching Characteristics**

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{GCLK}	Reference clock frequency range(1)	CLK	60	–	650	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	CLK	40	50	60	%
T_{GJTT}	Reference clock total jitter(2)(3)	At 100 KHz	—	–145	–	dBc/Hz
		At 1 MHz	–	–150	–	dBc/Hz
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock	–	0.25	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock	–	–	200	µs

Notes:

1. GREFCLK can be used for serial bit rates up to 1 Gb/s; however, Jitter Specifications are not guaranteed when using GREFCLK.
2. GTX_DUAL jitter characteristics measured using a clock with specification T_{GJTT}. A reference clock with higher phase noise can be used with link margin trade off.
3. The selection of the reference clock is application dependent. This parameter describes the quality of the reference clock used during transceiver jitter characterization - see Table 21 and Table 22.

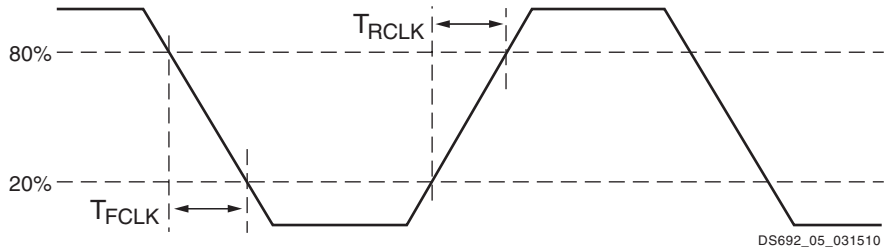

Figure 5: **Reference Clock Timing Parameters**

Table 20: **GTX_DUAL Tile User Clock Switching Characteristics(1)**

Symbol	Description	Conditions	Value	Units
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit datapath	212.5	MHz
		Internal 16-bit datapath	265.625	MHz
F_{RXREC}	RXRECCLK maximum frequency		265.625	MHz
T_{RX}	RXUSRCLK maximum frequency		265.625	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1-byte interface	235.625	MHz
		2-byte interface	265.625	MHz
		4-byte interface	132.813	MHz
T_{TX}	TXUSRCLK maximum frequency	2-byte or 4-byte interface	265.625	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1-byte interface	235.625	MHz
		2-byte interface	265.625	MHz
		4-byte interface	132.813	MHz

Notes:

1. Clocking must be implemented as described in UG198: *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*.

Table 21: **GTX_DUAL Tile Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.15	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%	–	120	–	ps
T_{FTX}	TX Fall time	80%–20%	–	120	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	350	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	75	ns
$T_{J6.5}$	Total Jitter(2)	6.5 Gb/s	–	–	0.33	UI
$D_{J6.5}$	Deterministic Jitter(2)		–	–	0.17	UI
$T_{J5.0}$	Total Jitter(2)	5.0 Gb/s	–	–	0.33	UI
$D_{J5.0}$	Deterministic Jitter(2)		–	–	0.15	UI
$T_{J4.25}$	Total Jitter(2)	4.25 Gb/s	–	–	0.33	UI
$D_{J4.25}$	Deterministic Jitter(2)		–	–	0.14	UI
$T_{J3.75}$	Total Jitter(2)	3.75 Gb/s	–	–	0.34	UI
$D_{J3.75}$	Deterministic Jitter(2)		–	–	0.16	UI
$T_{J3.2}$	Total Jitter(2)	3.2 Gb/s	–	–	0.20	UI
$D_{J3.2}$	Deterministic Jitter(2)		–	–	0.10	UI
$T_{J3.2L}$	Total Jitter(2)	3.2 Gb/s(3)	–	–	0.36	UI
$D_{J3.2L}$	Deterministic Jitter(2)		–	–	0.16	UI
$T_{J2.5}$	Total Jitter(2)	2.5 Gb/s	–	–	0.20	UI
$D_{J2.5}$	Deterministic Jitter(2)		–	–	0.08	UI
$T_{J1.25}$	Total Jitter(2)	1.25 Gb/s	–	–	0.15	UI
$D_{J1.25}$	Deterministic Jitter(2)		–	–	0.06	UI
T_{J750}	Total Jitter(2)(4)	750 Mb/s	–	–	0.10	UI
D_{J750}	Deterministic Jitter(2)(4)		–	–	0.03	UI
T_{J150}	Total Jitter(2)(4)	150 Mb/s	–	–	0.02	UI
D_{J150}	Deterministic Jitter(2)(4)		–	–	0.01	UI

Notes:

1. Using the same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTX_DUAL sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.
3. PLL frequency at 1.6 GHz and OUTDIV = 1.
4. GREFCLK can be used for serial data rates up to 1.0 Gb/s, but performance is not guaranteed.

Table 22: **GTX_DUAL Tile Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTXRX}	Serial data rate	RX oversampler not enabled	0.75	–	F_{GTXMAX}	Gb/s
		RX oversampler enabled	0.15	–	0.75	Gb/s
$T_{RXELECIDLE}$	TIme for RXELECIDLE to respond to loss or restoration of data	OOBDETECT_THRESHOLD = 110	–	–	75	ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak	OOBDETECT_THRESHOLD = 110	55	–	135	mV
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)	Internal AC capacitor bypassed	–	–	512	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance(2)	CDR 2nd-order loop disabled	–200	–	200	ppm
		CDR 2nd-order loop enabled	–2000	–	2000	ppm
SJ Jitter Tolerance(3)						
$JT\_SJ_{6.5}$	Sinusoidal Jitter(4)	6.5 Gb/s	0.44	–	–	UI
$JT\_SJ_{5.0}$	Sinusoidal Jitter(4)	5.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{4.25}$	Sinusoidal Jitter(4)	4.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.75}$	Sinusoidal Jitter(4)	3.75 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.2}$	Sinusoidal Jitter(4)	3.2 Gb/s	0.45	–	–	UI
$JT\_SJ_{3.2L}$	Sinusoidal Jitter(4)	3.2 Gb/s(5)	0.45	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(4)	2.5 Gb/s	0.50	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(4)	1.25 Gb/s	0.50	–	–	UI
JT_SJ_{750}	Sinusoidal Jitter(4)(6)	750 Mb/s	0.57	–	–	UI
JT_SJ_{150}	Sinusoidal Jitter(4)(6)	150 Mb/s	0.57	–	–	UI
SJ Jitter Tolerance with Stressed Eye(3)						
$JT\_TJSE_{4.25}$	Total Jitter with Stressed Eye(7)	4.25 Gb/s	0.69	–	–	UI
$JT\_SJSE_{4.25}$	Sinusoidal Jitter with Stressed Eye(7)	4.25 Gb/s	0.1	–	–	UI

Notes:

1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. Indicates the maximum offset between the receiver reference clock and the serial data. For example, a reference clock with ±100 ppm resolution results in a maximum offset of 200 ppm between the reference clock and the serial data.
3. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.
4. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
5. PLL frequency at 1.6 GHz and OUTDIV = 1.
6. GREFCLK can be used for serial data rates up to 1.0 Gb/s, but performance is not guaranteed.
7. Composite jitter with RX equalizer enabled. DFE disabled.

CRC Block Switching Characteristics

Table 23: **CRC Block Switching Characteristics**

Symbol	Description	Value	Units
F_{CRC}	CRCCLK maximum frequency	270	MHz

Ethernet MAC Switching Characteristics

Consult UG194: *Virtex-5 FPGA Tri-Mode Ethernet Media Access Controller User Guide* for further information.

Table 24: **Maximum Ethernet MAC Performance**

Description	Value	Units
Ethernet MAC maximum performance	10/100/1000	Mb/s

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in the Virtex-5QV device. These values are subject to the same guidelines as the Switching Characteristics, page 31. Table 25 shows the memory interface performance for the XQR5VFX130-CF1752 device.

Table 25: **Memory Interface Performance**

Description	Value
DDR(1)	200 MHz
DDR2(2)	200 MHz
QDR	250 MHz
QDR II(3)	250 MHz
RLDRAM(4)	250 MHz

Notes:

1. Performance defined using design implementation described in XAPP851, *DDR SDRAM Controller Using Virtex-5 FPGA Devices*.
2. Performance defined using design implementation described in XAPP858, *High-Performance DDR2 SDRAM Interface in Virtex-5 Devices*.
3. Performance defined using design implementation described in XAPP853, *QDRII SRAM Interface for Virtex-5 Devices*.
4. Performance defined using design implementation described in XAPP852, *RLDRAM II Memory Interface for Virtex-5 Devices*.

Switching Characteristics

All values represented in this data sheet are based on a speed specification version. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete engineering sample (ES) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 26 correlates the current status of each Virtex-5QV device on a per speed grade basis.

Table 26: **Virtex-5QV Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XQR5VFX130			-1

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to the Virtex-5QV device.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 27 lists the production released Virtex-5QV family member, speed grade, and the minimum corresponding supported speed specification version and ISE® software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 27: **Virtex-5QV Device Production Software and Speed Specification Release**

Device	Speed Grade Designation
	-1
XQR5VFX130	ISE 13.2 with overlay using speed specification v1.0(1)

Notes:
1. Production timing support for the XQR5VFX130 device requires ISE 13.2 and the XQR overlay with speed specification v1.0. Contact your local FAE for more information.

IOB Pad Input/Output/3-State Switching Characteristics

Table 28 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 29 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high-impedance state).

Table 28: **IOB Switching Characteristics**

I/O Standard	T_{IOPI}	T_{IOOP}	T_{IOTP}	Units
LVDS_25	1.19	1.85	3000	ns
LVDSEXT_25	1.45	1.91	3000	ns
HT_25	1.19	1.88	3000	ns
BLVDS_25	1.19	4.58	4.58	ns
RSDS_25 (point to point)	1.19	1.85	3000	ns
ULVDS_25	1.19	1.58	3000	ns
PCI33_3	1.11	2.66	2.66	ns
PCI66_3	1.11	2.66	2.66	ns
PCI-X	1.11	2.02	2.02	ns
GTL	1.35	2.08	2.08	ns
GTLP	1.30	2.16	2.16	ns
HSTL_I	1.12	2.02	2.02	ns
HSTL_II	1.12	2.03	2.03	ns
HSTL_III	1.12	2.07	2.07	ns
HSTL_IV	1.12	2.05	2.05	ns
HSTL_I _18	1.12	2.01	2.01	ns
HSTL_II _18	1.12	2.03	2.03	ns
HSTL_III _18	1.13	2.08	2.08	ns
HSTL_IV_18	1.13	2.03	2.03	ns
SSTL2_I	1.12	2.09	2.09	ns
SSTL2_II	1.12	2.00	2.00	ns
LVTTL, Slow, 2 mA	1.11	5.61	5.61	ns
LVTTL, Slow, 4 mA	1.11	3.82	3.82	ns
LVTTL, Slow, 6 mA	1.11	3.69	3.69	ns
LVTTL, Slow, 8 mA	1.11	2.94	2.94	ns
LVTTL, Slow, 12 mA	1.11	2.75	2.75	ns
LVTTL, Slow, 16 mA	1.11	2.65	2.65	ns
LVTTL, Slow, 24 mA	1.11	2.67	2.67	ns
LVTTL, Fast, 2 mA	1.11	4.54	4.54	ns
LVTTL, Fast, 4 mA	1.11	3.25	3.25	ns
LVTTL, Fast, 6 mA	1.11	2.94	2.94	ns
LVTTL, Fast, 8 mA	1.11	2.51	2.51	ns
LVTTL, Fast, 12 mA	1.11	2.32	2.32	ns

Table 28: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}	T_{IOOP}	T_{IOTP}	Units
LVTTL, Fast, 16 mA	1.11	2.25	2.25	ns
LVTTL, Fast, 24 mA	1.11	2.23	2.23	ns
LVCMOS33, Slow, 2 mA	1.11	4.98	4.98	ns
LVCMOS33, Slow, 4 mA	1.11	3.91	3.91	ns
LVCMOS33, Slow, 6 mA	1.11	3.63	3.63	ns
LVCMOS33, Slow, 8 mA	1.11	2.93	2.93	ns
LVCMOS33, Slow, 12 mA	1.11	2.74	2.74	ns
LVCMOS33, Slow, 16 mA	1.11	2.65	2.65	ns
LVCMOS33, Slow, 24 mA	1.11	2.66	2.66	ns
LVCMOS33, Fast, 2 mA	1.11	4.02	4.02	ns
LVCMOS33, Fast, 4 mA	1.11	3.18	3.18	ns
LVCMOS33, Fast, 6 mA	1.11	2.90	2.90	ns
LVCMOS33, Fast, 8 mA	1.11	2.50	2.50	ns
LVCMOS33, Fast, 12 mA	1.11	2.32	2.32	ns
LVCMOS33, Fast, 16 mA	1.11	2.24	2.24	ns
LVCMOS33, Fast, 24 mA	1.11	2.24	2.24	ns
LVCMOS25, Slow, 2 mA	0.92	4.95	4.95	ns
LVCMOS25, Slow, 4 mA	0.92	3.30	3.30	ns
LVCMOS25, Slow, 6 mA	0.92	3.07	3.07	ns
LVCMOS25, Slow, 8 mA	0.92	2.89	2.89	ns
LVCMOS25, Slow, 12 mA	0.92	2.94	2.94	ns
LVCMOS25, Slow, 16 mA	0.92	2.58	2.58	ns
LVCMOS25, Slow, 24 mA	0.92	2.62	2.62	ns
LVCMOS25, Fast, 2 mA	0.92	4.28	4.28	ns
LVCMOS25, Fast, 4 mA	0.92	2.73	2.73	ns
LVCMOS25, Fast, 6 mA	0.92	2.51	2.51	ns
LVCMOS25, Fast, 8 mA	0.92	2.37	2.37	ns
LVCMOS25, Fast, 12 mA	0.92	2.18	2.18	ns
LVCMOS25, Fast, 16 mA	0.92	2.14	2.14	ns
LVCMOS25, Fast, 24 mA	0.92	2.09	2.09	ns
LVCMOS18, Slow, 2 mA	1.00	5.70	5.70	ns
LVCMOS18, Slow, 4 mA	1.00	4.30	4.30	ns
LVCMOS18, Slow, 6 mA	1.00	3.33	3.33	ns
LVCMOS18, Slow, 8 mA	1.00	3.04	3.04	ns
LVCMOS18, Slow, 12 mA	1.00	2.77	2.77	ns
LVCMOS18, Slow, 16 mA	1.00	2.75	2.75	ns
LVCMOS18, Fast, 2 mA	1.00	4.65	4.65	ns
LVCMOS18, Fast, 4 mA	1.00	3.33	3.33	ns
LVCMOS18, Fast, 6 mA	1.00	2.66	2.66	ns
LVCMOS18, Fast, 8 mA	1.00	2.40	2.40	ns
LVCMOS18, Fast, 12 mA	1.00	2.16	2.16	ns
LVCMOS18, Fast, 16 mA	1.00	2.11	2.11	ns
LVCMOS15, Slow, 2 mA	1.10	4.86	4.86	ns
LVCMOS15, Slow, 4 mA	1.10	3.19	3.19	ns
LVCMOS15, Slow, 6 mA	1.10	2.99	2.99	ns

Table 28: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}	T_{IOOP}	T_{IOTP}	Units
LVCMOS15, Slow, 8 mA	1.10	2.84	2.84	ns
LVCMOS15, Slow, 12 mA	1.10	2.68	2.68	ns
LVCMOS15, Slow, 16 mA	1.10	2.56	2.56	ns
LVCMOS15, Fast, 2 mA	1.10	3.90	3.90	ns
LVCMOS15, Fast, 4 mA	1.10	2.65	2.65	ns
LVCMOS15, Fast, 6 mA	1.10	2.49	2.49	ns
LVCMOS15, Fast, 8 mA	1.10	2.38	2.38	ns
LVCMOS15, Fast, 12 mA	1.10	2.23	2.23	ns
LVCMOS15, Fast, 16 mA	1.10	2.10	2.10	ns
LVCMOS12, Slow, 2 mA	1.30	5.13	5.13	ns
LVCMOS12, Slow, 4 mA	1.30	2.98	2.98	ns
LVCMOS12, Slow, 6 mA	1.30	2.75	2.75	ns
LVCMOS12, Slow, 8 mA	1.30	2.77	2.77	ns
LVCMOS12, Fast, 2 mA	1.30	4.34	4.34	ns
LVCMOS12, Fast, 4 mA	1.30	2.67	2.67	ns
LVCMOS12, Fast, 6 mA	1.30	2.43	2.43	ns
LVCMOS12, Fast, 8 mA	1.30	2.25	2.25	ns
LVDCI_33	1.11	2.51	2.51	ns
LVDCI_25	0.92	2.40	2.40	ns
LVDCI_18	1.00	2.89	2.89	ns
LVDCI_15	1.10	2.69	2.69	ns
LVDCI_DV2_25	0.92	2.16	2.16	ns
LVDCI_DV2_18	1.00	2.25	2.25	ns
LVDCI_DV2_15	1.10	2.39	2.39	ns
GTL_DCI	1.35	2.07	2.07	ns
GTLP_DCI	1.30	1.97	1.97	ns
HSTL_I_12	1.12	2.07	2.07	ns
HSTL_I_DCI	1.12	2.06	2.06	ns
HSTL_II_DCI	1.12	1.99	1.99	ns
HSTL_II_T_DCI	1.12	2.06	2.06	ns
HSTL_III_DCI	1.12	2.18	2.18	ns
HSTL_IV_DCI	1.12	1.87	1.87	ns
HSTL_I_DCI_18	1.12	1.96	1.96	ns
HSTL_II_DCI_18	1.12	1.94	1.94	ns
HSTL_II _T_DCI_18	1.12	2.14	2.14	ns
HSTL_III_DCI_18	1.13	2.14	2.14	ns
HSTL_IV_DCI_18	1.13	1.88	1.88	ns
DIFF_HSTL_I_18	1.19	2.49	2.49	ns
DIFF_HSTL_I_DCI_18	1.19	2.37	2.37	ns
DIFF_HSTL_I	1.19	2.56	2.56	ns
DIFF_HSTL_I_DCI	1.19	2.64	2.64	ns
DIFF_HSTL_II_18	1.19	2.28	2.28	ns
DIFF_HSTL_II_DCI_18	1.19	2.09	2.09	ns
DIFF_HSTL_II	1.19	2.40	2.40	ns
DIFF_HSTL_II_DCI	1.19	2.42	2.42	ns

Table 28: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}	T_{IOOP}	T_{IOTP}	Units
SSTL2_I_DCI	1.12	2.06	2.06	ns
SSTL2_II_DCI	1.12	2.00	2.00	ns
SSTL2_II_T_DCI	1.12	2.06	2.06	ns
SSTL18_I	1.12	2.06	2.06	ns
SSTL18_II	1.12	2.00	2.00	ns
SSTL18_I_DCI	1.12	2.00	2.00	ns
SSTL18_II_DCI	1.12	1.94	1.94	ns
SSTL18_II_T_DCI	1.12	2.00	2.00	ns
DIFF_SSTL2_I	1.19	3.11	3.11	ns
DIFF_SSTL2_I_DCI	1.19	3.13	3.13	ns
DIFF_SSTL18_I	1.19	2.76	2.76	ns
DIFF_SSTL18_I_DCI	1.19	2.77	2.77	ns
DIFF_SSTL2_II	1.19	2.59	2.59	ns
DIFF_SSTL2_II_DCI	1.19	2.76	2.76	ns
DIFF_SSTL18_II	1.19	2.29	2.29	ns
DIFF_SSTL18_II_DCI	1.19	2.25	2.25	ns

Table 29: **IOB 3-State ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Value	Units
T_{IOTPHZ}	T input to Pad high-impedance	1.26	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 30 shows the test setup parameters used for measuring input delay.

Table 30: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(3)(5)	V_{REF} (1)(4)(5)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	0	3.0	1.4	–
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
PCI (Peripheral Component Interconnect), 33 MHz, 3.3V	PCI33_3	Per PCI™ Specification			–
PCI, 66 MHz, 3.3V	PCI66_3	Per PCI Specification			–
PCI-X, 133 MHz, 3.3V	PCIX	Per PCI-X™ Specification			–
GTL (Gunning Transceiver Logic)	GTL	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.80
GTL Plus	GTLP	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	1.0
HSTL (High-Speed Transceiver Logic), Class I and II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL, Class III and IV	HSTL_III, HSTL_IV	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class I and II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL, Class III and IV, 1.8V	HSTL_III_18, HSTL_IV_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I and II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 1.00$	$V_{REF} + 1.00$	V_{REF}	1.5
SSTL, Class I and II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
SSTL, Class I and II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
AGP-2X/AGP (Accelerated Graphics Port)	AGP	$V_{REF} - (0.2 \times V_{CCO})$	$V_{REF} + (0.2 \times V_{CCO})$	V_{REF}	AGP Spec
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0 (6)	–
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	0 (6)	–
LDT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0 (6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Input voltage level from which measurement starts.
4. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 6.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4 inches of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4-inch trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 6 and Figure 7.

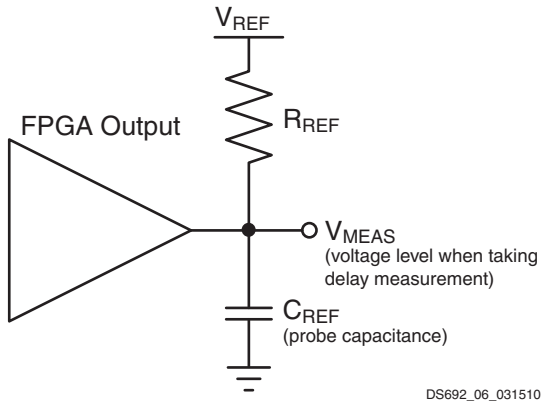

Figure 6: **Single-Ended Test Setup**

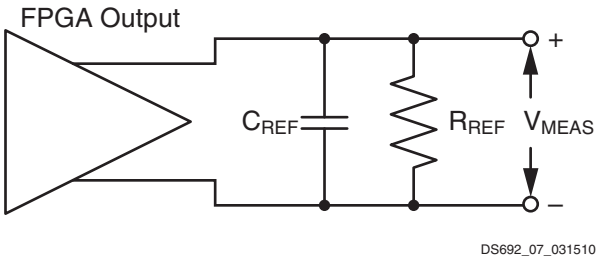

Figure 7: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 31.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 31: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF} (1) (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.4	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	10 (2)	0.94	0
	PCI33_3 (falling edge)	25	10 (2)	2.03	3.3

Table 31: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	10[2]	0.94	0
	PCI66_3 (falling edge)	25	10[2]	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	10[3]	0.94	
	PCIX (falling edge)	25	10[3]	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0[4]	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_25	100	0	0[4]	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[4]	0
LDT (HyperTransport), 2.5V	LDT_25	100	0	0[4]	0.6
LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33, HSLVDCI_33	1M	0	1.65	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I and II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III and IV, with DCI	HSTL_III_DCI, HSTL_IV_DCI	50	0	0.9	1.5
HSTL, Class I and II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III and IV, 1.8V, with DCI	HSTL_III_DCI_18, HSTL_IV_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I and II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I and II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	50	0	0.8	1.2
GTL Plus with DCI	GTLP_DCI	50	0	1.0	1.5

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. Per PCI-X specifications.
4. The value given is the differential input voltage.

Input/Output Logic Switching Characteristics

Table 32: **ILOGIC Switching Characteristics**

Symbol	Description	Value	Units
Setup/Hold			
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.66/–0.26	ns
T_{ISRCK}/T_{ICKSR}	SR/REV pin Setup/Hold with respect to CLK	1.37/–0.22	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.44/–0.12	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.40/–0.08	ns
Combinatorial			
T_{IDI}	D pin to O pin propagation delay, no Delay	0.33	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.29	ns
Sequential Delays			
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.65	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.61	ns
T_{ICKQ}	CLK to Q outputs	0.67	ns
T_{RQ}	SR/REV pin to OQ/TQ out	1.72	ns
T_{GSRQ}	Global Set/Reset to Q outputs	11.32	ns
Set/Reset			
T_{RPW}	Minimum Pulse Width, SR/REV inputs	1.35	ns, Min

Table 33: **OLOGIC Switching Characteristics**

Symbol	Description	Value	Units
Setup/Hold			
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.49/–0.11	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.25/–0.00	ns
T_{OSRCK}/T_{OCKSR}	SR/REV pin Setup/Hold with respect to CLK	1.30/–0.13	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.46/–0.18	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.32/–0.01	ns
Combinatorial			
T_{DOQ}	D1 to OQ out or T1 to TQ out	0.93	ns
Sequential Delays			
T_{OCKQ}	CLK to OQ/TQ out	0.70	ns
T_{RQ}	SR/REV pin to OQ/TQ out	2.54	ns
T_{GSRQ}	Global Set/Reset to Q outputs	11.32	ns
Set/Reset			
T_{RPW}	Minimum Pulse Width, SR/REV inputs	1.40	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 34: **ISERDES Switching Characteristics**

Symbol	Description	Value	Units
Setup/Hold for Control Lines			
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.14/0.00	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.66/–0.26	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.06/0.17	ns
Setup/Hold for Data Lines			
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.44/–0.12	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.40/–0.08	ns
T_{ISDCK_DDR} /T_{ISCKD_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	0.44/–0.12	ns
$T_{ISDCK\_DDLY\_DDR}$/$T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY)	0.40/–0.8	ns
Sequential Delays			
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.67	ns
Propagation Delays			
T_{ISDO_DO}	D input to DO output pin	0.29	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 35: **OSERDES Switching Characteristics**

Symbol	Description	Value	Units
Setup/Hold			
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.33/–0.02	ns
T_{OSDCK_T}/T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	0.46/–0.18	ns
T_{OSDCK_T2}/T_{OSCKD_T2}(1)	T input Setup/Hold with respect to CLKDIV	0.32/–0.03	ns
T_{OSCCK_OCE}/T_{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.25/0.00	ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.78	ns
T_{OSCCK_TCE}/T_{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.32/–0.01	ns
Sequential Delays			
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.68	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.70	ns
Combinatorial			
T_{OSDO_TTQ}	T input to TQ Out	0.93	ns
T_{OSCO_OQ}	Asynchronous Reset to OQ	2.45	ns
T_{OSCO_TQ}	Asynchronous Reset to TQ	2.54	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Input/Output Delay Switching Characteristics

Table 36: **Input/Output Delay Switching Characteristics**

Symbol	Description	Value	Units
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern	0	ps
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)	±5	ps
$T_{IDELAYRESOLUTION}$	IODELAY Chain Delay Resolution(1)	$1/(64 \times F_{REF} \times 1e^6)$	ps
$T_{IDELAYCTRLCO\_RDY}$	Reset to Ready for IDELAYCTRL	3.00	µs
$F_{IDELAYCTRL\_REF}$	REFCLK frequency	200.00	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	50.00	ns
$T_{IODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IODELAY	250	MHz
T_{IODCCK_CE} / T_{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.47/–0.06	ns
T_{IODCK_INC}/ T_{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.27/0.07	ns
T_{IODCK_RST}/ T_{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.37/–0.12	ns

Notes:
1. Average tap delay at 200 MHz = 78 ps.

CLB Switching Characteristics

Table 37: **CLB Switching Characteristics**

Symbol	Description	SET Filter(2)(3)		Units
		On	Off	
Combinatorial Delays				
T_{BYP}	CIN input to COUT output	–	0.11	ns, Max
T_{CINA}	CIN input to AMUX output	–	0.34	ns, Max
T_{CINB}	CIN input to BMUX output	–	0.37	ns, Max
T_{CINC}	CIN input to CMUX output	–	0.39	ns, Max
T_{CIND}	CIN input to DMUX output	–	0.44	ns, Max
Sequential Delays				
T_{CKO}	Clock to AQ – DQ outputs	–	0.66	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK				
T_{DICK}/T_{CKDI}	A – D input to CLK on A – D flip-flops	2.80/0.41	0.70/0.41	ns, Min
T_{RCK}	DX input to CLK when used as REV	2.68	0.58	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK on A – D flip-flops	3.11/–0.45	1.01/–0.45	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops	2.77/–0.03	0.67/–0.03	ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D flip-flops	2.47/0.35	0.37/0.35	ns, Min
Set/Reset				
T_{SRMIN}	SR input minimum pulse width	–	0.80	ns, Min
T_{RQ}	Delay from SR or REV input to AQ – DQ flip-flops	–	0.70	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	–	1.61	ns, Max
F_{TOG}	Toggle frequency (for export control)	–	1098	MHz

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. For more information on SET filters, refer to DS192: *Radiation-Hardened, Space-Grade Virtex-5QV Device Overview.*
3. See XMP120: *Quick Start Guide for Virtex-5QV FPGAs* for testing limitations of redundant (fault tolerant) circuits in an XQR5VFX130 device. Contact your local Xilinx sales representative to obtain a copy of XMP120.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 38: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Value	Units
Sequential Delays			
T_{SHCKO}[(2)]	Clock to A – B outputs	1.99	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	2.16	ns, Max
Setup and Hold Times Before/After Clock CLK			
T_{DS}/T_{DH}	A – D inputs to CLK	1.35/0.25	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock	0.54/0.26	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.46/–0.03	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.51/–0.07	ns, Min
Clock CLK			
T_{MPW}	Minimum pulse width	1.34	ns, Min
T_{MCP}	Minimum clock period	2.67	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 39: **CLB Shift Register Switching Characteristics**

Symbol	Description	Value	Units
Sequential Delays			
T_{REG}	Clock to A – D outputs	2.58	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	2.74	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	2.01	ns, Max
Setup and Hold Times Before/After Clock CLK			
T_{WS}/T_{WH}	WE input	0.29/–0.03	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.33/–0.07	ns, Min
T_{DS}/T_{DH}	A – D inputs to CLK	0.84/0.10	ns, Min
Clock CLK			
T_{MPW}	Minimum pulse width	1.31	ns, Min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM and FIFO Switching Characteristics

Table 40: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Value	Units
Block RAM and FIFO Clock to Out Delays			
T_{RCKO_DO} and T_{RCKO_DOR}(1)	Clock CLK to DOUT output (without output register)(2)(3)	2.46	ns, Max
	Clock CLK to DOUT output (with output register)(4)(5)	0.92	ns, Max
	Clock CLK to DOUT output with ECC (without output register)(2)(3)	4.04	ns, Max
	Clock CLK to DOUT output with ECC (with output register)(4)(5)	1.04	ns, Max
	Clock CLK to DOUT output with Cascade (without output register)(2)	3.30	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)(4)	1.46	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs(6)	1.15	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointer outputs(7)	1.66	ns, Max
T_{RCKO_ECCR}	Clock CLK to BITERR (with output register)	1.04	ns, Max
T_{RCKO_ECC}	Clock CLK to BITERR (without output register)	3.82	ns, Max
	Clock CLK to ECCPARITY in standard ECC mode	1.95	ns, Max
	Clock CLK to ECCPARITY in ECC encode only mode	1.18	ns, Max
Setup and Hold Times Before/After Clock CLK			
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs(8)	0.54/0.40	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs(9)	0.39/0.32	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with ECC in standard mode(9)	0.47/0.41	ns, Min
	DIN inputs with ECC encode only(9)	0.86/0.41	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.47/0.15	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.20/0.31	ns, Min
$T_{RCCK\_SSR}/T_{RCKC\_SSR}$	Synchronous Set/ Reset (SSR) input	0.30/0.31	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input	0.70/0.20	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN/RDEN FIFO inputs(10)	0.54/0.45	ns, Min
Reset Delays			
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers(11)	1.66	ns, Max
Maximum Frequency			
F_{MAX}	Block RAM in all modes	360	MHz
$F_{MAX\_CASCADE}$	Block RAM in Cascade mode	320	MHz
F_{MAX_FIFO}	FIFO in all modes	360	MHz
F_{MAX_ECC}	Block RAM in ECC mode	260	MHz
$F_{MAX\_WRITEBACK}$	Block RAM in ECC mode with writeback enabled	130	MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes these parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted even though WE is deasserted. Otherwise, block RAM data corruption is possible.
9. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
10. These parameters also apply to RDEN.
11. T_{RCO_FLAGS} includes these flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.

DSP48E Switching Characteristics

Table 41: **DSP48E Switching Characteristics**

Symbol	Description	Value	Units
Setup and Hold Times of Data/Control Pins to the Input Register Clock			
TDSPDCK_{AA, BB, ACINA, BCINB}/ TDSPCKD_{AA, BB, ACINA, BCINB}	{A, B, ACIN, BCIN} input to {A, B} register CLK	0.29/0.34	ns
TDSPDCK_CC/TDSPCKD_CC	C input to C register CLK	0.23/0.42	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock			
TDSPDCK_{AM, BM, ACINM, BCINM}/ TDSPCKD_{AM, BM, ACINM, BCINM}	{A, B, ACIN, BCIN} input to M register CLK	1.91/0.19	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock			
TDSPDCK_{AP, BP, ACINP, BCINP}_M/ TDSPCKD_{AP, BP, ACINP, BCINP}_M	{A, B, ACIN, BCIN} input to P register CLK using multiplier	3.64/–0.30	ns
TDSPDCK_{AP, BP, ACINP, BCINP}_NM/ TDSPCKD_{AP, BP, ACINP, BCINP}_NM	{A, B, ACIN, BCIN} input to P register CLK not using multiplier	2.05/–0.10	ns
TDSPDCK_CP/TDSPCKD_CP	C input to P register CLK	1.91/–0.13	ns
TDSPDCK_{PCINP, CRYCINP, MULTSIGNINP}/ TDSPCKD_{PCINP, CRYCINP, MULTSIGNINP}	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.46/0.11	ns
Setup and Hold Times of the CE Pins			
TDSPCCK_{CEA1A, CEA2A, CEB1B, CEB2B}/ TDSPCKC_{CEA1A, CEA2A, CEB1A, CEB2B}	{CEA1, CEA2A, CEB1B, CEB2B} input to {A, B} register CLK	0.37/0.34	ns
TDSPCCK_CECC/TDSPCKC_CECC	CEC input to C register CLK	0.29/0.31	ns
TDSPCCK_CEMM/TDSPCKC_CEMM	CEM input to M register CLK	0.40/0.29	ns
TDSPCCK_CEPP/TDSPCKC_CEPP	CEP input to P register CLK	0.82/0.01	ns
Setup and Hold Times of the RST Pins			
TDSPCCK_{RSTAA, RSTBB}/ TDSPCKC_{RSTAA, RSTBB}	{RSTA, RSTB} input to {A, B} register CLK	0.37/0.34	ns
TDSPCCK_RSTCC/ TDSPCKC_RSTCC	RSTC input to C register CLK	0.29/0.31	ns
TDSPCCK_RSTMM/ TDSPCKC_RSTMM	RSTM input to M register CLK	0.40/0.29	ns
TDSPCCK_RSTPP/TDSPCKC_RSTPP	RSTP input to P register CLK	0.82/0.01	ns
Combinatorial Delays from Input Pins to Output Pins			
TDSPDO_{AP, ACRYOUT, BP, BCRYOUT}_M	{A, B} input to {P, CARRYOUT} output using multiplier	4.30	ns
TDSPDO_{AP, ACRYOUT, BP, BCRYOUT}_NM	{A, B} input to {P, CARRYOUT} output not using multiplier	2.49	ns
TDSPDO_{CP, CCRYOUT, CRYINP, CRYINCRYOUT}	{C, CARRYIN} input to {P, CARRYOUT} output	2.33	ns
Combinatorial Delays from Input Pins to Cascading Output Pins			
TDSPDO_{AACOUT, BBCOUT}	{A, B} input to {ACOUT, BCOUT} output	1.46	ns
TDSPDO_{APCOUT, ACRYCOUT, AMULTSIGNOUT, BPCOUT, BCRYCOUT, BMULTSIGNOUT}_M	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	4.30	ns
TDSPDO_{APCOUT, ACRYCOUT, AMULTSIGNOUT, BPCOUT, BCRYCOUT, BMULTSIGNOUT}_NM	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.71	ns
TDSPDO_{CPCOUT, CCRYCOUT, CMULTSIGNOUT, CRYINPCOUT, CRYINCRYCOUT, CRYINMULTSIGNOUT}	{C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.55	ns

Table 41: **DSP48E Switching Characteristics *(Cont'd)***

Symbol	Description	Value	Units
Combinatorial Delays from Cascading Input Pins to All Output Pins			
TDSPDO_{ACINP, ACINCRYOUT, BCINP, BCINCRYOUT}_M	{ACIN, BCIN} input to {P, CARRYOUT} output using multiplier	4.30	ns
TDSPDO_{ACINP, ACINCRYOUT, BCINP, BCINCRYOUT}_NM	{ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier	2.49	ns
TDSPDO_{ACINACOUT, BCINBCOUT}	{ACIN, BCIN} input to {ACOUT, BCOUT} output	1.46	ns
TDSPDO_{ACINPCOUT, ACINCRYCOUT, ACINMULTSIGNOUT, BCINPCOUT, BCINCRYCOUT, BCINMULTSIGNOUT}_M	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	4.30	ns
TDSPDO_{ACINPCOUT, ACINCRYCOUT, ACINMULTSIGNOUT, BCINPCOUT, BCINCRYCOUT, BCINMULTSIGNOUT}_NM	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.71	ns
TDSPDO_{PCINP, CRYCINP, MULTSIGNINP, PCINCRYOUT, CRYCINCRYOUT, MULTSIGNINCRYOUT}	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output	2.04	ns
TDSPDO_{PCINPCOUT, CRYCINPCOUT, MULTSIGNINPCOUT, PCINCRYCOUT, CRYCINCRYCOUT, MULTSIGNINCRYCOUT, PCINMULTSIGNOUT, CRYCINMULTSIGNOUT, MULTSIGNINMULTSIGNOUT}	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.26	ns
Clock to Outs from Output Register Clock to Output Pins			
TDSPCKO_{PP, CRYOUTP}	CLK (PREG) to {P, CARRYOUT} output	0.63	ns
TDSPCKO_{CRYCOUTP, PCOUTP, MULTSIGNOUTP}	CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output	0.69	ns
Clock to Outs from Pipeline Register Clock to Output Pins			
TDSPCKO_{PM, CRYOUTM}	CLK (MREG) to {P, CARRYOUT} output	2.76	ns
TDSPCKO_{PCOUTM, CRYCOUTM, MULTSIGNOUTM}	CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.98	ns
Clock to Outs from Input Register Clock to Output Pins			
TDSPCKO_{PA, CRYOUTA, PB, CRYOUTB}_M	CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier	4.73	ns
TDSPCKO_{PA, CRYOUTA, PB, CRYOUTB}_NM	CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier	2.94	ns
TDSPCKO_{PC, CRYOUTC}	CLK (CREG) to {P, CARRYOUT} output	2.93	ns
Clock to Outs from Input Register Clock to Cascading Output Pins			
TDSPCKO_{ACOUTA, BCOUTB}	CLK (AREG, BREG) to {ACOUT, BCOUT}	0.88	ns
TDSPCKO_{PCOUTA, CRYCOUTA, MULTSIGNOUTA, PCOUTB, CRYCOUTB, MULTSIGNOUTB}_M	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	4.73	ns
TDSPCKO_{PCOUTA, CRYCOUTA, MULTSIGNOUTA, PCOUTB, CRYCOUTB, MULTSIGNOUTB}_NM	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	3.16	ns
TDSPCKO_{PCOUTC, CRYCOUTC, MULTSIGNOUTC}	CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	3.15	ns
Maximum Frequency			
F_{MAX}	With all registers used	360.00	MHz
F_{MAX_PATDET}	With pattern detector	328.00	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	220.00	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	203.20	MHz

Configuration Switching Characteristics

Table 42: **Configuration Switching Characteristics**

Symbol	Description	Value	Units
Power-up Timing Characteristics			
T_{PL}	Program latency	5	ms, Max
T_{POR}	Power-on reset (minimum/maximum)	10/55	ms, Min/Max
T_{ICCK}	CCLK (output) delay	300	ns, Min
$T_{PROGRAM}$	Program pulse width	250	ns, Min
Master/Slave Serial Mode Programming Switching(1)			
T_{DCCK}/T_{CCKD}	DIN setup/hold, slave mode	4.0/0.0	ns, Min
T_{DSCCK}/T_{SCCKD}	DIN setup/hold, master mode	4.0/0.0	ns, Min
T_{CCO}	DOUT	7.5	ns, Max
F_{MCCK}	Maximum frequency, master mode with respect to nominal CCLK	100	MHz, Max
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	±50	%
F_{MSCCK}	Slave mode external CCLK	100	MHz
SelectMAP Mode Programming Switching(1)			
T_{SMDCCK}/T_{SMCCKD}	SelectMAP data setup/hold	4.0/0.0	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CS_B setup/hold	4.5/0.0	ns, Min
T_{SMCCKW}/T_{SMWCCK}	RDWR_B setup/hold	11.0/0.0	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330Ω pull-up resistor required)	10	ns, Max
T_{SMCO}	CCLK to DATA out in readback	9.0	ns, Max
T_{SMCKBY}	CCLK to BUSY out in readback	7.5	ns, Max
F_{SMCCK}	Maximum frequency, master mode with respect to nominal CCLK	100	MHz, Max
F_{RBCCK}	Maximum Readback frequency with respect to nominal CCLK	40	MHz, Max
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	±50	%
Boundary-Scan Port Timing Specifications			
T_{TAPTCK}	TMS and TDI setup time before TCK	1.5	ns, Min
T_{TCKTAP}	TMS and TDI hold time after TCK	3.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid	6	ns, Max
F_{TCK}	Maximum configuration TCK clock frequency	66	MHz, Max
F_{TCKB}	Maximum Boundary-Scan TCK clock frequency	66	MHz, Max
BPI Master Flash Mode Programming Switching			
T_{BPICCO}(4)	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge	10	ns
T_{BPIDCC}/T_{BPICCD}	Setup/Hold on D[15:0] data input pins	3.0/0.5	ns
$T_{INITADDR}$	Minimum period of initial ADDR[25:0] address cycles	3.0	CCLK cycles
SPI Master Flash Mode Programming Switching			
$T_{SPIDCC}/T_{SPIDCCD}$	DIN setup/hold before/after the rising CCLK edge	4.0/0.0	ns
T_{SPICCM}	MOSI clock to out	10	ns

Table 42: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Value	Units
$T_{SPICCFC}$	FCS_B clock to out	10	ns
$T_{FSINIT}/T_{FSINITH}$	FS[2:0] to INIT_B rising edge setup and hold	2	µs
CCLK Output (Master Modes)			
T_{MCCKL}	Master CCLK clock minimum low time	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock minimum high time	40/60	%, Min/Max
CCLK Input (Slave Modes)			
T_{SCCKL}	Slave CCLK clock minimum low time	2.0	ns, Min
T_{SCCKH}	Slave CCLK clock minimum high time	2.0	ns, Min
Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK			
F_{DCK}	Maximum frequency for DCLK	320	MHz
$T_{DMCCK\_DADDR}/T_{DMCKC\_DADDR}$	DADDR setup/hold	1.75/0.0	ns
$T_{DMCCK\_DI}/T_{DMCKC\_DI}$	DI setup/hold	1.75/0.0	ns
$T_{DMCCK\_DEN}/T_{DMCKC\_DEN}$	DEN setup/hold time	1.75/0.0	ns
$T_{DMCCK\_DWE}/T_{DMCKC\_DWE}$	DWE setup/hold time	1.75/0.0	ns
T_{DMCKO_DO}	CLK to out of DO(3)	1.46	ns
$T_{DMCKO\_DRDY}/T_{DMCKCO\_DRDY}$	CLK to out of DRDY	1.46	ns

Notes:

1. Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
2. To support longer delays in configuration, use the design solutions described in *Virtex-5 FPGA User Guide*.
3. DO will hold until the next DRP operation.
4. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

Clock Buffers and Networks

Table 43: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Value	Units
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins Setup/Hold	0.31/0.00	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins Setup/Hold	0.31/0.00	ns
T_{BCCKO_O}	BUFGCTRL delay from I0/I1 to O	0.95	ns
T_{BGCKO_O}	BUFG delay from I0 to O	0.95	ns
Maximum Frequency			
F_{MAX}	BUFG	450	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGCTRL primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.

Table 44: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Value	Units
$T_{BUFIOCKO\_O}$	Clock to out delay from I to O	1.45	ns
Maximum Frequency			
F_{MAX}	I/O clock tree (BUFIO)	515.20	MHz

Table 45: **Regional Clock Switching Characteristics (BUFR)**

Symbol	Description	Value	Units
T_{BRCKO_O}	Clock to out delay from I to O	0.75	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.26	ns
T_{BRDO_CLRO}	Propagation delay from CLR to O	0.92	ns
Maximum Frequency			
F_{MAX}	Regional clock tree (BUFR)	250	MHz

PLL Switching Characteristics

PLL in PMCD mode is not supported for operation beyond the industrial temperature range.

Table 46: **PLL Specification**

Symbol	Description	Value	Units
F_{INMAX}	Maximum Input Clock Frequency	516	MHz
F_{INMIN}	Minimum Input Clock Frequency	19	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	<20% of clock input period or 1 ns Max	
F_{INDUTY}	Allowable Input Duty Cycle: 19-49 MHz	25	%
	Allowable Input Duty Cycle: 50-199 MHz	30	%
	Allowable Input Duty Cycle: 200-399 MHz	35	%
	Allowable Input Duty Cycle: 400-499 MHz	40	%
	Allowable Input Duty Cycle: >500 MHz	45	%
F_{VCOMIN}	Minimum PLL VCO Frequency	400	MHz
F_{VCOMAX}	Maximum PLL VCO Frequency	800	MHz
$F_{BANDWIDTH}$	Low PLL Bandwidth at Typical	1	MHz
	High PLL Bandwidth at Typical	4	MHz
$T_{STAPHAOFFSET}$	Static Phase Offset of the PLL Outputs	120	ps
$T_{OUTJITTER}$	PLL Output Jitter	Note 1	
$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision(2)	200	ps
$T_{LOCKMAX}$	PLL Maximum Lock Time(3)	100	µs
F_{OUTMAX}	PLL Maximum Output Frequency	360	MHz
F_{OUTMIN}	PLL Minimum Output Frequency(4)	3.13	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max	
$RST_{MINPULSE}$	Minimum Reset Pulse Width	5	ns
F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector	360	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	19	MHz
$T_{FBDELAY}$	Maximum External Delay in the Feedback Path	3 ns Max or one CLKIN cycle	

Notes:

1. Values for this parameter are available in the Architecture Wizard.
2. Includes global clock buffer.
3. The LOCK signal must be sampled after $T_{LOCKMAX}$. The LOCK signal is invalid after configuration or reset until the $T_{LOCKMAX}$ time has expired.
4. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

DCM Switching Characteristics

DCM in Maximum Range (MR) mode is not supported for operation beyond industrial temperature range.

Table 47: **Operating Frequency Ranges for DCM in Maximum Speed (MS) Mode**

Symbol	Description	Value	Units
Outputs Clocks (Low Frequency Mode)			
$F_{1XLFMSMIN}$	CLK0, CLK90, CLK180, CLK270	32.00	MHz
$F_{1XLFMSMAX}$		120.00	MHz
$F_{2XLFMSMIN}$	CLK2X, CLK2X180	64.00	MHz
$F_{2XLFMSMAX}$		240.00	MHz
$F_{DVLFMSMIN}$	CLKDV	2.0	MHz
$F_{DVLFMSMAX}$		80.00	MHz
$F_{FXLFMSMIN}$	CLKFX, CLKFX180	32.00	MHz
$F_{FXLFMSMAX}$		140.00	MHz
Input Clocks (Low Frequency Mode)			
$F_{DLLLFMSMIN}$	CLKIN (using DLL outputs)(1)(3)(4)	32.00	MHz
$F_{DLLLFMSMAX}$		120.00	MHz
$F_{CLKINLFFXMSMIN}$	CLKIN (using DFS outputs only)(2)(3)(4)	1.00	MHz
$F_{CLKINLFFXMSMAX}$		140.00	MHz
$F_{PSCLKLFMSMIN}$	PSCLK	1.00	KHz
$F_{PSCLKLFMSMAX}$		450.00	MHz
Outputs Clocks (High Frequency Mode)			
$F_{1XHFMSMIN}$	CLK0, CLK90, CLK180, CLK270	120.00	MHz
$F_{1XHFMSMAX}$		450.00	MHz
$F_{2XHFMSMIN}$	CLK2X, CLK2X180	240.00	MHz
$F_{2XHFMSMAX}$		450.00	MHz
$F_{DVHFMSMIN}$	CLKDV	7.5	MHz
$F_{DVHFMSMAX}$		300.00	MHz
$F_{FXHFMSMIN}$	CLKFX, CLKFX180	140.00	MHz
$F_{FXHFMSMAX}$		350.00	MHz
Input Clocks (High Frequency Mode)			
$F_{DLLHFMSMIN}$	CLKIN (using DLL outputs)(1)(3)(4)	120.00	MHz
$F_{DLLHFMSMAX}$		450.00	MHz
$F_{CLKINHFFXMSMIN}$	CLKIN (using DFS outputs only)(2)(3)(4)	25.00	MHz
$F_{CLKINHFFXMSMAX}$		350.00	MHz
$F_{PSCLKHFMSMIN}$	PSCLK	1.00	KHz
$F_{PSCLKHFMSMAX}$		450.00	MHz

Notes:

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. When using the DCMs CLKIN_DIVIDE_BY_2 attribute these values should be doubled. Other resources can limit the maximum input frequency.
4. When using a CLKIN frequency > 400 MHz and the DCMs CLKIN_DIVIDE_BY_2 attribute, the CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Table 48: **Input Clock Tolerances**

Symbol	Description	Frequency Range	Value	Units
Duty Cycle Input Tolerance (in %)				
$T_{DUTYCYCRANGE\_1}$	PSCLK only	< 1 MHz	25 - 75	%
$T_{DUTYCYCRANGE\_1\_50}$	PSCLK and CLKIN	1 - 50 MHz	25 - 75	%
$T_{DUTYCYCRANGE\_50\_100}$		50 - 100 MHz	30 - 70	%
$T_{DUTYCYCRANGE\_100\_200}$		100 - 200 MHz	40 - 60	%
$T_{DUTYCYCRANGE\_200\_400}$		200 - 400 MHz(4)	45 - 55	%
$T_{DUTYCYCRANGE\_400}$		> 400 MHz	45 - 55	%
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)				
$T_{CYCLFDLL}$	CLKIN (using DLL outputs)(1)		345.00	ps
$T_{CYCLFFX}$	CLKIN (using DFS outputs)(2)		345.00	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)				
$T_{CYCHFDLL}$	CLKIN (using DLL outputs)(1)		173.00	ps
$T_{CYCHFFX}$	CLKIN (using DFS outputs)(2)		173.00	ps
Input Clock Period Jitter (Low Frequency Mode)				
$T_{PERLFDLL}$	CLKIN (using DLL outputs)(1)		1.15	ns
$T_{PERLFFX}$	CLKIN (using DFS outputs)(2)		1.15	ns
Input Clock Period Jitter (High Frequency Mode)				
$T_{PERHFDLL}$	CLKIN (using DLL outputs)(1)		1.15	ns
$T_{PERHFFX}$	CLKIN (using DFS outputs)(2)		1.15	ns
Feedback Clock Path Delay Variation				
$T_{CLKFB\_DELAY\_VAR}$	CLKFB off-chip feedback		1.15	ns

Notes:

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. If both DLL and DFS outputs are used, follow the more restrictive specifications.
4. This duty cycle specification does not apply to the GTP_DUAL to DCM or GTX_DUAL to DCM connection. The GTX transceivers drive the DCMs at 450 MHz.

Output Clock Jitter

Table 49: **Output Clock Jitter**

Symbol	Description	Value	Units
Clock Synthesis Period Jitter			
$T_{PERJITT\_0}$	CLK0	±120	ps
$T_{PERJITT\_90}$	CLK90	±120	ps
$T_{PERJITT\_180}$	CLK180	±120	ps
$T_{PERJITT\_270}$	CLK270	±120	ps
$T_{PERJITT\_2X}$	CLK2X, CLK2X180	±230	ps
$T_{PERJITT\_DV1}$	CLKDV (integer division)	±180	ps
$T_{PERJITT\_DV2}$	CLKDV (non-integer division)	±350	ps
$T_{PERJITT\_FX}$	CLKFX, CLKFX180	Note (1)	ps

Notes:

1. Values for this parameter are available in the Architecture Wizard.

Output Clock Phase Alignment

Table 50: **Output Clock Phase Alignment**

Symbol	Description	Value	Units
Phase Offset Between CLKIN and CLKFB			
$T_{IN\_FB\_OFFSET}$	CLKIN/CLKFB	±60	ps
Phase Offset Between Any DCM Outputs(4)			
$T_{OUT\_OFFSET\_1X}$	CLK0, CLK90, CLK180, CLK270	±160	ps
$T_{OUT\_OFFSET\_2X}$	CLK2X, CLK2X180, CLKDV	±200	ps
$T_{OUT\_OFFSET\_FX}$	CLKFX, CLKFX180	±220	ps
Duty Cycle Precision			
$T_{DUTY\_CYC\_DLL}$(3)	DLL outputs(1)	±180	ps
$T_{DUTY\_CYC\_FX}$	DFS outputs(2)	±180	ps

Notes:

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION = TRUE.
4. All phase offsets are in respect to group CLK1X.

Table 51: **Miscellaneous Timing Parameters**

Symbol	Description	Value	Units
Time Required to Achieve LOCK			
T_{DLL_240}	DLL output – Frequency range > 240 MHz(1)	80.00	µs
$T_{DLL\_120\_240}$	DLL output – Frequency range 120 - 240 MHz(1)	250.00	µs
$T_{DLL\_60\_120}$	DLL output – Frequency range 60 - 120 MHz(1)	900.00	µs
$T_{DLL\_50\_60}$	DLL output – Frequency range 50 - 60 MHz(1)	1300.00	µs
$T_{DLL\_40\_50}$	DLL output – Frequency range 40 - 50 MHz(1)	2000.00	µs
$T_{DLL\_30\_40}$	DLL output – Frequency range 30 - 40 MHz(1)	3600.00	µs
$T_{DLL\_24\_30}$	DLL output – Frequency range 24 - 30 MHz(1)	5000.00	µs
T_{DLL_30}	DLL output – Frequency range < 30 MHz(1)	5000.00	µs
T_{FX_MIN}	DFS outputs(2)	10.00	ms
T_{FX_MAX}		10.00	ms
$T_{DLL\_FINE\_SHIFT}$	Multiplication factor for DLL lock time with Fine Shift	2.00	–
Fine Phase Shifting			
T_{RANGE_MS}	Absolute shifting range in maximum speed mode	7.00	ns
Delay Lines			
$T_{TAP\_MS\_MIN}$	Tap delay resolution (Min) in maximum speed mode	7.00	ps
$T_{TAP\_MS\_MAX}$	Tap delay resolution (Max) in maximum speed mode	30.00	ps

Notes:

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.

Table 52: **Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY	2	33
CLKFX_DIVIDE	1	32

Table 53: **DCM Switching Characteristics**

Symbol	Description	Value	Units
T_{DMCCK_PSEN}/ T_{DMCKC_PSEN}	PSEN Setup/Hold	1.56/0.00	ns
$T_{DMCCK\_PSINCDEC}$/ $T_{DMCKC\_PSINCDEC}$	PSINCDEC Setup/Hold	1.56/0.00	ns
T_{DMCKO_PSDONE}	Clock to out of PSDONE	1.30	ns

Virtex-5QV Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 54. Values are expressed in nanoseconds unless otherwise noted.

Table 54: **Global Clock Input to Output Delay without DCM or PLL**

Symbol	Description	Device	Value	Units
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12 mA, Fast Slew Rate, *without* DCM or PLL				
T_{ICKOF}	Global Clock and OUTFF *without* DCM or PLL	XQR5VFX130	9.82	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 55: **Global Clock Input to Output Delay with DCM in System-Synchronous Mode**

Symbol	Description	Device	Value	Units
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12 mA, Fast Slew Rate, *with* DCM in System-Synchronous Mode.				
$T_{ICKOFDCM}$	Global Clock and OUTFF *with* DCM	XQR5VFX130	4.65	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 56: **Global Clock Input to Output Delay with DCM in Source-Synchronous Mode**

Symbol	Description	Device	Value	Units
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12 mA, Fast Slew Rate, *with* DCM in Source-Synchronous Mode.				
$T_{ICKOFDCM\_0}$	Global Clock and OUTFF *with* DCM	XQR5VFX130	6.33	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 57: **Global Clock Input to Output Delay with PLL in System-Synchronous Mode**

Symbol	Description	Device	Value	Units
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12 mA, Fast Slew Rate, *with* PLL in System-Synchronous Mode.				
$T_{ICKOFPLL}$	Global Clock and OUTFF *with* PLL	XQR5VFX130	4.39	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 58: **Global Clock Input to Output Delay with PLL in Source-Synchronous Mode**

Symbol	Description	Device	Value	Units
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12 mA, Fast Slew Rate, *with* PLL in Source-Synchronous Mode.				
$T_{ICKOFPLL\_0}$	Global Clock and OUTFF *with* PLL	XQR5VFX130	6.90	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 59: **Global Clock Input to Output Delay with DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Value	Units
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12 mA, Fast Slew Rate, *with* DCM and PLL in System-Synchronous Mode.				
$T_{ICKOFDCM\_PLL}$	Global Clock and OUTFF with DCM and PLL	XQR5VFX130	4.56	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 60: **Global Clock Input to Output Delay with DCM and PLL in Source-Synchronous Mode**

Symbol	Description	Device	Value	Units
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12 mA, Fast Slew Rate, *with* DCM and PLL in Source-Synchronous Mode.				
$T_{ICKOFDCM0\_PLL}$	Global Clock and OUTFF with DCM and PLL	XQR5VFX130	6.24	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Virtex-5QV Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 61. Values are expressed in nanoseconds unless otherwise noted.

Table 61: **Global Clock Setup and Hold without DCM or PLL**

Symbol	Description	Device	Value	Units
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)				
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock and IFF(2) without DCM or PLL	XQR5VFX130	3.59/0.81	ns

Notes:
1. Setup and Hold times are measured over worst-case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 62: **Global Clock Setup and Hold with DCM in System-Synchronous Mode**

Symbol	Description	Device	Value	Units
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)				
T_{PSDCM}/T_{PHDCM}	No Delay Global Clock and IFF(2) with DCM in System-Synchronous Mode	XQR5VFX130	3.84/0.76	ns

Notes:
1. Setup and Hold times are measured over worst-case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 63: **Global Clock Setup and Hold with DCM in Source-Synchronous Mode**

Symbol	Description	Device	Value	Units
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)				
T_{PSDCM0}/T_{PHDCM0}	No Delay Global Clock and IFF(2) with DCM in Source-Synchronous Mode	XQR5VFX130	1.62/2.43	ns

Notes:
1. Setup and Hold times are measured over worst-case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 64: **Global Clock Setup and Hold with PLL in System-Synchronous Mode**

Symbol	Description	Device	Value	Units
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)				
T_{PSPLL}/T_{PHPLL}	No Delay Global Clock and IFF(2) with PLL in System-Synchronous Mode	XQR5VFX130	3.83/0.58	ns

Notes:
1. Setup and Hold times are measured over worst-case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 65: **Global Clock Setup and Hold with PLL in Source-Synchronous Mode**

Symbol	Description	Device	Value	Units
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)				
T_{PSPLL0}/T_{PHPLL0}	No Delay Global Clock and IFF(2) with PLL in Source-Synchronous Mode	XQR5VFX130	1.51/3.01	ns

Notes:
1. Setup and Hold times are measured over worst-case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 66: **Global Clock Setup and Hold with DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Value	Units
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)				
$T_{PSDCMPLL}/T_{PHDCMPLL}$	No Delay Global Clock and IFF(2) with DCM and PLL in System-Synchronous Mode	XQR5VFX130	4.01/0.67	ns

Notes:
1. Setup and Hold times are measured over worst-case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 67: **Global Clock Setup and Hold with DCM and PLL in Source-Synchronous Mode**

Symbol	Description	Device	Value	Units
Example Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin,(1) Using DCM, PLL, and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in IOB Switching Characteristics, page 14.				
$T_{PSDCMPLL\_0}/T_{PHDCMPLL\_0}$	No Delay Global Clock and IFF(2) with DCM and PLL in Source-Synchronous Mode	XQR5VFX130	1.79/2.34	ns

Notes:
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG. Package skew is not included in these measurements.
2. IFF = Input Flip-Flop.

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-5QV FPGA source-synchronous transmitter and receiver data-valid windows.

Table 68: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Value	Units
T_{DCD_CLK}	Global clock tree duty cycle distortion(1)	XQR5VFX130	0.12	ns
T_{CKSKEW}	Global clock tree skew(2)	XQR5VFX130	1.91	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	XQR5VFX130	0.10	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	XQR5VFX130	0.08	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	XQR5VFX130	0.25	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 69: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XQR5VFX130	CF1752	140.94	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

Table 70: **Sample Window**

Symbol	Description	Device	Value	Units
T_{SAMP}	Sampling Error at Receiver Pins(1)	XQR5VFX130	0.62	ns
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	XQR5VFX130	0.51	ns

Notes:

1. This parameter indicates the total sampling error of Virtex-5QV FPGA DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 DCM jitter
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-5QV FPGA DDR input registers across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 71: **Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out**

Symbol	Description	Value	Units
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO			
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock	–0.26/2.13	ns
Pin-to-Pin Clock-to-Out Using BUFIO			
$T_{ICKOFCS}$	Clock-to-Out of I/O clock	6.03	ns

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/19/2010	1.0	Initial Xilinx release.
08/23/2010	1.0.1	Released to www.xilinx.com.
07/12/2011	1.1	Moved data sheet from Advance Product Specification to Production. This includes revising Table 26 and updating Note 1 in Table 27. Updated values and notes in Table 2 (I_{IN}) and Table 3 (maximum I_{REF}, I_L , I_{RPU}, and I_{BATT}), Table 4, Table 5, Table 7 (V_{IH} minimum for PCI standards), Table 8 (V_{OD} maximum), and V_{OCM} in Table 9 and Table 10. Completely updated Table 5 and the Power-On Power Supply Requirements section including adding a required power-down sequence. Removed Table 11: *LVPECL DC Specifications* as the LVPECL standard is not supported in this data sheet. Removed LVPECL standard from Table 28, Table 30, and Table 31. Updated the values and notes in Table 13 through Table 18, and Table 19 through Table 23. Removed Table 25: *Register-to-Register Performance*. Added values and note 3 to Table 37. Added $F_{MAX\_WRITEBACK}$ value in Table 40 and removed note 11. In Table 42, updated values for T_{PL}, T_{POR}, T_{ICCK}, $T_{SMCKCSO}$, T_{SMDCCK}/T_{SMCCKD}, $T_{SMCSCCK}/T_{SMCCKCS}$, T_{SMCCKW}/T_{SMWCCK}, T_{TAPTCK}, T_{TCKTAP}, T_{MCCKL}, and T_{MCCKH}, and added F_{RBCCK}. Revised description of PLL support in PLL Switching Characteristics, page 31 and removed Table 49: *PLL in PMCD Mode Switching Characteristics*. Revised description of DCM support in DCM Switching Characteristics, page 32 and removed Table 51: *Operating Frequency Ranges for DCM in Maximum Range (MR) Mode*. In Table 51, removed T_{RANGE_MR}, $T_{TAP\_MR\_MIN}$, and $T_{TAP\_MR\_MAX}$. Added value to Table 69. Updated the Notice of Disclaimer.
07/24/2013	1.2	Replaced XPOWER with Xilinx Power throughout. In Important Note, removed “commercial” from second sentence and removed sentence describing differentiation in quiescent supply current by speed grade. Updated Note 3 and added Note 4 to Table 4. Updated title of Table 5. Updated Note 4 in Table 13. Updated Note 3 in Table 14. In Table 18, replaced GTXDRPCLK with GTP DCLK (DRP clock). Removed Conditions entry for T_{RX} in Table 20. Updated V_{REF} column for LVDS, LVDSEXT, and LDT in Table 30. Added $T_{IDELAYPAT\_JIT}$ to Table 36. Added Note 8 to Table 40. Replaced BUFGMUX_VIRTEX4 with BUFGCTRL in Note 1 of Table 43. Updated description of $T_{FBDELAY}$ in Table 46. In Table 70, replaced ps with ns and “All” with XQR5VFX130.
01/13/2015	1.3	Reduced the $F_{MAX\_WRITEBACK}$ value. Updated Notice of Disclaimer.
01/16/2015	1.3.1	Updated typographical error.

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