Important Product Information: Do Not Discard

Virtex-II Pro X FPGAs: -6 and -5 Speed Grade Errata and Deviations from Data Sheet DS083

DS083-E01 (v2.3) June 30, 2004 **Errata Notice**

These errata apply ONLY to -6 and -5 speed grade engineering sample *and* Step 0 production Virtex-II Pro X FPGAs. See section below for affected devices. These errata DO NOT apply to any other FPGAs. If using a different FPGA, check for errata specific to that device.

Thank you for your interest in Virtex-II Pro X devices.

The Device Errata and Operational Guidelines contained herein apply to all Virtex-II Pro X engineering sample and Step 0 production devices (in all package types), and for the -6 and -5 speed grades only. A separate errata list for -7 speed grade engineering sample devices (DS083-E02) is also available.

Obtaining the Most Recent Version of This Document

By its very nature, an errata notice is a living document and is subject to updates based on recent findings. If this document is printed or saved locally in electronic form, please check for the most recent release, available to registered users via the Xilinx mysupport.xilinx.com web site. If you have additional questions after reviewing this document, please contact your local Xilinx field application engineer (FAE) or sales representative. See: www.xilinx.com/support/services/contact_info.htm.

Devices Affected by These Errata

These errata apply only to the following part numbers:

Device Types	XC2VPX20 -6, XC2VPX20 -5
Packages	All
Date Codes or Other Differentiating Characteristics	Engineering sample *and* Step 0 production devices

Operational Details

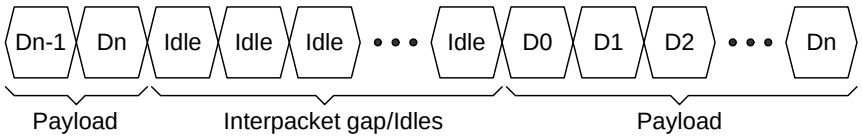
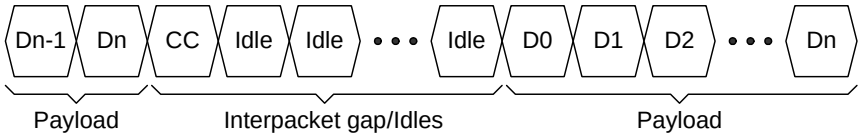
The errata described below represent deviations from DS083 data sheet specifications, and may or may not have an impact on device operation in any given design.

Details about any proposed workaround are included.

Errata	Device Specification	Deviation and Workaround(s)	Impact
1	AVCCAUXRX	AVCCAUXRX must be set to 1.8V ±3%	N/A

2	Channel Bonding Feature	Channel bonding match detection logic is always active; it cannot be disabled.
		
		Workaround:
		
		If the Channel Bonding feature is NOT desired, the match sequence should be set to an illegal sequence, one which will not occur in the actual data stream.
		
		For example, in a system with a maximum run length less than 80, the following settings will suffice as an illegal sequence that will not be reproduced in the data stream:
		
		`CHAN_BOND_SEQ_1_1 = 11'b01111111111`
		`CHAN_BOND_SEQ_1_2 = 11'b01111111111`
		`CHAN_BOND_SEQ_1_3 = 11'b01111111111`
		`CHAN_BOND_SEQ_1_4 = 11'b01111111111`
		`CHAN_BOND_SEQ_2_1 = 11'b01111111111`
		`CHAN_BOND_SEQ_2_2 = 11'b01111111111`
		`CHAN_BOND_SEQ_2_3 = 11'b01111111111`
		`CHAN_BOND_SEQ_2_4 = 11'b01111111111`
		
		`CHAN_BOND_SEQ_1_MASK = 4'b0000`
		`CHAN_BOND_SEQ_2_MASK = 4'b0000`
		
		`CHAN_BOND_SEQ_2_USE = FALSE`
		
		`CHAN_BOND_SEQ_LEN = 8`
		
		If Channel Bonding feature is desired, use as specified in the datasheet.
			Work-around must be used.

Errata	Device Specification	Deviation and Workaround(s)	Impact

3	Clock Correction Mode	Packet data can become corrupted when the idle data received between packets contains more than one idle symbol.
		
		Workaround #1:
		
		The Clock Correction symbols must be separated by at least 12 bytes. To ensure this, a special clock correction symbol can be used within the normal idle pattern to avoid the issue. This is possible if a proprietary protocol is being used or if the user has the capability to insert non-idle characters in the data.
		
		Further, if Clock Correction is used in conjunction with Channel Bonding, the Clock Correction character must be separated from the channel bonding sequence by at least 32 bytes.
		
		Normal Packet Operation:
		`<packet><idle><packet><idle><packet>`
		
		Workaround:
		`<packet><CC symbol><idle><packet>`
		
		The Clock Correction symbol can occur anywhere within the idle sequence including adjacent to the start or end of packet.
		
		Standard Mode where Idle is also clock correction character
		 
		
		Workaround where CC = Clock correction character
		 
		
		Work Around #2:
		
		Turn off Virtex-II Pro X Clock Correction and implement the function in the fabric using a Xilinx-supplied module.
			Work-around must be used.

<table>
<tr><th>Errata</th><th>Device Specification</th><th colspan="3">Deviation and Workaround(s)</th><th>Impact</th></tr>
<tr><td rowspan="7">4</td><td rowspan="7">Available MGT Mode and corresponding PMA Modes (verified in silicon)

For an explanation of MGT Modes and PMA Modes, please see the RocketIO X Transceiver User Guide, UG035.</td><td>MGT Mode</td><td>PMA Mode to Use</td><td>Available</td><td rowspan="7">N/A</td></tr>
<tr><td>OC48 /4-2-1 [4byte-2byte-1byte]</td><td>30_16, 30_32</td><td>Yes</td></tr>
<tr><td>XAUI /4-2-1</td><td>25_20, 25_40</td><td>Yes</td></tr>
<tr><td>INFINIBAND /4-2-1</td><td>28_20, 28_40</td><td>Yes</td></tr>
<tr><td>PCI-EXPRESS /4-2-1</td><td>28_20, 28_40</td><td>Yes</td></tr>
<tr><td>AURORA /4-2-1</td><td>25_20, 25_40, 28_20, 28_40, 30_16, 30_32</td><td>Yes</td></tr>
<tr><td>CUSTOM</td><td>20_40, 20_80, 25_20, 25_40, 28_20, 28_40, 30_16, 30_32</td><td>Yes</td></tr>
<tr><td>5</td><td>ESD Protection</td><td colspan="3">ESD protection on RocketIO X pins is 200V CDM</td><td>N/A</td></tr>
<tr><td>6</td><td>Clocking Requirement</td><td colspan="3">TX Fabric interface hold time issue:
- Requires Fabric clock and TXUSRCLK2 to be complementary.

RX Internal hold time issue:
- Requires RXUSRCLK and RXUSRCLK2 to be complementary only when RXUSRCLK and RXUSRCLK2 have identical frequencies.</td><td>N/A</td></tr>
<tr><td>7</td><td>TXOUTCLK deactivated on PMAINIT and Power down</td><td colspan="3">When PMAINIT or POWERDOWN is activated, TXOUTCLK is deactivated. In clocking schemes where TXOUTCLK is used to generate TXUSRCLK/TXUSRCLK2, this will result in deactivating them. Also, once powered down, the MGT does not come out of the powerdown state.

Workaround(s):

(1) Power down the MGT by writing PMA_ATTRIBUTE register 0x0f to 0x00. Release from powerdown by writing register 0x0f to 0x0f.

OR

(2) Use alternative clocking scheme if PMAINIT or POWERDOWN signals are used.</td><td>N/A</td></tr>
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Errata	Device Specification	Deviation and Workaround(s)	Impact
8	Loss of Lock	If the receiver has any frequency offset between the reference clock and the RXRECCLK, the PMARXLOCK may get deactivated causing errors in the receiver operation. **Workaround(s):** (1) Use PMARXLOCKSEL to force receiver either to LOCK-to-DATA or LOCK-to-REFERENCE.	N/A
9	Termination Impedance	Differential Termination Impedance for Rx = 115Ω ±10% Differential Termination Impedance for Tx = 134Ω ±10% **Note:** Optimal operation is achieved by designing the boards to 100Ω differential characteristic impedance.	N/A

Additional Questions or Clarifications

If additional questions arise or clarifications are needed regarding these errata, please contact your local Xilinx field application engineer (FAE) or sales representative. For the phone number in your area, see www.xilinx.com/support/services/contact_info.htm.

Any feedback with regard to these errata can be e-mailed to qa_com@xilinx.com.