Virtex-4 XC4VFX12CES Errata

EN005 (v1.2) February 21, 2006 **Errata Notification**

Introduction

Thank you for participating in the Xilinx Virtex™-4 Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the Virtex-4 XC4VFX12 FPGA. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the XC4VFX12 devices as shown in Table 1.

Table 1: **XC4VFX12 FPGA Devices Affected by These Errata**

Devices	XC4VFX12CES	JTAG ID (Revision Code): 2, 0
Packages	All	
Speed Grades	All	

Hardware Errata Details (JTAG ID = 2)

This section provides a detailed description of each hardware issue known at the release time of this document.

FIFO16

The FIFO16 does not correctly generate the ALMOST EMPTY, EMPTY, ALMOST FULL, and FULL flags after the following sequence occurs:

1. Read or Write has reached the threshold value of ALMOST EMPTY OFFSET or ALMOST FULL OFFSET.
2. A single Read or Write operation is performed, followed by a simultaneous Read or Write operation, when active Read and Write clock edges are very close together.

Unexpected or corrupt data can occur as a result of the flag failures, even if the ALMOST EMPTY or ALMOST FULL flags are not being used.

This issue does not happen in FIFO16 applications where Read and Write never occur simultaneously. Workarounds (downloadable macros) are available for users who are performing simultaneous Read/Writes. Not all workarounds will achieve data sheet performance. See Xilinx answer record 22462 for more details, workaround solutions, and corresponding performance information.

Processor Block

Frequency Performance

When using the APU controller interface, the maximum operating frequency of the processor block is 275 MHz, for -10 speed grade, 325MHz for -11 speed grades and 350MHz for -12 speed grade.

For other processor block errata and operational guidelines, please refer to answer record 20658.

Operational Guidelines

Design Software Requirements

The devices covered by these errata, unless otherwise specified, require the following Xilinx development software installations.

- Speed specification v1.57 (or later) and Xilinx software ISE 7.1i Service Pack 4 (SP4) or later is required when designing for the devices covered by this errata. Contact Xilinx technical support for SP4 help. Updates are

available on the following web page:

http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

The Stepping should be set to "0" in the constraint file (UCF file):

CONFIG STEPPING = "0";

- A summary list of ISE software known issues pertaining to the Virtex-4 features is available at:
  http://support.xilinx.com/xlnx/xil_ans_display.jsp?iLanguageID=1&iCountryID=1&getPagePath=19713

Notes and Recommendations

Virtex-II and Virtex-II Pro FPGA Designers

For Virtex-II and Virtex-II Pro designers, the CCLK specification in Virtex-4 devices was changed to LVCMOS 12mA Fast slew rate. Xilinx recommends designing to this new standard.

Hardware Errata Details (JTAG ID = 0)

This section provides a detailed description of each hardware issue known at the release time of this document for devices where JTAG ID = 0.

FIFO16

The errata for JTAG ID = 0 is the same as the errata for JTAG ID = 2. See FIFO16, page 1.

DSP48

CarryIn Input Register

The CarryIn input register from fabric is not supported (that is, the attribute `CARRYINREG = 1`).

Workaround

Use the CLB register to replace the CarryIn input register, and set attribute `CARRYINREG = 0`.

Symmetric Rounding Logic

The DSP48 element supports five different modes of symmetric rounding. All four non-pipelined rounding modes are fully supported. Only the pipelined Round (A x B) mode (that is, when `CarryInSel[1:0] = 11`) is not supported.

Workaround

Perform the equivalent logic for carry in a CLB, and connect the carry to the CarryIn input of the DSP48 using `CarryInSel[1:0] = 00` (set attribute `CARRYINREG = 0`).

DCM

1. The DCM attribute CLKOUT_PHASE_SHIFT set to the value VARIABLE_CENTER is not supported.
2. If the only clock outputs used from a DCM are CLKFX and/or CLKFX180, and the input clock frequency (CLKIN) is outside of the CLKIN_FREQ_DLL_(HF or LF)_(MS or MR)_MIN/MAX range, then use the macro in answer record 20529 to properly generate the LOCKED signal.
3. For source-synchronous applications, it is best to use the ChipSync™ features for the highest performance and lowest skew. If the DCM must be used, follow the guidelines outlined in answer record 20529 to achieve a CLKIN_CLKFB_PHASE specification of ±300 ps.

Processor Block

Frequency Performance

1) The Power PC™405 processor (PPC405) core maximum operating frequency is 300 MHz for -10 speed grade and 350 MHz for -11 speed grade.

Workaround

Compile code with the Xilinx provided Gnu compiler to achieve full frequency (350 MHz for -10 speed grade; 400 MHz -11 speed grade). For details, see answer record 21075.

When using all other compilers, the frequency is as stated in item 1.

2) When using the APU controller interface, the maximum operating frequency of the processor block is 275 MHz, for -10 speed grade and 300 MHz for -11 speed grade.

For other processor block errata and operational guidelines, refer to answer record 20658.

Operational Guidelines

Design Software Requirements

The devices covered by these errata, unless otherwise specified, require the following Xilinx development software installations.

- Speed specification v1.57 (or later) and Xilinx software ISE 7.1i Service Pack 4 (SP4) or later is required when designing for the devices covered by this errata. Contact Xilinx technical support for SP4 help. Updates are available on the following web page:

  http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

The Stepping should be set to "ES" in the constraint file (UCF file):

CONFIG STEPPING = "ES";

- A summary list of ISE software known issues pertaining to the Virtex-4 features is available at:

  http://support.xilinx.com/xlnx/xil_ans_display.jsp?iLanguageID=1&iCountryID=1&getPagePath=19713

Notes and Recommendations

Virtex-II and Virtex-II Pro FPGA Designers

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Traceability

The XC4VFX12 is marked as shown in Figure 1.

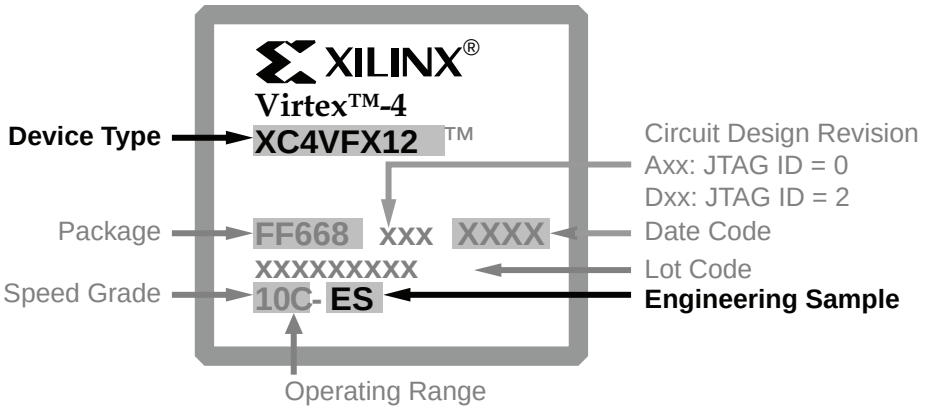

Figure 1: **Example XC4VFX12CES Package Marking**

Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications.

For additional questions regarding these errata, please contact your Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Obtaining the Most Recent Errata Version

If this document is printed or saved locally in electronic form, check for the most recent release, available to registered users on the Xilinx website at: http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Errata.

To receive an e-mail alert when this document changes, sign up at: http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=18815.

These errata apply to the following Virtex-4 documents:

Virtex-4 Overview (http://www.xilinx.com/bvdocs/publications/ds112.pdf)

Virtex-4 Data Sheet (http://www.xilinx.com/bvdocs/publications/ds302.pdf)

Virtex-4 User Guide (http://www.xilinx.com/bvdocs/user guides/ug070.pdf)

XtremeDSP™ Design Guide (http://www.xilinx.com/bvdocs/user guides/ug073.pdf)

Virtex-4 Configuration Guide (http://www.xilinx.com/bvdocs/user guides/ug071.pdf)

Virtex-4 Packaging Guide (http://www.xilinx.com/bvdocs/user guides/ug075.pdf)

PowerPC 405 Processor Block Reference Guide (http://www.xilinx.com/bvdocs/user guides/ug018.pdf)

Revision History

Date	Version	Description
03/04/05	1.0	Initial release.
03/24/05	1.1	Updated processor block information.
02/21/06	1.2	• Updated the JTAG information and the Processor Block section. • Added the FIFO16 section. • Updated Design Software Requirements section. • Replaced the LVTTL I/O standard with LVCMOS I/O standard in the Notes and Recommendations section. • Removed System Monitor errata because it is no longer in the Virtex-4 data sheet.