Spartan-3AN XC3S50AN FPGA Errata for Engineering Samples

EN027 (v1.2) December 12, 2007 **Errata Notice**

Introduction

Thank you for your interest in the Xilinx Spartan™-3AN family XC3S50AN FPGA device engineering samples. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in this errata notification. These errata do not apply to the XC3S50AN production FPGAs.

Device Identification

These errata apply to the XC3S50AN engineering samples as shown in Table 1. See the top-mark in Figure 1.

Table 1: **XC3S50AN Devices Affected by These Errata**

Device Types	XC3S50AN
Packages	All
Speed Grades	-4
Date Codes	All
Marked as "ES"	Yes

Traceability

XC3S50AN engineering samples are marked as shown in Figure 1. The other devices listed in Table 1 are marked similarly.

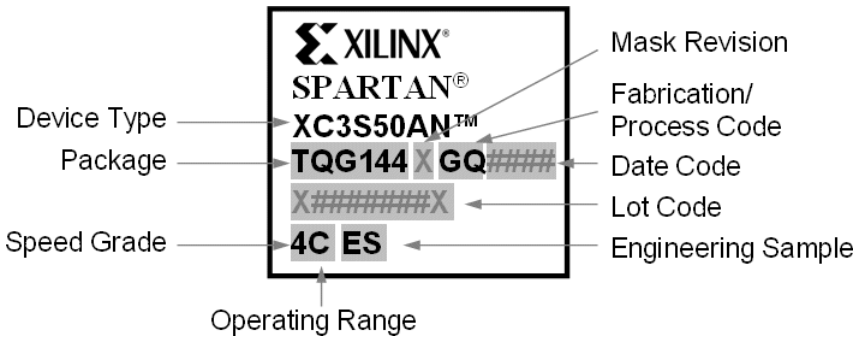

Figure 1: **XC3S50AN FPGA Top Marking**

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Hardware Errata Summary

Table 2 summarizes the known hardware issues with the XC3S50AN engineering samples. See Hardware Errata for a detailed description of each known issue. Table 2 also shows which revision is affected by a particular errata item.

Table 2: **Hardware Errata Summary**

Errata Issue	Severity	Engineering Samples	Production Devices
"ICAP Commands including MultiBoot Unavailable after Configuration from In-System Flash"	Major	Applies	Fixed
"In-System Flash May Be Pre-Programmed"	Minor	Applies	Blank
"Package Has Exposed Pad"	Minor	Applies	Fixed

Hardware Errata

This section provides a detailed description of each known hardware issue.

ICAP Commands including MultiBoot Unavailable after Configuration from In-System Flash

Applications affected

This issue affects applications that use the In-System Flash (ISF) for configuration and then use the ICAP_SPARTAN3A component for commands such as MultiBoot or readback. Applications that configure from external memory are not affected.

Description

After configuration from the In-System Flash, the ICAP_SPARTAN3A component is not available. The MultiBoot feature uses the REBOOT command on the ICAP_SPARTAN3A component. A MultiBoot request will be ignored and the current design will continue to function. The MultiBoot feature is only available after configuration from an external source, such as external SPI or Platform Flash memories.

In addition to MultiBoot, readback and access to command registers is not available through ICAP_SPARTAN3A after configuration through the In-System Flash.

Workaround

The ICAP commands for MultiBoot and readback are available after configuration from external memory. A Spartan™-3AN FPGA In-System Flash MultiBoot application can be prototyped with a Spartan-3A or Spartan-3AN FPGA and external SPI Flash memory.

This issue has been corrected in production revisions of the XC3S50AN silicon.

In-System Flash May Be Pre-Programmed

Applications affected

This issue affects applications that use the FPGA before programming the In-System Flash. Applications that erase or program the In-System Flash before use on a board are not affected.

Description

The In-System Flash memory is pre-programmed as part of Xilinx testing. Engineering Samples may be shipped with this design instead of a blank device. If the Mode pins are set to configure from the In-System Flash, then the pre-programmed design will be used to configure the FPGA at power-up. The design uses the default configuration options, including pull-down resistors on unused pins. The design uses no I/O pins, other than an input on M2. The DONE pin will be driven High, and the I/O pins will have internal pull-down resistors.

Workaround

XC3S50AN engineering sample devices should have the In-System Flash programmed with the user application, or erased, before use on a board. Alternatively, set the Mode pins to any configuration mode other than ISF so that the

FPGA does not configure with the pre-programmed pattern. If the FPGA is configured with the pre-programmed pattern, make sure the internal pull-downs are acceptable on the PC board. Where necessary, add external pull-ups that are strong enough to overcome the internal pull-down value shown in the data sheet.

This issue has been corrected in production revisions of the XC3S50AN device. All production devices are shipped blank.

Package Has Exposed Pad

Applications affected

The XC3S50AN FPGA engineering samples are offered in only one package and therefore this issue could affect all applications. This issue specifically restricts applications that route signals under the package.

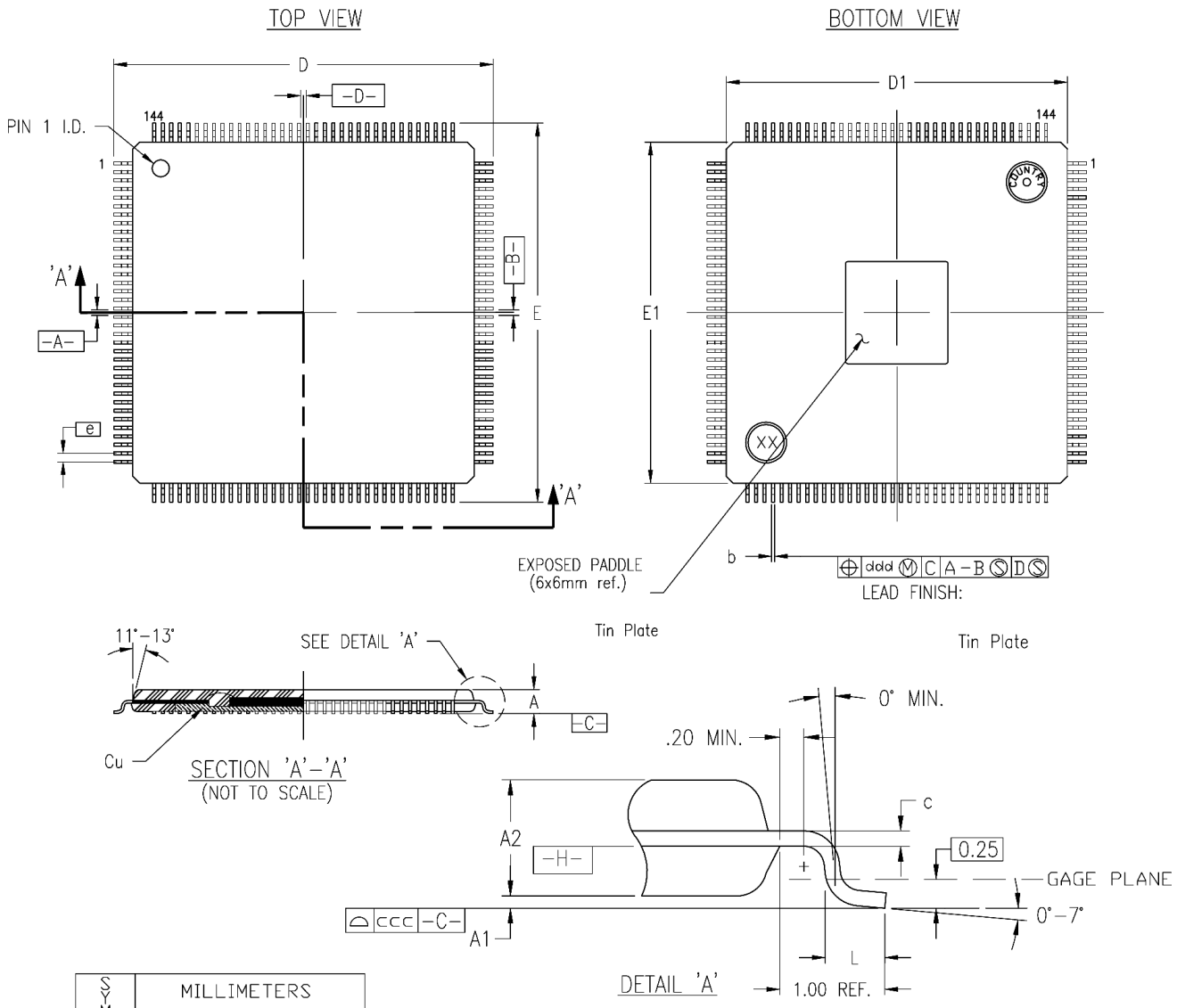
Description

The XC3S50AN engineering samples are assembled in a non-standard package with an exposed metal pad on the bottom. The package dimensions shown in Figure 2 match those of the standard TQG144 package which will be used for production. As shown in Figure 2, the package used for the engineering samples has an exposed pad in the middle of the bottom side, with maximum dimensions of 6mm x 6mm. The exposed pad package is typically used to enhance thermal characteristics and signal integrity, but is not being used for those reasons. The package is only a temporary solution until the production package is available. All thermal, material, and reliability characteristics of this package are similar to those of the standard package.

Workaround

Do not route signals in the area of the exposed pad. The exposed pad can be unconnected on the board, or it can be connected to GND. Do not use the engineering samples for qualification.

This issue has been corrected in production revisions of the XC3S50AN device. Production devices use the standard TQG144 package, with a different assembly process and without the exposed pad.



SYMBOL	MILLIMETERS		
	MIN.	NOM.	MAX.
A			1.60
A_1	0.05	0.10	0.15
A_2	1.35	1.40	1.45
D/E	22.00 BSC		
D_1/E_1	20.00 BSC		
L	0.45	0.60	0.75
e	0.50 BSC		
b	0.17	0.22	0.27
c	0.09		0.20
ccc			0.08
ddd			0.08

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5-1982.
2. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm ON EACH SIDE.
3. THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.
4. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026

Figure 2: **XC3S50AN ES Package Dimensions with Exposed Pad**

Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications. For questions about these errata, please contact Xilinx Technical Support http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx sales representative, http://www.xilinx.com/company/contact.htm.

Obtaining Errata Notification Updates

If this document is printed or saved locally, please check for the most recent release, available to registered users on the Xilinx web site at http://www.xilinx.com/support/documentation/spartan-3an_errata.htm. To receive an e-mail alert when this document changes, sign up for alerts on xilinx.com.

Applicable Documents

These errata apply to the following XC3S50AN documents:

- **DS557: Spartan-3AN FPGA Family Data Sheet**
  www.xilinx.com/support/documentation/data_sheets/ds557.pdf
- **UG331: Spartan-3 Generation FPGA User Guide**
  www.xilinx.com/support/documentation/user_guides/ug331.pdf
- **UG332: Spartan-3 Generation Configuration User Guide**
  www.xilinx.com/support/documentation/user_guides/ug332.pdf
- **UG333: Spartan-3AN FPGA In-System Flash User Guide**
  www.xilinx.com/support/documentation/user_guides/ug333.pdf

Revision History

The following table shows the revision history for this document.

Date	Version	Description
05/21/07	1.0	Initial release
06/25/07	1.1	Added “In-System Flash May Be Pre-Programmed” and “Package Has Exposed Pad”
12/12/07	1.2	Updated to note that all errata are fixed in production devices. Updated links.