Virtex-4 LX/SX Family and FX12 Production Errata

EN041 (v1.2) August 6, 2007 **Errata Notification**

Introduction

Thank you for designing with the Xilinx Virtex™-4 family of devices. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the Virtex-4 LX, SX, and FX devices, as shown in Table 1 and in Table 2.

Table 1: **Virtex-4 LX and SX Devices Affected by These Errata—All Speed Grades and Packages**

Device	Step 1		Step 2	
	JTAG ID (Revision Code)	Config Stepping	JTAG ID (Revision Code)	Config Stepping
XC4VLX15	3	1	5	2
XC4VLX25	9	1	A	2
XC4VLX40	3	1	5	2
XC4VLX60	2, 3	1	4, 5	2
XC4VLX80	3	1	5	2
XC4VLX100	2, 3	1	4, 5	2
XC4VLX160	0, 3	1	2, 5	2
XC4VLX200	0, 3	1	4, 5	2
XC4VSX25	2	1	4	2
XC4VSX35	2	1	4	2
XC4VSX55	2	1	4	2

Table 2: **Virtex-4 FX Devices Affected by These Errata—All Speed Grades and Packages**

Device	Step 0	
	JTAG ID (Revision Code)	Config Stepping
XC4VFX12	2	0

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

FIFO16

The FIFO16 does not correctly generate the ALMOST EMPTY, EMPTY, ALMOST FULL, and FULL flags after the following sequence occurs:

1. Read or Write has reached the threshold value of ALMOST EMPTY OFFSET or ALMOST FULL OFFSET.
2. A single Read or Write operation is performed, followed by a simultaneous Read or Write operation, when active Read and Write clock edges are very close together.

Unexpected or corrupt data can occur as a result of the flag failures, even if the ALMOST EMPTY or ALMOST FULL flags are not being used.

This issue does not happen in FIFO16 applications where Read and Write never occur simultaneously. Workarounds (downloadable macros) are available for users who are performing simultaneous Read/Writes. Not all workarounds will achieve data sheet performance. See Xilinx answer record 22462 for more details, workaround solutions, and corresponding performance information.

Processor Block

Frequency Performance (applies to FX12 devices only)

When using the APU controller interface, the maximum operating frequency of the processor block is 275 MHz for -10 speed grade, 325 MHz for -11 speed grades, and 350 MHz for -12 speed grade.

For other processor block errata and operational guidelines, please refer to answer record 20658.

Configuration

FRAME_ECC (applies to LX and SX Step 1 devices only)

FRAME_ECC readback of unused configuration bits in I/O IDELAY frames might indicate readback errors. These are false errors and can be ignored because they have no functional impact.

Workaround

The reference design described in XAPP714 can be used to eliminate this error indication.

Operational Guidelines

Design Software Requirements

The devices covered by these errata, unless otherwise specified, require the following Xilinx development software installations.

- When designing with the devices listed in Table 1, speed specification v1.58 (or later) and Xilinx software ISE 7.1i Service Pack 4 (SP4) or later is required.
  - Speed specification v1.58 for ISE 7.1i SP4 is available upon request through Xilinx technical support.
  - Speed specification v1.58 for ISE8.1i is available in SP1 at: http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp.

  The Stepping in the constraint file (UCF file) should be set to the configuration stepping value listed for the specific device in Table 1 or Table 2.

  CONFIG STEPPING = "*Config Stepping Value from Table 1 or* Table 2";
- A summary list of ISE software known issues pertaining to the Virtex-4 features is available at:

  http://support.xilinx.com/xlnx/xil_ans_display.jsp?iLanguageID=1&iCountryID=1&getPagePath=19713

Notes and Recommendations

Virtex-II and Virtex-II Pro FPGA Designers

For Virtex-II and Virtex-II Pro designers, the CCLK specification in Virtex-4 devices was changed to LVTTL 12mA Fast slew rate. Xilinx recommends designing to this new standard.

Traceability

All Virtex-4 devices have package markings similar to the example shown in Figure 1.

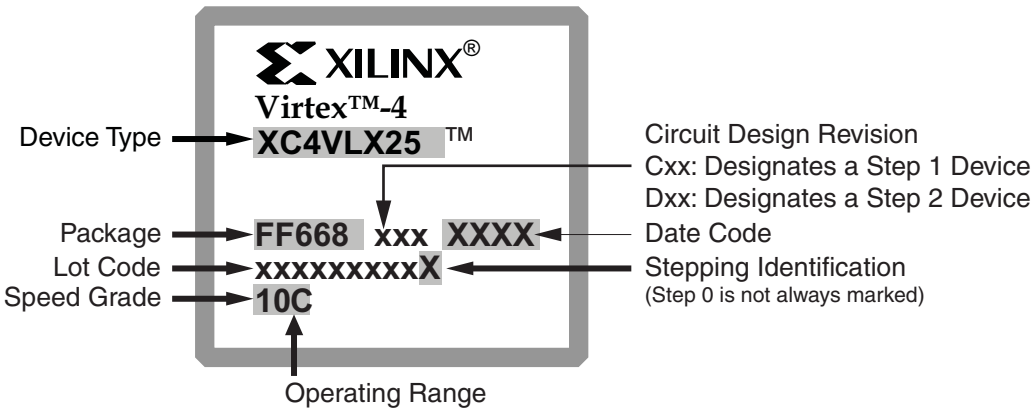

Figure 1: **Example XC4VLX25 Package Marking**

Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications.

To receive notification when this document changes, see answer record 18815 to sign up for Alerts.

For additional questions regarding these errata, please contact your Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Obtaining the Most Recent Errata Version

If this document is printed or saved locally in electronic form, check for the most recent release, available to registered users on the Xilinx website at: http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Errata.

To receive an e-mail alert when this document changes, sign up at: http://www.xilinx.com/xlnx/xil_ans_display.jsp?getPagePath=18815.

These errata apply to the following Virtex-4 documents:

Virtex-4 Overview (http://www.xilinx.com/bvdocs/publications/ds112.pdf)

Virtex-4 Data Sheet (http://www.xilinx.com/bvdocs/publications/ds302.pdf)

Virtex-4 User Guide (http://www.xilinx.com/bvdocs/userguides/ug070.pdf)

XtremeDSP™ Design Guide (http://www.xilinx.com/bvdocs/userguides/ug073.pdf)

Virtex-4 Configuration Guide (http://www.xilinx.com/bvdocs/userguides/ug071.pdf)

Virtex-4 Packaging Guide (http://www.xilinx.com/bvdocs/userguides/ug075.pdf)

Revision History

Date	Version	Description
02/23/06	1.0	Initial Xilinx release.
02/24/06	1.0.1	Fixed link to reference in the Configuration section.
06/08/07	1.1	Updated JTAG ID for XC4VLX160 and XC4VLX200 devices.
08/06/07	1.2	Updated title.