Virtex-5 XC5VFX30T CES, XC5VFX70T CES, XC5VFX100T CES, XC5VFX130T CES, and XC5VFX200T CES FPGA Errata

EN057 (v1.3) March 31, 2009

Errata Notification

Introduction

Although Xilinx has made every effort to ensure the highest possible quality, these Virtex®-5 FPGA engineering samples (ES) are subject to the limitations described in the following errata.

Devices

These errata apply to the Virtex-5 devices, as shown in Table 1.

Table 1: **Virtex-5 Devices Affected by These Errata**

Devices	Speed Grades	JTAG ID (Revision Code)
XC5VFX30T CES	-1, -2, -3	6
XC5VFX70T CES	-1, -2, -3	6
XC5VFX100T CES	-1, -2, -3	2
XC5VFX130T CES	-1, -2, -3	2
XC5VFX200T CES	-1, -2	0
Packages	All	

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

GTX Transceivers

Clock Correction

The Clock Correction feature of the Virtex-5 FPGA GTX transceiver can cause data corruption on the receiver when a clock correction sequence is skipped or added. See UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* for more detailed information about the Clock Correction feature.

This issue can occur when all of the following conditions are true:

- Asynchronous operation: When the local reference clock of the Virtex-5 FPGA GTX transceiver is driven from a different oscillator than the far-end transceiver. This introduces a parts per million (PPM) offset in frequency between the operation of the transceivers, requiring clock correction to skip or add clock correction sequences on a periodic basis. This also implies that the RXUSRCLK and RXUSRCLK2 ports of the Virtex-5 FPGA GTX transceiver are derived from the local oscillator and not the RXRECCLK port.
- Clock Correction is enabled.
  - CLK_CORRECT_USE_0/1 attribute is set to **TRUE**.
- The length of the clock correction sequence is 1 or 3 Bytes.
  - CLK_COR_ADJ_LEN_0/1 attribute is set to **1** or **3**.

When the conditions described above are met, one of the multiple work-around options described below shall be used to mitigate this issue. XAUI, PCIe®, SRIO, and Infiniband are the most common protocols affected but only when used in asynchronous operation.

© Copyright 2008–2009 Xilinx, Inc. XILINX, the Xilinx logo, Virtex, Spartan, ISE, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. PCI, PCIe and PCI Express are trademarks of PCI-SIG and used under license. All other trademarks are the property of their respective owners.

Work-around

If the application permits, implement one of the following work-around options:

•Use synchronous clocking
•Convert to 2 byte or 4 byte clock correction sequence
•If the application does not permit one of these options, see Answer Record 32164.

All versions of UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* subsequent to the current version, v2.1, will properly reflect the Clock Correction behavior described herein.

PowerPC 440 Processor

Branch History Table

The Branch History Table (BHT) must be disabled for deterministic execution latency.

Auxiliary Processor Unit

There are two errata for the Auxiliary Processor Unit (APU):

- After a Translation Look-aside Buffer (TLB) miss caused by an instruction fetch, in a very specific combination of events, the Auxiliary Processor Unit (APU) can lock up or corrupt the data.
- When the floating-point execution is disabled in the PowerPC® 440 processor but enabled in the APU controller, and an FPU instruction is executed, the processor can generate a spurious program exception instead of an FPU-unavailable exception.

Additional Information

For more details, including work-arounds for the processor errata, refer to answer record 30529.

Operational Guidelines

Design Software Requirements

CORE Generator™ software must be used to correctly configure the GTX transceivers.

The devices listed in Table 1, unless otherwise specified, require the following Xilinx development software installations.

- Speed specification v1.59 (or later), Xilinx ISE™ Design Suite 10.1 (or later).
  - For -3 speed grade, the minimum software requirement is Xilinx ISE Design Suite 10.1 with Service Pack 2 (or later).
- The stepping should not be set, but if set, it must be set to zero in the user constraint file (UCF):

  CONFIG STEPPING = “0”;

Traceability

The XC5VFX30T CES is marked as shown in Figure 1. The other devices listed in Table 1 are marked similarly.

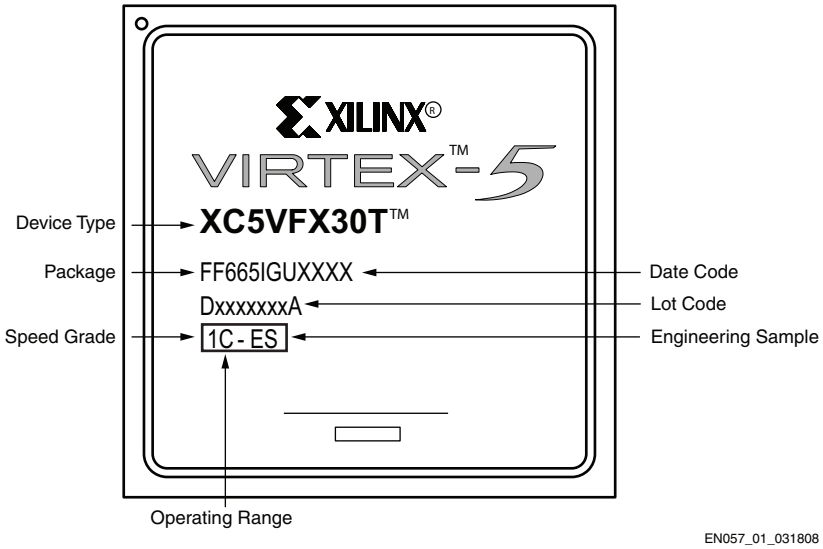

Figure 1: **Example XC5VFX30T CES Package Marking**

Additional Questions or Clarifications

All other device functionality and timing meet the data sheet specifications. For additional questions regarding these errata, please contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Revision History

Date	Version	Description
03/31/08	1.0	Initial Xilinx release.
07/08/08	1.1	Added -3 speed grade to Table 1 and updated the Design Software Requirements section.
07/25/08	1.2	Added XC5VFX200T device.
03/31/09	1.3	Added GTX Transceivers section.

Notice of Disclaimer

THE XILINX HARDWARE FPGA AND CPLD DEVICES REFERRED TO HEREIN (“PRODUCTS”) ARE SUBJECT TO THE TERMS AND CONDITIONS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT http://www.xilinx.com/warranty.htm. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED ON THE XILINX DATA SHEET. ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE. PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, OR ANY OTHER APPLICATION THAT INVOKES THE POTENTIAL RISKS OF DEATH, PERSONAL INJURY OR PROPERTY OR ENVIRONMENTAL DAMAGE (“CRITICAL APPLICATIONS”). USE OF PRODUCTS IN CRITICAL APPLICATIONS IS AT THE SOLE RISK OF CUSTOMER, SUBJECT TO APPLICABLE LAWS AND REGULATIONS. ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

THE LEGAL DISCLAIMER FOR FPGA ENGINEERING SAMPLES CAN BE VIEWED AT: http://www.xilinx.com/warranty.htm#engsample.