Kintex-7 FPGA XC7K325T CES9937 Errata

EN171 (v1.6) February 28, 2012 **Errata Notification**

Introduction

Thank you for participating in the Kintex™-7 FPGAs Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in Table 1. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in Table 1.

Table 1: **Devices Affected by These Errata**

Product Family	Device	JTAG ID (Revision Code)	Packages	Speed Grades	Temperature
Kintex-7	XC7K325T CES9937	2	All	-1, -2	0 to 85°C

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

Block RAM

Synchronous Built-in FIFO

When using the Built-In FIFO as a Synchronous FIFO (EN_SYN=TRUE) with asynchronous reset, correct behavior of the FIFO flags cannot be guaranteed after the first write.

All configurations other than EN_SYN=TRUE are not affected by this issue.

Work-around

To work around this issue, synchronize the negative edge of reset to RDCLK/WRCLK.

Asynchronous Built-in FIFO

The dual clock built-in FIFO, when used with different read and write clocks (asynchronous clocking), is not supported.

Work-around

To work around the issue, use the built-in FIFO in synchronous mode (set the EN-SYN attribute to TRUE).

See Answer Record 39995 for more information.

External Memory Interfaces

Phaser Block Divide by Two Mode for DDR3 and DDR2

The Phaser block "divide by two" mode used to implement DDR3 and DDR2 external memory interfaces at frequencies from 303–399 MHz is not operational. The Phaser block must be used in 1:1 mode, which restricts the minimum supported DDR3 and DDR2 memory clock frequency to 400 MHz (800 Mb/s DDR).

Work-around

Select a Memory Clock frequency of 400 MHz (DDR3 or DDR2) or higher (DDR3 only) in the Memory Interface Generator (MIG) tool to ensure that the Phaser block is set to 1:1 mode.

PHY Control Block 2:1 Mode for DDR3 and DDR2

The PHY control block used to implement DDR3 and DDR2 memory interfaces does not support a 2:1 PHY clock to memory controller clock ratio, preventing implementation of half rate solutions.

Work-around

Select the 4:1 PHY clock to Memory Controller clock ratio in the Memory Interface Generator (MIG) tool to generate a quarter rate DDR3 or DDR2 memory interface solution.

XADC

Integral Nonlinearity

The XADC has a four LSB (~1 mV) integral nonlinearity (INL) error versus the data sheet specifications (DS182, *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics,* v1.3) of two LSBs.

XADC On-chip Reference Variation

The XADC on-chip reference source can exceed the DS182, *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics* data sheet specification of 1.25V ±1% by an additional 0.5%. See Answer Record 44971 for more information on the impact to XADC measurements when the on-chip reference source is used.

GTX Transceivers

Out-of-Band Signaling

The GTX transceiver circuitry for out-of-band (OOB) signaling is always enabled.

GTX Line Rate

The GTX transceiver operation is limited to a maximum of 6.6 Gb/s.

QPLL Frequency Range

The supported QPLL frequency range is 5.93–6.6 GHz.

TXOUTCLK and RXOUTCLK Ports

The GTX transceiver TXOUTCLK and RXOUTCLK ports can exhibit loss of edges or excessive jitter when used simultaneously within a GTX channel and with other channels in a transceiver Quad.

The following rules must be followed for proper operation of TXOUTCLK and RXOUTCLK:

- Use either TXOUTCLK or RXOUTCLK within any GTX channel, not both.
- Use either TXOUTCLK of GTX0 or RXOUTCLK of GTX1, not both.
- Use the reference clock directly from IBUFDS_GTXE2 to drive the fabric logic and GTX user clocks when necessary ([TX/RX]USRCLK, [TX/RX]USRCLK2).

Set RXOUTCLKSEL = `3'b000` when RXOUTCLK is not used. Set TXOUTCLKSEL = `3'b000` when TXOUTCLK is not used.

See Answer Record 43244 for more information.

QPLL Use Mode

The QPLL can lose lock if reset at one temperature extreme and operated at the other.

Work-around

See Answer Record 43244 for the user design work-around.

Receiver Link Margin

The receiver can have a reduction in jitter tolerance when used in full-rate mode (RXOUT_DIV == 1).

Work-around

See Answer Record 43244 for attribute updates and equalization selection.

CPLL Jitter

The GTX CPLL when operated at 3.1 GHz, or above, can exhibit higher jitter when MGTAVTT is higher than nominal.

Transmit Electrical Idle

The transmitter common mode voltage is higher than expected when TX electrical idle is enabled. The electrical idle detection in the receiver is not impacted when links are AC coupled.

Receiver Detection for PCIe

The Receiver Detection feature used for PCIe® applications is not supported.

Work-around

Set the following attributes to force the transmitter to always detect a receiver:

- TX_RXDETECT_REF = `3'b000`
- RX_CM_SEL = `2'b11`
- (PMA_RSV2[4], RX_CM_TRIM[2:0]) = `4'b1010`

PCIe ASPM Support

ASPM L0s is not supported for Gen 2 (5 Gb/s) line rate.

Work-around

Set the following attributes on the Integrated Block for PCI Express to disable ASPM L0s:

- LINK_CAP_ASPM_OPTIONALITY = TRUE
- LINK_CAP_ASPM_SUPPORT= 0

See Answer Record 43243 for additional details.

IEEE Std 1149.1/1149.6 Boundary-Scan

IEEE Std 1149.1 for Dedicated and SelectIO Resources

In the devices listed in Table 1, IEEE Std 1149.1 (JTAG) boundary-scan test commands SAMPLE, PRELOAD, EXTEST, and HIGHZ are not functional when an MGTAVCC pin is not powered. All other JTAG commands, including device configuration and the ChipScope™ debugging tool, function as expected.

IEEE Std 1149.6 for GTX Transceivers

In the devices listed in Table 1, IEEE Std 1149.6 (ACJTAG) boundary-scan test commands EXTEST_PULSE and EXTEST_TRAIN are not supported.

SelectIO Resources

Internal Weak Pull-Ups/Pull-Downs for High-Range I/O Banks

The internal weak pull-ups/pull-downs for the high-range (HR) I/O banks will not achieve valid logic-1 and logic-0 states for 1.8V and lower V_{CCO}. External resistors should be used for V_{CCO} of 1.8V and lower.

Power

Static Current

The devices listed in Table 1 can exhibit up to 50% higher static current on all supplies compared to the static current reported in XPE 13.3. Also, up to an additional 95 mA is consumed by the MGTAVCC for each powered and uninstantiated transceiver Quad.

Power-On/Off Requirement

For V_{CCO} voltages of 3.3V in the high-range (HR) I/O banks, the following requirements must be followed:

- When V_{CCINT} is less than 0.7V, V_{CCO} must not exceed 2.625V for longer than 800 ms with T_j = 85°C for each power-on/off cycle to maintain device reliability levels.
  - This time can be allocated in any percentage between the power-on and power-off ramps.
  - This time is based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.

Design Software Requirements

The devices listed in Table 1, unless otherwise specified, require the following Xilinx Design Tools:

- Speed specification v1.02 (or later) of Xilinx® ISE® Design Suite 13.3 available at http://www.xilinx.com/support/download/ with the patch in Answer Record 43060.
- See Kintex-7 FPGA Answer Record 43347 for known issues and work-arounds for Xilinx Design Tools.

Operational Guidelines

Designs targeting DDR3 data rates above 800 Mb/s must include an external V_{REF}. For further details, refer to Answer Record 42036.

Traceability

The XC7K325T devices listed in Table 1 are marked as shown in Figure 1.

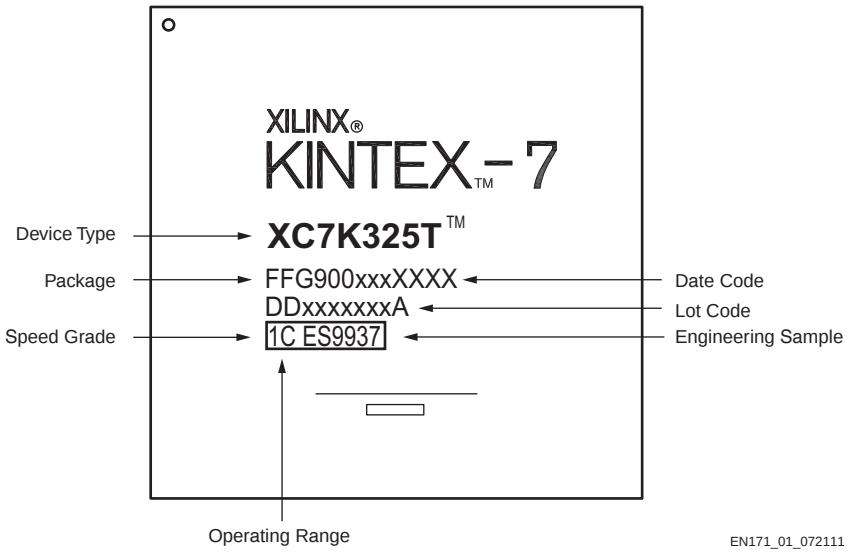

Figure 1: **Example Device Top Mark**

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact/index.htm.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/28/11	1.0	Initial Xilinx release.
08/25/11	1.1	Updated document title to Kintex-7 FPGAs CES9937 Errata. Updated Table 1 and PCIe ASPM Support. Added QPLL Frequency Range, IEEE Std 1149.1 for Dedicated and SelectIO Resources. Updated Design Software Requirements.
10/18/11	1.2	Updated Static Current. Updated Power-On/Off Sequence; new title is Power-On/Off Requirement and contains updated text.
11/03/11	1.3	Updated Design Software Requirements section.
12/01/11	1.4	Added PHY Control Block 2:1 Mode for DDR3 and DDR2 and XADC On-chip Reference Variation. Updated Power-On/Off Requirement and Design Software Requirements section
01/24/12	1.5	Added Phaser Block Divide by Two Mode for DDR3 and DDR2. Updated Phaser Block Divide by Two Mode for DDR3 and DDR2 and PHY Control Block 2:1 Mode for DDR3 and DDR2 to include DDR2. Updated XADC On-chip Reference Variation. Added Out-of-Band Signaling.
02/28/12	1.6	Removed Dual Rank for DDR3 and DDR2; silicon support for dual rank reinstated.

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