Kintex-7 FPGA CES Errata

EN183 (v1.8) April 29, 2013 **Errata Notification**

Introduction

Thank you for participating in the Kintex™-7 FPGAs Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in Table 1. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in Table 1.

Table 1: **Devices Affected by These Errata**

Product Family	Device	JTAG ID (Revision Code)	Packages	Speed Grades
Kintex-7	XC7K160T CES	0	All	-1, -2
	XC7K325T CES	3		
	XC7K410T CES	0		
	XC7K420T CES	1		
	XC7K480T CES	1		

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

Block RAM

Single Block RAM Location Not Available (Applies only to XC7K410T Devices)

For only the XC7K410T devices listed in Table 1, the 36K block RAM location at `X4Y11` is not available for use. Use the CONFIG PROHIBIT=RAMB36_X4Y11 constraint in the UCF file in the ISE® Design Suite, or the set_property PROHIBIT TRUE [RAMB36_X4Y11] constraint in the SDC file in the Vivado™ Design Suite, to prevent the design tools from using this block RAM location.

XADC

XADC On-Chip Reference Variation (Applies only to XC7K325T, XC7K410T, XC7K420T, and XC7K480T Devices)

The XADC on-chip reference source can exceed the DS182, *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics* specification of 1.25V ±1.0% by an additional 0.5% (1.25V ±1.5%). See Answer Record 44971 for more information on the impact to XADC measurements when the on-chip reference source is used.

GTX Transceivers

QPLL Upper Band Usage (Applies only to the XC7K410T, XC7K420T, and XC7K480T Devices)

When using the QPLL upper band VCO mode (QPLL_CFG[6]=0), the $V_{MGTAVCC}$ power supply must be 1.05V ±30mV.

The operating frequency range ($F_{GCPLLRANGE2}$) of the QPLL upper band VCO mode (QPLL_CFG[6]=0) is 9.94 GHz to 10.3125 GHz. Due to this limitation, GTX data rates between 9.80 Gb/s to 9.93 Gb/s are not supported.

Out-of-Band Signaling (Applies only to the XC7K325T, XC7K410T, XC7K420T, and XC7K480T Devices)

The GTX transceiver circuitry for out-of-band (OOB) signaling is always enabled.

CPLL Power Down (Applies only to the XC7K325T, XC7K410T, XC7K420T, and XC7K480T Devices)

The GTX transceiver CPLL can become inoperative if conditions (1) and (2) persist for more than 8,000 hours:

1. Power has been applied to $V_{MGTAVCC}$ and $V_{MGTAVTT}$.
2. The device is in one of the following states:
   a. The FPGA is not configured.
   b. The FPGA is configured, but the transceiver is uninstantiated.
   c. The transceiver is instantiated, but the CPLL is held in power-down state.

When the QPLL is being used, enabling each CPLL will consume up to 30 mA on the $V_{MGTAVTT}$ supply and 20 mA on $V_{MGTAVCC}$. See Answer Record 45360 for more details.

GTX Transceiver Power-On/Power-Off

For the XC7K325T, XC7K410T, XC7K420T, and XC7K480T devices, if the recommended power sequences are not followed, then the GTX transceiver can become inoperative if both of the following conditions occur at the same time:

- $V_{MGTAVTT}$ is within its recommended operating range
- $V_{MGTAVCC}$ is at a voltage less than 0.4V for more than 10,000 cumulative hours

For the XC7K325T, XC7K410T, XC7K420T, and XC7K480T devices, an additional 100 mA per transceiver is drawn when $V_{MGTAVTT}$ is within its recommended operating range and $V_{MGTAVCC}$ is at a voltage less than 0.4V.

For the XC7K325T, XC7K410T, XC7K420T, and XC7K480T devices, if the recommended sequence is followed, while $V_{MGTAVCC}$ is powered within its recommended operating range and $V_{MGTAVTT}$ is below 0.7V, an additional 50 mA per transceiver is drawn from $V_{MGTAVCC}$.

Depending on the number of transceivers used, this extra current can be greater than the consumption reported in XPE.

Refer to Answer Record 47817 for more information.

IEEE Std 1149.1 and IEEE Std 1149.6 for GTX Transceivers (Applies only to the XC7K325T, XC7K410T, XC7K420T, and XC7K480T Devices)

IEEE Std 1149.1 (JTAG) boundary-scan test commands are not supported for the GTX transceiver. IEEE Std 1149.6 (ACJTAG) boundary-scan test commands EXTEST_PULSE and EXTEST_TRAIN are not supported.

GTX Transceiver Data Rate

The maximum GTX transceiver data rate (F_{GTXMAX}) is 6.6 Gb/s in the -1 speed grade.

Power

Static Power

All power supplies can exhibit up to 25% higher static current compared to the static current reported in XPE.

Also, up to an additional 30 mA per used transceiver, and up to an additional 50 mA per powered transceiver quad can be consumed by the $V_{MGTAVCC}$ supply. And, up to an additional 50 mA per powered transceiver quad can be consumed by the $V_{MGTAVTT}$ supply.

Design Tool Requirements

The XC7K325T, XC7K410T, XC7K420T, and XC7K480T devices require the following Xilinx Design Tools:

- Speed specification v1.03 or v1.04 (or later) of Xilinx® ISE® Design Suite 13.4/14.1 or Vivado Design Suite 2012.4 (or later) available at http://www.xilinx.com/support/download/. The -2 speed grade devices designed with ISE Design Suite 14.2 (or later) or Vivado Design Suite require a patch; refer to Answer Record 50906.

The XC7K160T requires the following Xilinx Design Tools:

- Speed specification v1.04 (or later) of Xilinx ISE Design Suite 14.1 or Vivado Design Suite 2012.4 (or later) available at http://www.xilinx.com/support/download/.

For all devices listed in Table 1:

- For GTX transceiver attribute updates, refer to Answer Record 45360.
- See Kintex-7 FPGA Answer Record 45696 for known issues and work-arounds for Xilinx Design Tools.

Operational Guidelines

Hardware Validation for Memory Interfaces

The memory interfaces listed in Table 2 have been validated in hardware across the operating conditions for these devices at the time of publication. See Answer Record 46521 for the latest hardware validation information.

Table 2: **Hardware Validated Memory Interfaces**

Type	Condition	Bank
DDR3	DIMM and Component Single Rank	HP and HR
QDRII+	Component Single Rank	
RLDRAMII	Component Single Rank	
DDR2	DIMM and Component Single Rank	

Traceability

Figure 1 shows an example device top mark for the devices listed in Table 1.

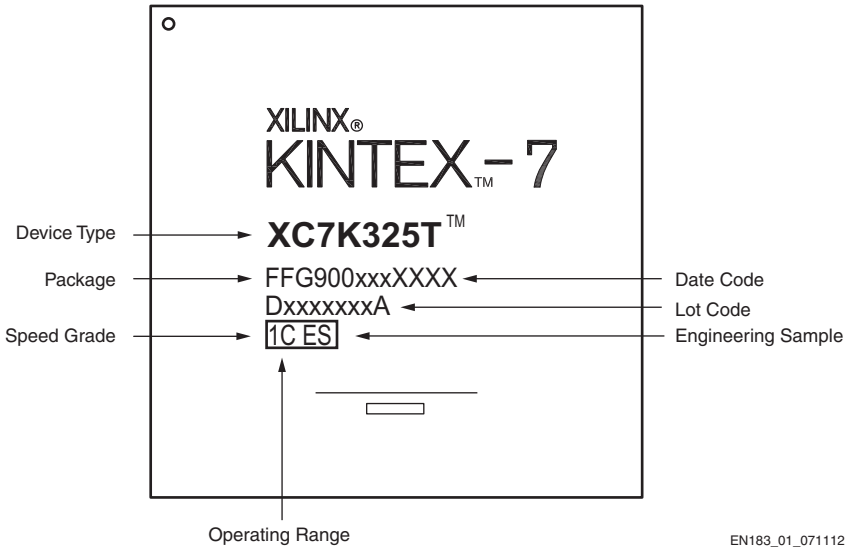

Figure 1: **Example Device Top Mark**

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact/index.htm.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
01/17/12	1.0	Initial Xilinx release.
01/18/12	1.0.1	Update document date to 2012.
02/16/12	1.1	Changed title; document pertains to all Kintex-7 CES devices. Updated Table 1 with XC7K480T CES and XC7K480T CES devices. Added Single Block RAM Location Not Available (Applies only to XC7K410T Devices). Removed the Dual Rank for DDR3 and DDR2 errata (no longer a deviation due to changes in MIG IP in ISE Design Suite 14.2 and Vivado Design Suite 2012.2.). Updated XADC Errata Table 2 and Static Power.
02/29/12	1.2	Updated XADC Errata Table 2, Added QPLL Upper Band Usage (Applies only to the XC7K410T, XC7K420T, and XC7K480T Devices). Added the Hardware Validation for Memory Interfaces operational guideline.
03/30/12	1.3	Added XC7K420T CES and temperature range to Table 1. Updated QPLL Upper Band Usage (Applies only to the XC7K410T, XC7K420T, and XC7K480T Devices), Table 2, and GTX Transceiver Power-On/Power-Off.
07/23/12	1.4	Updated Table 1 with XC7K160T CES device information. Updated Single Block RAM Location Not Available (Applies only to XC7K410T Devices). Removed XADC specifications except for XADC On-Chip Reference Variation (Applies only to XC7K325T, XC7K410T, XC7K420T, and XC7K480T Devices) because they are now documented in the data sheet: DS182, *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics*, v1.5, May 23, 2012. Updated Out-of-Band Signaling (Applies only to the XC7K325T, XC7K410T, XC7K420T, and XC7K480T Devices) and CPLL Power Down (Applies only to the XC7K325T, XC7K410T, XC7K420T, and XC7K480T Devices): Only apply to specific devices. Updated GTX Transceiver Power-On/Power-Off. Updated Design Tool Requirements. Removed Physical Interface Rate for Memory Interfaces because they are now documented in the data sheet: DS182, *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics*, v1.5, May 23, 2012. Added additional memories to Hardware Validation for Memory Interfaces in Table 2.
08/07/12	1.5	Updated Table 1; XC7K160T is extended to all packages. Updated GTX Transceiver Power-On/Power-Off; restored the following: “An additional 100 mA per transceiver is drawn when $V_{MGTAVTT}$ is within its recommended operating range and $V_{MGTAVCC}$ is at a voltage less than 0.4V.”
10/25/12	1.6	Removed recommended sequence from GTX Transceiver Power-On/Power-Off because it was included in the data sheet DS182, *Kintex-7 FPGAs Data Sheet: DC and Switching Characteristics*, v1.6, July 25, 2012. Added GTX Transceiver Data Rate. Clarified Design Tool Requirements. Updated Table 2.
01/29/13	1.7	Updated IEEE Std 1149.1 and IEEE Std 1149.6 for GTX Transceivers (Applies only to the XC7K325T, XC7K410T, XC7K420T, and XC7K480T Devices).
04/29/13	1.8	Updated Design Tool Requirements.

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