Introduction

Thank you for participating in the Artix™-7 FPGAs Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in Table 1. Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in Table 1.

Table 1: **Devices Affected by These Errata**

Product Family	Device	JTAG ID (Revision Code)	Packages	Speed Grades
Artix-7	XC7A100T CES9937	0	CSG324	-1, -2
			FGG676	
	XC7A200T CES9937	0	SBG484	-1, -2
			FBG676	
			FFG1156	

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

XADC

ADC Accuracy

The XADC Gain Error is ±0.5% max and the XADC Offset Error is ±8 LSBs max.

IEEE Std 1149.1 Boundary-Scan

IEEE Std 1149.1 for Dedicated and SelectIO Resources (Applies only to XC7A100T Device)

IEEE Std 1149.1 (JTAG) boundary-scan test commands SAMPLE, PRELOAD, EXTEST, and HIGHZ are not functional. All other JTAG commands, including device configuration and the ChipScope™ debugging tool, function as expected.

Power

Static Power

For XPE 14.2, the V_{CCAUX} power supply can exhibit up to 25% higher static current compared to the reported static current.

Design Tool Requirements

The devices listed in Table 1, unless otherwise specified, require the following Xilinx Design Tools:

- Speed specification v1.04 (or later) of Xilinx® ISE® Design Suite 14.2 or Vivado™ Design Suite 2012.2 (or later) available at http://www.xilinx.com/support/download/.
- For GTP transceiver attribute updates, refer to Answer Record 47852.
- See Artix-7 FPGA Answer Record 51192 for the most current known issues and work-arounds for Xilinx Design Tools.

Traceability

Figure 1 shows an example device top mark for the devices listed in Table 1.

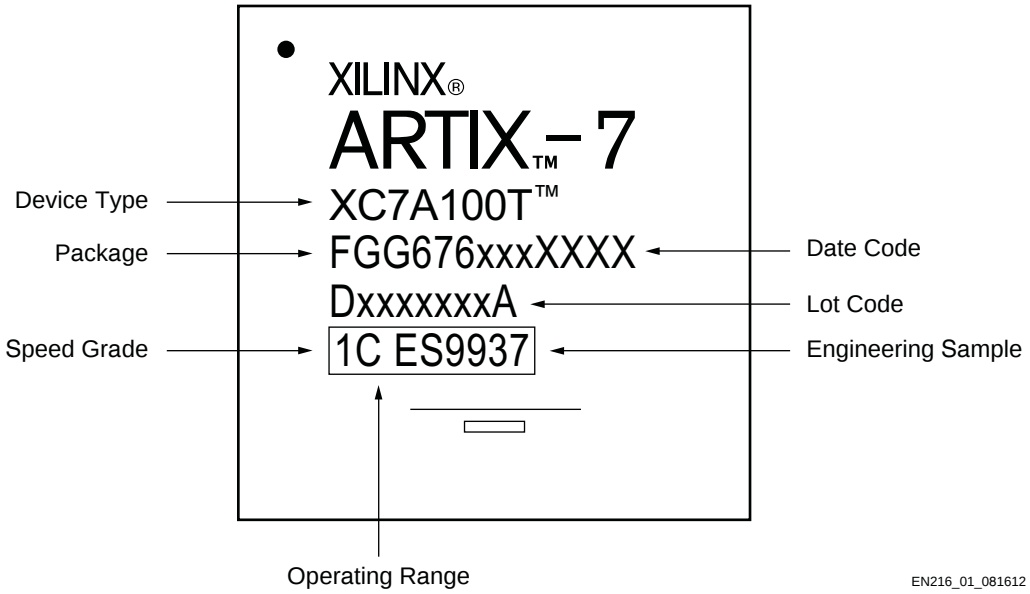

Figure 1: **Example Device Top Mark**

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact/index.htm.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/04/12	1.0	Initial Xilinx release.
09/24/12	1.1	In Table 1, extended -2 speed grade to all packages and added the FFG1156 package for the XC7A200T. Removed GTP Transceivers Power-On/Off Power Supply Sequencing (Applies only to XC7A100T FGG676 and XC7A200T Devices) because it is now documented in DS181, *Artix-7 FPGAs Data Sheet: DC and Switching Characteristics* (v1.4) September 20, 2012.

Notice of Disclaimer

Engineering Sample Disclaimer