

Introduction

Thank you for participating in the Artix™-7 FPGAs Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the devices listed in [Table 1](#). Although Xilinx has made every effort to ensure the highest possible quality, these devices are subject to the limitations described in the following errata.

Devices

These errata apply to the devices shown in [Table 1](#).

Table 1: Devices Affected by These Errata

Product Family	Device	JTAG ID (Revision Code)	Packages	Speed Grades
Artix-7	XC7A100T CES9937	0	CSG324	-1, -2
			FGG676	
	XC7A200T CES9937	0	SBG484	-1, -2
			FBG676	
		FFG1156		

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

XADC

ADC Accuracy

The XADC Gain Error is $\pm 0.5\%$ max and the XADC Offset Error is ± 8 LSBs max.

IEEE Std 1149.1 Boundary-Scan

IEEE Std 1149.1 for Dedicated and SelectIO Resources (Applies only to XC7A100T Device)

IEEE Std 1149.1 (JTAG) boundary-scan test commands SAMPLE, PRELOAD, EXTEST, and HIGHZ are not functional. All other JTAG commands, including device configuration and the ChipScope™ debugging tool, function as expected.

Power

Static Power

For XPE 14.2, the V_{CCAUX} power supply can exhibit up to 25% higher static current compared to the reported static current.

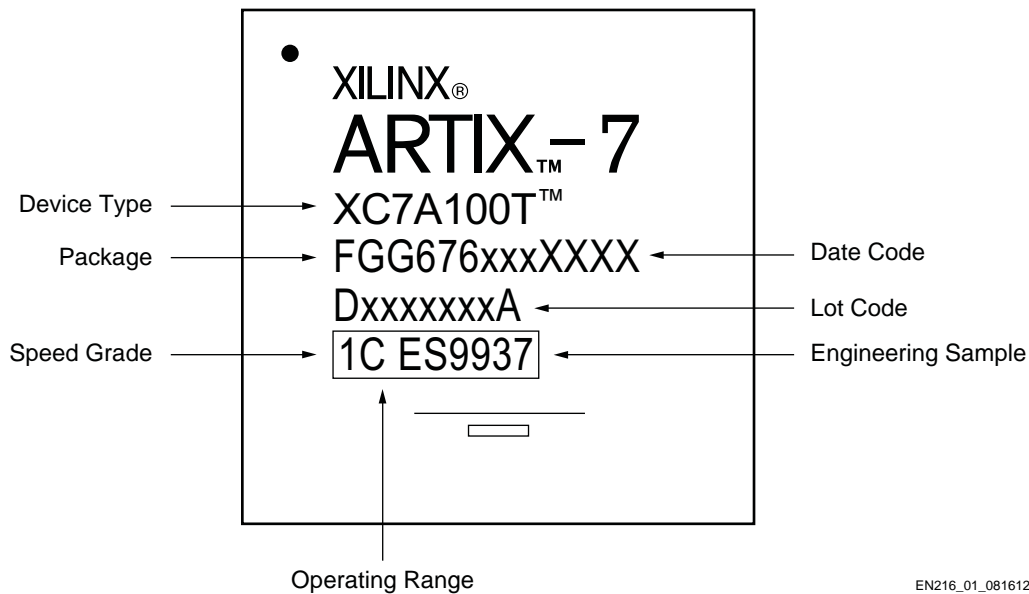
Design Tool Requirements

The devices listed in [Table 1](#), unless otherwise specified, require the following Xilinx Design Tools:

- Speed specification v1.04 (or later) of Xilinx® ISE® Design Suite 14.2 or Vivado™ Design Suite 2012.2 (or later) available at <http://www.xilinx.com/support/download/>.
- For GTP transceiver attribute updates, refer to [Answer Record 47852](#).
- See Artix-7 FPGA [Answer Record 51192](#) for the most current known issues and work-arounds for Xilinx Design Tools.

Traceability

[Figure 1](#) shows an example device top mark for the devices listed in [Table 1](#).



EN216_01_081612

Figure 1: Example Device Top Mark

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: <http://www.xilinx.com/support/clearxpress/websupport.htm> or your Xilinx Sales Representative: <http://www.xilinx.com/company/contact/index.htm>.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/04/12	1.0	Initial Xilinx release.
09/24/12	1.1	In Table 1 , extended -2 speed grade to all packages and added the FFG1156 package for the XC7A200T. Removed GTP Transceivers Power-On/Off Power Supply Sequencing (Applies only to XC7A100T FGG676 and XC7A200T Devices) because it is now documented in DS181, <i>Artix-7 FPGAs Data Sheet: DC and Switching Characteristics</i> (v1.4) September 20, 2012.

Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at <http://www.xilinx.com/warranty.htm>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: <http://www.xilinx.com/warranty.htm#critapps>.

Engineering Sample Disclaimer

ENGINEERING SAMPLE (ES) DEVICES ARE MADE AVAILABLE SOLELY FOR PURPOSES OF RESEARCH, DEVELOPMENT AND PROTOTYPING. ALL ES DEVICES ARE SOLD "AS-IS" WITH NO WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED. XILINX DOES NOT WARRANT THAT ES DEVICES ARE FULLY VERIFIED, TESTED, OR WILL OPERATE IN ACCORDANCE WITH DATA SHEET SPECIFICATIONS. XILINX DISCLAIMS ANY OBLIGATIONS FOR TECHNICAL SUPPORT AND BUG FIXES. XILINX SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING WITHOUT LIMITATION DIRECT, INDIRECT, INCIDENTAL, SPECIAL, RELIANCE, OR CONSEQUENTIAL DAMAGES ARISING FROM OR IN CONNECTION WITH THE USE OF ES DEVICES IN ANY MANNER WHATSOEVER, EVEN IF XILINX HAS BEEN ADVISED OF THE POSSIBILITY THEREOF. XILINX MAKES NO REPRESENTATION THAT ES DEVICES PROVIDE ANY PARTICULAR FUNCTIONALITY, OR THAT ES DEVICES WILL MEET THE REQUIREMENTS OF A PARTICULAR USER APPLICATION. XILINX DOES NOT WARRANT THAT ES DEVICES ARE ERROR-FREE, NOR DOES XILINX MAKE ANY OTHER REPRESENTATIONS OR WARRANTIES, WHETHER EXPRESS OR IMPLIED, STATUTORY OR OTHERWISE, INCLUDING, WITHOUT LIMITATION, IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. THE FOREGOING STATES THE ENTIRE LIABILITY OF XILINX WITH RESPECT TO ES DEVICES.