LogiCORE IP AHB Lite to AXI Bridge v1.00a

DS825 October 16, 2012 **Product Specification**

Introduction

The AMBA® (Advanced Microcontroller Bus Architecture) AHB-Lite (Advanced High Performance Bus) to AXI (Advanced extensible interface) bridge translates AHB-Lite transactions into AXI4 transactions. It functions as an AHB-Lite slave on the AHB bus and as an AXI master on the AXI bus.

Features

The Xilinx® AHB Lite to AXI bridge is a soft IP core with the following features:

- AXI interface is based on the AXI4 specification
- AHB-Lite interface based on the AHB specification
- Supports 1:1 (AXI:AHB) synchronous clock ratio
- AHB and AXI data widths are the same and either 32 or 64 bit based on the configuration
- Supports narrow transfers on the AHB interface
- Supports burst termination on the AHB during which dummy transfers are initiated on the AXI interface
- Timeout feature to indicate no response from AXI slave during write and read transactions

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family(1)	Zynq™-7000(2), Virtex®-7(3), Kintex™-7(3) Artix™(3)-7, Virtex -6(4) Spartan®-6(5)				
Supported User Interfaces	AXI4, AHB-Lite				
	Resources and Frequency				
Configuration	**LUTs**	**FFs**	**DSP Slices**	**Max. Freq**	**Block RAMS**
Configuration 1	See Table 6, Table 7, Table 8, and Table 9.				0
Provided with Core					
Design Files	ISE: VHDL Vivado: RTL				
Example Design	Not Provided				
Test Bench	Not Provided				
Constraints File	None				
Simulation Model	None				
Supported S/W Driver	N/A				
Tested Design Tools(6)					
Design Entry Tools	Vivado™ Design Suite v2012.3(7) Xilinx® Platform Studio (XPS) v14.3				
Simulation	Mentor Graphics ModelSim				
Synthesis Tools	Vivado Synthesis Xilinx Synthesis Technology (XST)				
Support					
Provided by Xilinx at www.xilinx.com/support					

Notes:

1. For a complete listing of supported derivative devices, see the IDS Embedded Edition Derivative Device Support.
2. Supported in ISE® Design Suite implementations only.
3. For more information, see the *7 Series FPGAs Overview* [Ref 2].
4. For more information, see the *Virtex-6 Familiy Overview* [Ref 3].
5. For more information, see the *Spartan-6 Family Overview* [Ref 4].
6. For a listing of the supported tool versions, see the Xilinx Design Tools: Release Notes Guide.
7. Supports 7 series devices only.

Functional Description

The AHB Lite to AXI Bridge translates AHB-Lite transactions into AXI4 transactions. The bridge functions as an AHB-Lite slave on the AHB bus and as an AXI master on the AXI bus. AHB Lite to AXI Bridge block diagram is shown in Figure 1 and described in following sections.

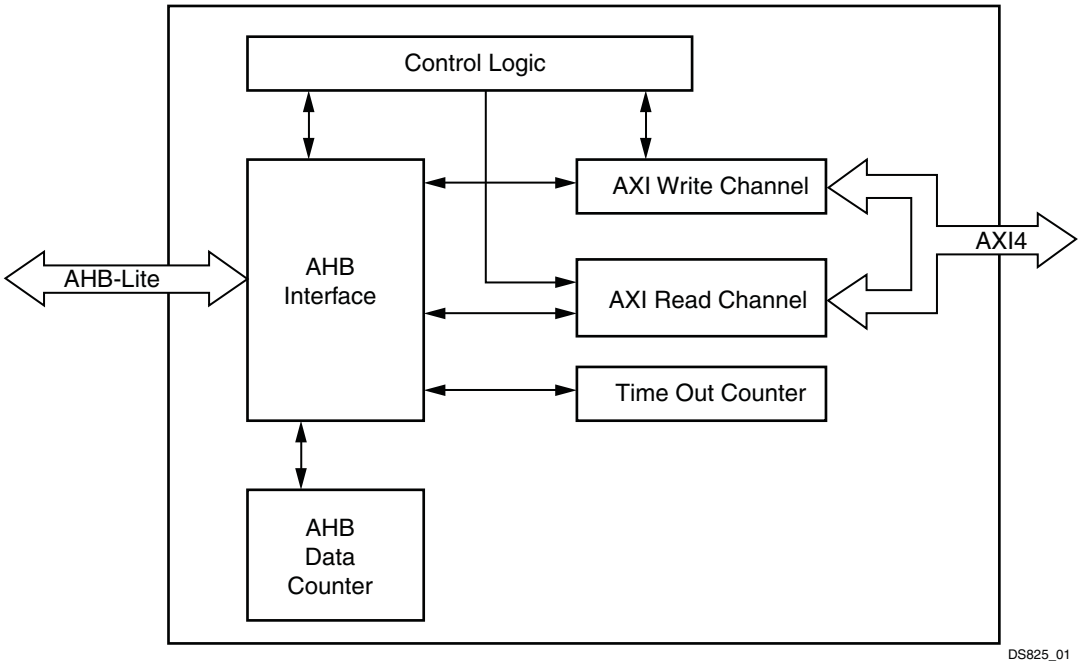

Figure 1: **AHB Lite to AXI Bridge Block Diagram**

AHB Interface

The AHB-Lite Slave module provides the AHB-Lite slave interface on the AHB bus side. This module registers the AHB side control signals when a new transfer is initiated. Generates the HREADY based on the current transfer progress on the AXI side and burst termination seen on AHB side.

AHB Data counter

This module counts the valid data received from AHB for the write transfers. The count value is used to limit the HREADY generation after the required number of samples received for the current transfer.

Control Logic

The control logic state machine is the central controlling unit which instructs the submodules on the progress of the transfer. It detects the characteristics of the transfer initiated on the AHB side (Read/Write, Burst, Single) and instructs the submodules to map the current AHB transfer to AXI transfer appropriately.

AXI Write Channel

The AXI Write channel controls the AXI Write transaction channels (Write Address channel, Write Data channel and Write response channel) based on the instruction from Control logic. The Write strobes are appropriately controlled during narrow transfers and burst termination on the AHB as per the protocol, the AXI Write channel completes the transfers with dummy data if required, when burst-termination is seen on the corresponding AHB transfer.

AXI Read Channel

The AXI Read channel controls the AXI Read transaction channels (Read Address channel and Read Data channel) based on the instruction from Control logic. As per the protocol, the AXI Read channel completes the transfers by discarding the data if required when burst-termination is seen on the corresponding AHB transfer

Time Out Module

The time out module generates the time out when the AXI slave is not responding to the transaction initiated by the AHB master. This is parameterized and generates the time out only when C_AHB_AXI_TIMEOUT value is nonzero. Time out module waits C_AHB_AXI_TIMEOUT number of AHB clocks for AXI slave response and then generates the time out if AXI slave is not responding.

I/O Signals

The I/O signals of the AHB Lite to AXI Bridge are shown in Table 1.

Table 1: **I/O Signal Description**

Port	Signal Name	Interface	I/O	Initial State	Description
AHB-Lite Signals					
P1	S_AHB_HCLK	AHB	I	-	AHB Clock.
P2	S_AHB_HRESETN	AHB	I	-	AHB active-Low reset. M_AXI_ARESETN is tied to S_AHB_HRESETN
P3	S_AHB_HSEL	AHB	I	-	Slave select signal for AHB interface
P4	S_AHB_HADDR[C_S_AHB_ADDR_WIDTH-1:0]	AHB	I	-	AHB Address bus
P5	S_AHB_HPROT[3:0]	AHB	I	-	Protection type. This signal indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
P6	S_AHB_HTRANS[1:0]	AHB	I	-	AHB Transfer Type (NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY.)
P7	S_AHB_HSIZE[2:0]	AHB	I	-	Indicates the size of the transfer
P8	S_AHB_HWRITE	AHB	I	-	Direction. This signal indicates an AHB write access when HIGH and an AHB read access when LOW.
P9	S_AHB_HBURST[2:0]	AHB	I	-	Burst type. Indicates if the transfer forms part of the burst.
P10	S_AHB_HWDATA[C_S_AHB_DATA_WIDTH -1:0]	AHB	I	-	Write data.The write data bus is used to transfer data from the master to the bus slaves during write operations
P11	S_AHB_HREADY_OUT	AHB	O	1	Transfer done. The AHB slave uses this signal to extend an AHB transfer.
P12	S_AHB_HREADY_IN	AHB	I	-	HREADY input signals from interconnect.
P13	S_AHB_HRDATA[C_S_AHB_DATA_WIDTH -1:0]	AHB	O	0	Read Data. The slave drives this bus during read cycles when S_AHB_HWRITE is LOW.
P14	S_AHB_HRESP	AHB	O	0	Provides information on the status of the transfer.
AXI Interface System Signals					
P15	M_AXI_ACLK	System	O	-	AXI clock.M_AXI_ACLK is tied to S_AHB_HCLK
P16	M_AXI_ARESETN	System	O	-	AXI active-Low reset.

Table 1: **I/O Signal Description *(Cont'd)***

Port	Signal Name	Interface	I/O	Initial State	Description
AXI Write Address Channel Signals					
P17	M_AXI_AWID[C_M_AXI_THREAD_ID_WIDTH-1:0]	AXI4	O	0	Write address ID.This signal is the identification tag for the write address group of signals
P18	M_AXI_AWLEN[3:0]	AXI4	O	0	Burst length.The burst length gives the exact number of transfers in a burst
P19	M_AXI_AWSIZE[2:0]	AXI4	O	0	Burst size.This signal indicates the size of each transfer in the burst
P20	M_AXI_AWBURST[1:0]	AXI4	O	0	Burst type.The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated.
P21	M_AXI_AWADDR[C_M_AXI_ADDR_WIDTH-1:0]	AXI4	O	0	AXI Write address. The write address bus gives the address of the first transfer in a write burst transaction
P22	M_AXI_AWCACHE[3:0]	AXI4	O	0	Cache type.This signal indicates the buffer, cache, write-through, write-back, and allocate attributes of the transaction.
P23	M_AXI_AWPROT[2:0]	AXI4	O	2	Protection type. This signal indicates the normal, privileged, or secure protection level of the write transaction and whether the transaction is a data access or an instruction access. The default value is normal, non secure, data access
P24	M_AXI_AWVALID	AXI4	O	0	Write address valid. This signal indicates that valid write address and control information are available
P25	M_AXI_AWREADY	AXI4	I	-	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals
P26	M_AXI_AWLOCK[1:0]	AXI4	O	0	Lock Type, this signal provides additional information about the atomic characteristics of the transfer.
AXI Write Data Channel Signals					
P27	M_AXI_WDATA[C_M_AXI_DATA_WIDTH-1:0]	AXI4	O	0	Write data bus.
P28	M_AXI_WSTRB[C_M_AXI_DATA_WIDTH/8-1:0]	AXI4	O	0	Write strobes. This signal indicates which byte lanes to update in memory.
P29	M_AXI_WLAST	AXI4	O	0	Write last. This signal indicates the last transfer of a burst transaction.
P30	M_AXI_WVALID	AXI4	O	0	Write valid. This signal indicates that valid write data and strobes are available.
P31	M_AXI_WREADY	AXI4	I	-	Write ready. This signal indicates that the slave can accept the write data.
AXI Write Response Channel Signals					
P32	M_AXI_BID[C_M_AXI_THREAD_ID_WIDTH-1:0]	AXI4	I	-	Response ID.This signal is the identification tag for the write response signals.
P33	M_AXI_BRESP[1:0]	AXI4	I	-	Write response. This signal indicates the status of the write transaction.
P34	M_AXI_BVALID	AXI4	I	-	Write response valid. This signal indicates that a valid write response is available.
P35	M_AXI_BREADY	AXI4	O	0	Response ready. This signal indicates that the master can accept the response information.
AXI Read Address Channel Signals					
P36	M_AXI_ARID[C_M_AXI_THREAD_ID_WIDTH-1:0]	AXI4	O	0	Read address ID.This signal is the identification tag for the read address group of signals.

Table 1: **I/O Signal Description *(Cont'd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P37	M_AXI_ARADDR[C_M_AXI_ADDR_WIDTH -1:0]	AXI4	O	0	Read address. The read address bus gives the initial address of a read burst transaction.
P38	M_AXI_ARPROT[2:0]	AXI4	O	2	Protection type. This signal provides protection unit information for the read transaction. The default value is normal, non secure, data access.
P39	M_AXI_ARCACHE[3:0]	AXI4	O	0	Cache type.This signal provides additional information about the cache characteristics of the transfer.
P40	M_AXI_ARVALID	AXI4	O	0	Read address valid. When High, this signal indicates that the read address and control information is valid. The signal remains stable until the address acknowledgement signal, M_AXI_ARREDY, is High.
P41	M_AXI_ARLEN[3:0]	AXI4	O	0	Burst length.The burst length gives the exact number of transfers in a burst.
P42	M_AXI_ARSIZE[2:0]	AXI4	O	0	Burst size.This signal indicates the size of each transfer in the burst.
P43	M_AXI_ARBURST[1:0]	AXI4	O	0	Burst type. The burst type, coupled with the size information, determines how the address for each transfer within the burst is calculated.
P44	M_AXI_ARLOCK[1:0]	AXI4	O	0	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P45	M_AXI_ARREADY	AXI4	I	-	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals.
AXI Read Data Channel Signals					
P46	M_AXI_RID[C_M_AXI_THREAD_ID_WIDTH-1:0]	AXI4	I	-	Read ID tag.This signal is the identification tag for the read data group of signals.
P47	M_AXI_RDATA[C_M_AXI_DATA_WIDTH -1:0]	AXI4	I	-	Read data bus
P48	M_AXI_RRESP[1:0]	AXI4	I	-	Read response. This signal indicates the status of the read transfer.
P49	M_AXI_RVALID	AXI4	I	-	Read valid. This signal indicates that the required read data is available and the read transfer can complete.
P50	M_AXI_RLAST	AXI4	I	-	Read last.This signal indicates the last transfer in a read burst.
P51	M_AXI_RREADY	AXI4	O	0	Read ready. This signal indicates that the master can accept the read data and response information.

Design Parameters

Table 2 shows the design parameters of the AHB Lite to AXI Bridge.

Inferred Parameters

In addition to the parameters listed in Table 2, there are also parameters that are inferred for each AXI interface in the EDK tools. Through the design, these EDK-inferred parameters control the behavior of the AXI Interconnect. For a complete list of the interconnect settings related to the AXI interface, see the *AXI Interconnect IP Data Sheet* [Ref 5].

Table 2: **Design Parameters**

Generic	Feature/Description	Parameter Name	Allowable Values	Default Values	VHDL Type
System Parameter					
G1	Target FPGA family	C_FAMILY	virtex6, spartan6,virtex7, kintex7,artix7,zynq	virtex6	string
G2	AHB Address bus width	C_S_AHB_ADDR_WIDTH	32	32	integer
G3	AXI Address bus width	C_M_AXI_ADDR_WIDTH	32	32	integer
G4	AHB Data bus width	C_S_AHB_DATA_WIDTH	32,64	32(1)	integer
G5	AXI Data bus width	C_M_AXI_DATA_WIDTH	32,64	32(1)	integer
G6	Time out value	C_AHB_AXI_TIMEOUT	0,16,32,64, 128,256(2)	0	integer
G7	Narrow transfer support	C_M_AXI_SUPPORTS_NARROW_BURST	0,1(3)	0	integer
AXI Parameters					
G8	AXI Interface type	C_M_AXI_PROTOCOL	axi4lite	axi4(4)	string
G9	AXI ID width	C_M_AXI_THREAD_ID_WIDTH	1 to 16	1	integer

Notes:

1. The same address and data width is used on both AHB Lite and AXI interfaces.
2. The timeout module is parameterized and does not generate timeout if C_AHB_AXI_TIMEOUT is set to 0.
3. Narrow transfer is not supported when the generic is set to 0; supported when set to 1.
4. This generic is needed by the system. Only the AXI4 interface is supported by the AHB Lite to AXI Bridge.

Parameter - I/O Signal Dependencies

The dependencies between the AHB Lite to AXI Bridge core design parameters and I/O signals are described in Table 3. In addition, when certain features are parameterized out of the design, the related logic is no longer a part of the design. The unused input signals and related output signals are set to a specified value.

Table 3: **Parameter - I/O Signal Dependencies**

Generic or Port	Name	Affects	Depends	Relationship Description
Design Parameters				
G2	C_S_AHB_ADDR_WIDTH	P4,P21,P38	-	Current generic value is fixed to 32.
G3	C_M_AXI_ADDR_WIDTH	P4,P21,P38	-	Current generic value is fixed to 32.
G4	C_S_AHB_DATA_WIDTH	P10,P13,P28, P29,P48	-	Varies the width of the read, write data buses, and write strobes
G5	C_M_AXI_DATA_WIDTH	P10,P13,P28, P29,P48	-	Varies the width of the read, write data buses and write strobes
G9	C_M_AXI_THREAD_ID_WIDTH	P17,P27,P33,P37,P47	-	Width of the ID tags.
I/O Signals				
P4	S_AHB_HADDR		G2	Width varies the size of the address bus
P10	S_AHB_HWDATA		G4	Width varies the size of the data bus
P13	S_AHB_HRDATA		G4	Width varies the size of the data bus
P21	M_AXI_AWADDR		G3	Width varies the size of the address bus
P38	M_AXI_ARADDR		G3	Width varies the size of the address bus
P28	M_AXI_WDATA		G5	Width varies the size of the data bus
P29	M_AXI_WSTRB		G5	Width varies size of the write strobe
P48	M_AXI_RDATA		G5	Width varies the size of the data bus
P17	M_AXI_AWID		G9	Write Address channel ID width
P32	M_AXI_BID		G9	Write response channel ID width
P36	M_AXI_ARID		G9	Read address channel ID width
P46	M_AXI_RID		G9	Read data channel ID width

Design Details

Clocking

The AHB Lite to AXI Bridge is a synchronous design and uses the S_AHB_HCLK at both AHB-Lite and AXI interfaces.

Reset

S_AHB_HRESETN is a synchronous active-Low reset input that resets the AHB Lite to AXI Bridge upon assertion. The S_AHB_HRESETN is also used to reset the AXI interface.

Memory Mapping

The AXI memory map and the AHB-Lite memory map are one single complete 32-bit (4 GB) memory space. The AHB Lite to AXI Bridge does not modify the address hence, the address that is presented on the AXI is exactly as received on the AHB Lite.

Data Width

The bridge supports the same data width on either sides of the bridge interface (AHB and AXI). The data width selection (either 32 or 64) can be made using the generic, C_S_AHB_DATA_WIDTH.

Narrow Transfers

The transactions where the transfer size is narrower than the data width, C_S_AHB_DATA_WIDTH, are treated as narrow transfers. Narrow transfer support is parameterized in the AHB-Lite to AXI bridge. Narrow transfers on AHB are supported and can be transferred to/from AXI, when C_M_AXI_SUPPORTS_NARROW_BURST parameter is set to 1. The 8/16/32 bit data can be transferred when C_M_AXI_SUPPORTS_NARROW_BURST is 1, C_S_AHB_DATA_WIDTH is 32. When C_M_AXI_SUPPORTS_NARROW_BURST is 0, C_S_AHB_DATA_WIDTH is 32 then the 32-bit data transfers are only allowed.

The 8/16/32/64 bit data can be transferred when C_M_AXI_SUPPORTS_NARROW_BURST is 1, C_S_AHB_DATA_WIDTH is 64. When C_M_AXI_SUPPORTS_NARROW_BURST is 0, C_S_AHB_DATA_WIDTH is 64 then the 64-bit data transfers are only allowed.

AHB Lite Response Signaling

OKAY and ERROR responses are supported. SPLIT and RETRY responses are not supported. SLVERR,DECERR and timeout error (if used) from AXI interface are mapped to ERROR response on the AHB Lite interface.

AXI Response Signaling

The responses expected from AXI slave are OKAY, SLVERR, and DECERR. EXOKAY response is not expected as exclusive accesses requests are not initiated by the AXI master interface.

Endianness

Both AHB and AXI interfaces are little endian.

Address/Data Translation

No address/data translation/conversion from AHB-Lite to AXI takes place inside AHB Lite to AXI Bridge. The write/read address from AHB Lite is passed to AXI address. AHB Lite write data is passed on to AXI and AXI read data is passed on to AHB Lite read data.

Data width Selection on AHB and AXI Interface

The data width of the AHB and AXI interfaces are selected to the same value either 32 or 64 bits based on the generic C_S_AHB_DATA_WIDTH.

Bridge Timeout Condition

Time out logic is parameterized in AHB-Lite to AXI Bridge, time out is generated when the parameter C_AHB_AXI_TIMEOUT value is 16/32/64/128/256. When a request is issued from AHB the bridge translates this request into corresponding AXI transfer and requests on AXI. If this request is not responded by AXI, the time out logic waits for time out period and automatically responds with ERROR on AHB side. If the C_AHB_AXI_TIMEOUT parameter value is '0' then it is assumed that AXI slave always responds when a transfer is requested and no time out logic exists that automatically responds on AHB side when AXI slave does not respond, the AHB-Lite to AXI bridge waits indefinitely for the AXI slave response.

- When C_AHB_AXI_TIMEOUT is selected and the timeout condition occurs, the transaction on the AXI side is closed as follows:
  - for write transactions AWVALID/WVALID are deasserted without waiting for AWREADY/WREADY. If the write transaction is in the response phase BREADY is deasserted.
  - For a read transaction ARREADY/READY are deasserted.
- Because the bridge gives the same ERROR response for slave error cases and time out cases, it is mandatory to provide a reset to the bridge after the ERROR response is detected from the bridge when the time out logic is activated (C_AHB_AXI_TIMEOUT is nonzero).
- When the Time out logic is not activated is not required to give reset to the bridge when an ERROR response is seen for a particular transaction (C_AHB_AXI_TIMEOUT is zero).

Transaction Mapping from AHB to AXI

The different possible transactions from AHB Lite interface to AXI interface are mapped in Table 4.

Table 4: **Transaction Mapping from AHB Lite to AXI Transaction**

AHB lite Transaction	AXI Transaction		Description
HBURST	AWBURST/ ARBURST	AWLEN/ ARLEN	
SINGLE	INCR	0	Single transfers on AHB are converted to INCR of length 0
INCR	INCR	0(1)	Indefinite length increment transfers on AHB are converted to INCR of length 0
WRAP4	WRAP	3	WRAP4 transfer on AHB is converted to WRAP transfer of length 3 on AXI side.
INCR4	INCR	3	INCR4 transfer on AHB is converted to INCR transfer of length 3 on AXI side.
WRAP8	WRAP	7	WRAP8 transfer on AHB is converted to WRAP transfer of length 7 on AXI side.
INCR8	INCR	7	INCR8 transfer on AHB is converted to INCR transfer of length 7 on AXI side.
WRAP16	WRAP	15	WRAP16 transfer on AHB is converted to WRAP transfer of length 15 on AXI side.
INCR16	INCR	15	INCR16 transfer on AHB is converted to INCR transfer of length 15 on AXI side.

Notes:

1. Infinite length of INCR transfers from the AHB Lite interface are initiated as INCR transactions of burst length 0. Each transaction on AHB is initiated as separate transfer on the AXI side.

Mapping of Protection signal from AHB LITE to AXI Interface

Table 5: **Mapping of Protection Signals from AHB Lite Interface to AXI Interface**

AHB Signal		AXI Signal(1)	
Signal	Value	Signal (AR/AW)	Value
HPROT[0]	0	PROT[2]	1
HPROT[0]	1	PROT[2]	0
HPROT[1]	0	PROT[0]	0
HPROT[1]	1	PROT[0]	1
HPROT[2]	0	CACHE[0]	0
HPROT[2]	1	CACHE[0]	1

Notes:

1. Values which are not mapped takes the default value for outputs. Input values which are not considered for mapping are ignored during mapping and outputs are set to default values for such inputs.

Register Descriptions

There are no registers implemented in AHB Lite to AXI Bridge.

Not Supported Features/Limitations

AHB Slave Interface

- Greater than 64-bit data width.
- SPLIT and RETRY responses.

AXI4 Master Interface

- Greater than 64-bit data width
- Register and posted write implementation
- Fixed address burst (as there is no such transaction in AHB)
- Locked, Barrier, trust zone, exclusive operations
- Out-of-order transaction completion
- Exclusive accesses initiation

Timing Diagrams

The timing diagram shown in the subsequent figures illustrate the operation for various read and write transfers.

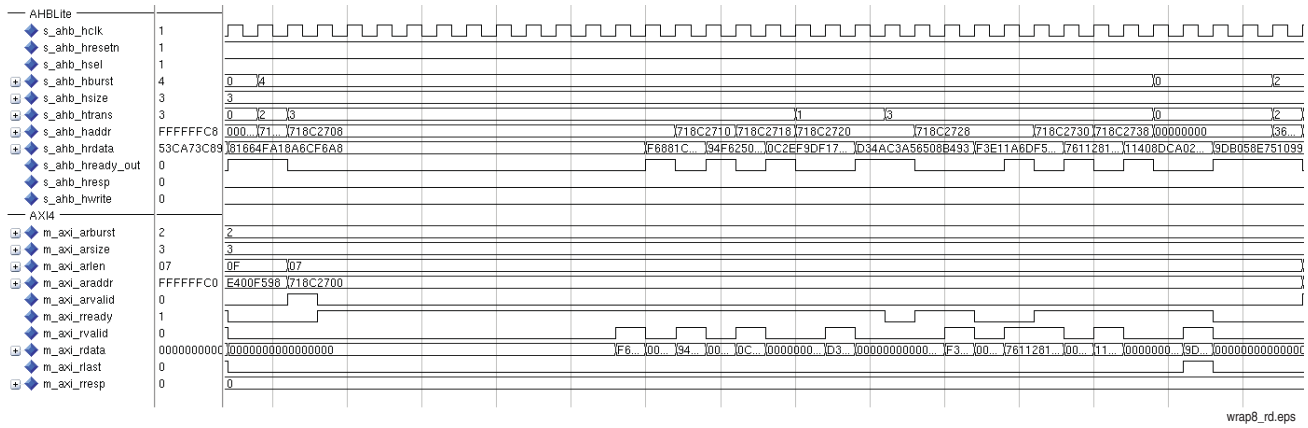

Figure 2: **Read Transfer With Burst Type WRAP8**

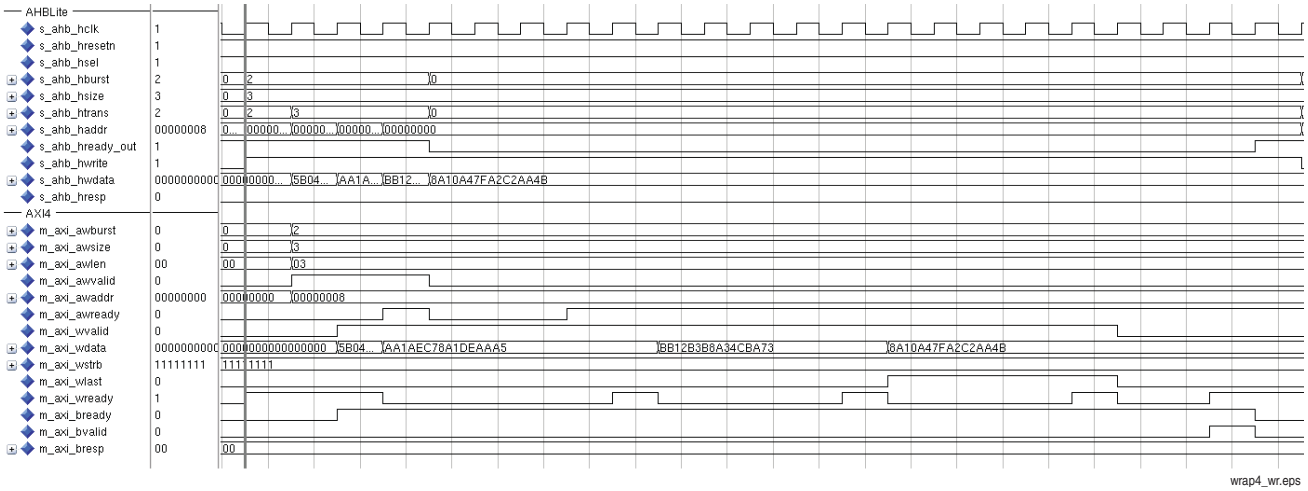

Figure 3: **Write Transfer With Burst Type WRAP4**

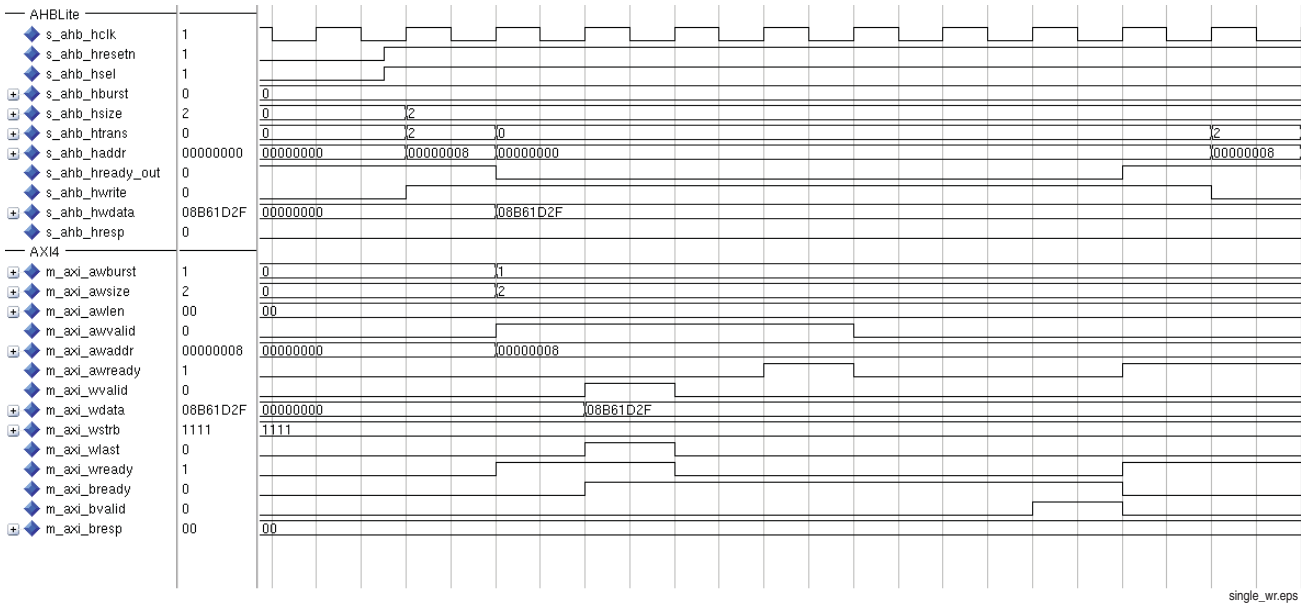

Figure 4: **Write Transfer With Burst Type SINGLE**

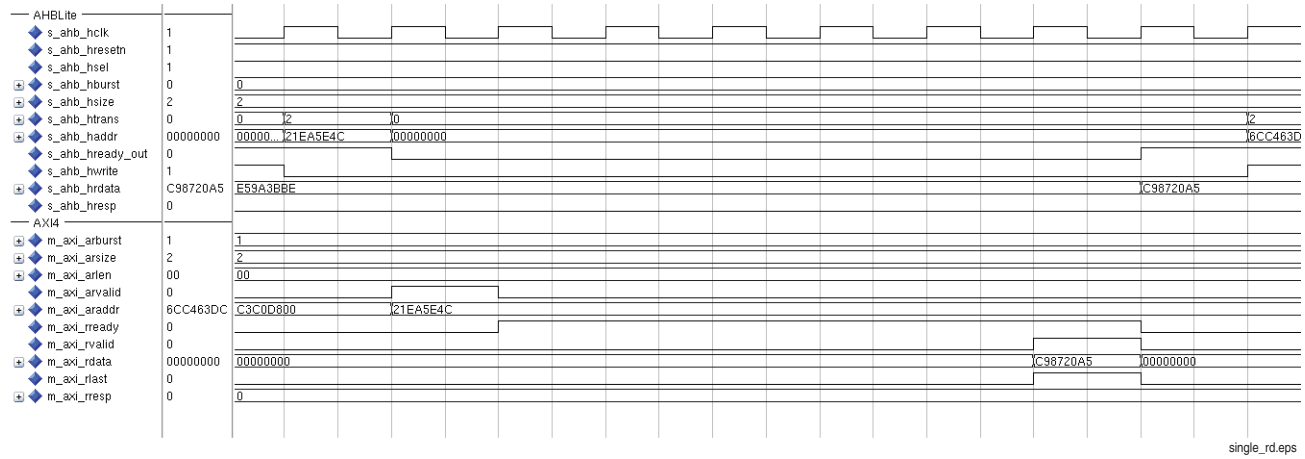

Figure 5: **Read Transfer With Burst Type SINGLE**

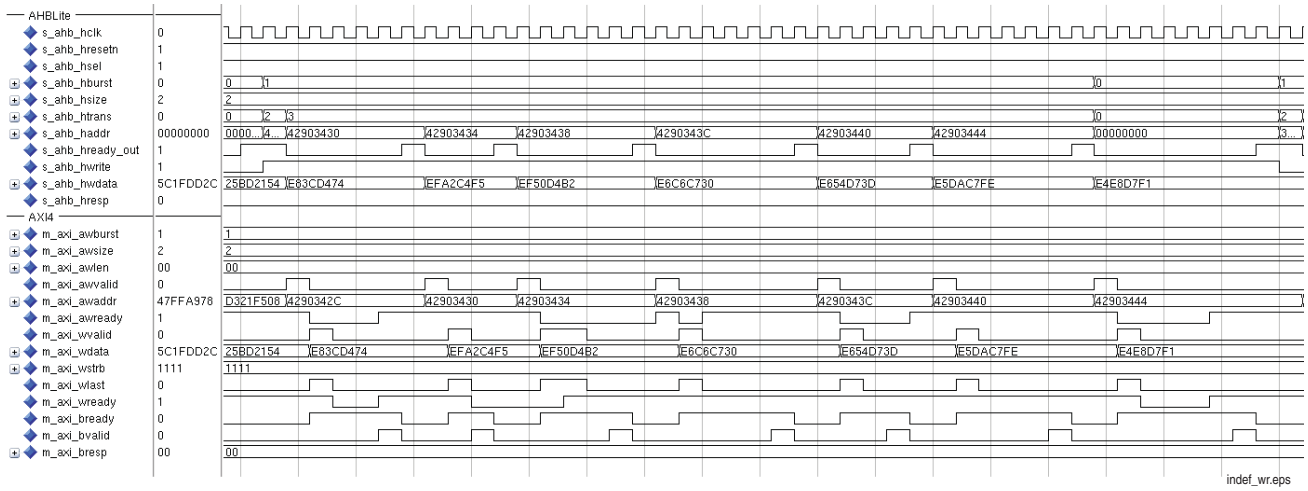

Figure 6: **Write Transfer With Burst Type INCR**

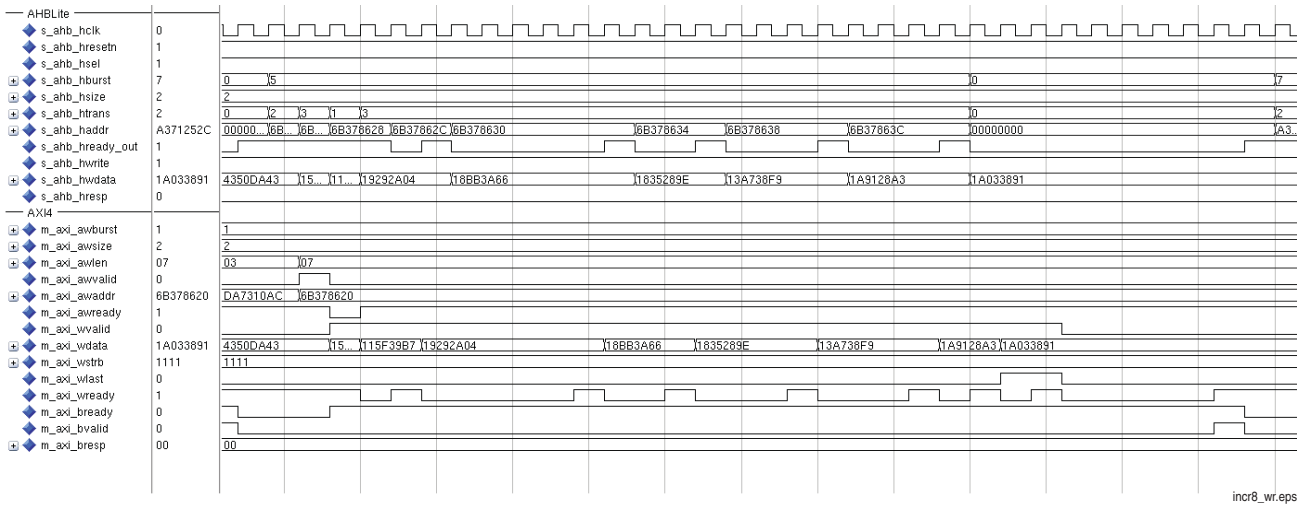

Figure 7: **Write Transfer With Burst Type INCR8**

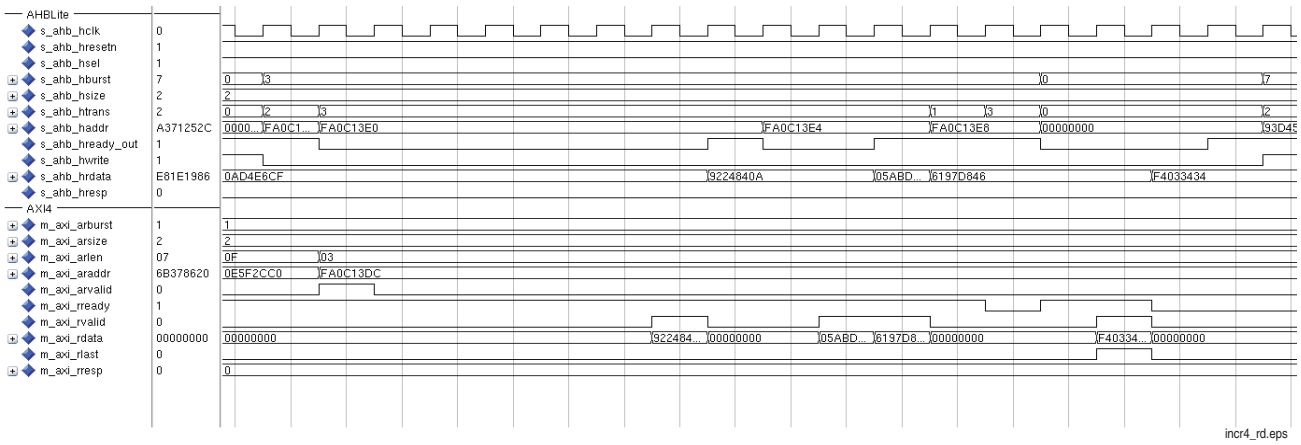

Figure 8: **Read Transfer With Burst Type INCR4**

Write Latency

The core is configured for best possible configuration for calculation of write latency. The write latency from write address valid (S_AHB_HTRANS= NONSEQ) to the write response (S_AHB_HREADY) of AHB Lite to AXI Bridge is 5 clock cycles.

Read Latency

The core is configured for best possible configuration for calculation of read latency. The read latency from read address valid (S_AHB_HTRANS= NONSEQ) to the data beat (S_AHB_HREADY) of AHB Lite to AXI Bridge is 4 clock cycles.

Design Implementation

Target Technology

The target FPGA technologies for the core are the supported device families listed in the LogiCORE IP Facts Table.

Device Utilization and Performance Benchmarks

Core Performance

Because the AHB Lite to AXI Bridge is a module that is used with other design pieces in the FPGA, the resource utilization and timing numbers reported in this section are estimates only. When the AHB Lite to AXI Bridge is combined with other pieces of the FPGA design, the utilization of FPGA resources and timing of the design can be expected to vary from the results reported here.

The AHB Lite to AXI Bridge resource utilization benchmarks for several parameter combinations measured with the Spartan®-6 FPGA as the target device are shown in Table 6.

Table 6: **Performance and Resource Utilization Benchmarks on the Spartan-6 FPGA (xc6slx150tfgg900-3)**

Parameter Values				Device Resources			Performance
C_M_AXI_SUPPORTS_NARROW_BURST	C_S_AHB_DATA_WIDTH	C_M_AXI_DATA_WIDTH	C_AHB_AXI_TIMEOUT	Slices	Slice Flip-Flops	LUTs	F_{MAX}
0	32	32	0	78	183	174	173
0	32	32	16	123	304	261	183
0	32	32	32	86	194	199	174
0	32	32	64	87	195	197	193
0	32	32	128	87	197	207	182
0	32	32	256	90	198	192	193
0	64	64	0	103	279	214	177
0	64	64	16	107	290	252	173
0	64	64	32	113	292	240	191
0	64	64	64	107	293	241	177
0	64	64	128	114	292	232	178
0	64	64	256	107	293	241	177
1	32	32	0	77	188	197	191
1	32	32	16	90	199	203	182
1	32	32	32	97	200	208	178
1	32	32	64	96	201	203	174
1	32	32	128	94	202	215	176
1	32	32	256	100	203	200	177
1	64	64	0	113	288	248	178
1	64	64	16	139	299	259	173
1	64	64	32	123	301	252	176
1	64	64	64	119	302	257	177
1	64	64	128	123	304	261	183
1	64	64	256	123	305	258	175

The AHB Lite to AXI Bridge resource utilization benchmarks for several parameter combinations measured with the Virtex®-6 FPGA as the target device are shown in Table 7.

Table 7: **Performance and Resource Utilization Benchmarks on the Virtex-6 FPGA (xc6vlx195tff1156-3)**

Parameter Values				Device Resources			Performance
C_M_AXI_SUPPORTS_NARROW_BURST	C_S_AHB_DATA_WIDTH	C_M_AXI_DATA_WIDTH	C_AHB_AXI_TIMEOUT	Slices	Slice Flip-Flops	LUTs	F_{MAX}
0	32	32	0	77	180	150	300
0	32	32	16	79	188	164	263
0	32	32	32	81	189	164	274
0	32	32	64	79	190	165	249
0	32	32	128	104	276	182	235
0	32	32	256	101	285	193	236
0	64	64	0	103	286	194	253
0	64	64	16	106	287	195	215
0	64	64	32	103	286	194	253
0	64	64	64	106	287	195	215
0	64	64	128	108	288	197	255
0	64	64	256	106	289	201	251
1	32	32	0	77	185	162	218
1	32	32	16	83	193	175	280
1	32	32	32	78	194	175	236
1	32	32	64	85	195	177	259
1	32	32	128	80	196	178	247
1	32	32	256	106	285	205	225
1	64	64	0	106	294	216	225
1	64	64	16	108	295	217	213
1	64	64	32	107	296	218	251
1	64	64	64	105	297	219	219
1	64	64	128	105	297	219	219
1	64	64	256	108	298	220	246

The AHB Lite to AXI Bridge resource utilization benchmarks for several parameter combinations measured with the Virtex-7 FPGA as the target device are shown in Table 8.

Table 8: **Performance and Resource Utilization Benchmarks on the Virtex-7 FPGA (xc7v285tffg1157-3)**

Parameter Values				Device Resources			Performance
C_M_AXI_SUPPORTS_NARROW_BURST	C_S_AHB_DATA_WIDTH	C_M_AXI_DATA_WIDTH	C_AHB_AXI_TIMEOUT	Slices	Slice Flip-Flops	LUTs	F_{MAX}
0	32	32	0	77	182	147	262
0	32	32	16	78	188	158	232
0	32	32	32	75	189	159	286
0	32	32	64	77	190	160	286
0	32	32	128	102	286	224	261
0	32	32	256	78	192	162	286
0	64	64	0	109	294	225	230
0	64	64	16	109	295	226	231
0	64	64	32	100	285	210	296
0	64	64	64	78	188	158	232
0	64	64	128	75	189	159	286
0	64	64	256	77	190	160	286
1	32	32	0	75	187	158	226
1	32	32	16	74	193	177	239
1	32	32	32	81	194	170	267
1	32	32	64	78	195	179	233
1	32	32	128	79	196	180	223
1	32	32	256	77	197	181	236
1	64	64	0	102	286	224	261
1	64	64	16	109	293	232	230
1	64	64	32	109	294	225	230
1	64	64	64	109	295	226	231
1	64	64	128	111	296	227	231
1	64	64	256	110	297	228	265

The AHB Lite to AXI Bridge resource utilization benchmarks for several parameter combinations measured with the Kintex™-7 FPGA as the target device are shown in Table 9.

Table 9: **Performance and Resource Utilization Benchmarks on the Kintex-7 FPGA (xc7k410tffg900-3)**

Parameter Values				Device Resources			Performance
C_M_AXI_SUPPORTS_NARROW_BURST	C_S_AHB_DATA_WIDTH	C_M_AXI_DATA_WIDTH	C_AHB_AXI_TIMEOUT	Slices	Slice Flip-Flops	LUTs	F_{MAX}
0	32	32	0	75	182	167	279
0	32	32	16	83	188	166	255
0	32	32	32	77	189	171	222
0	32	32	64	80	190	171	219
0	32	32	128	82	191	173	222
0	32	32	256	83	192	166	216
0	64	64	0	100	277	210	221
0	64	64	16	103	284	209	267
0	64	64	32	108	285	202	227
0	64	64	64	101	286	215	226
0	64	64	128	90	287	236	215
0	64	64	256	100	288	229	222
1	32	32	0	122	294	245	213
1	32	32	16	124	295	214	239
1	32	32	32	117	296	231	221
1	32	32	64	83	188	166	255
1	32	32	128	77	189	171	222
1	32	32	256	80	190	171	219
1	64	64	0	105	286	224	265
1	64	64	16	83	192	166	216
1	64	64	32	122	294	245	213
1	64	64	64	124	295	214	239
1	64	64	128	108	285	202	227
1	64	64	256	129	297	216	214

System Performance

To measure the system performance (F_{MAX}) of this core, the core was added to a Virtex-6 FPGA system and a Spartan-6 FPGA system as the device under test (DUT) along with AXI AHB Bridge as illustrated in Figure 9.

Because the AHB Lite to AXI Bridge core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When this core is combined with other designs in the system, the design's FPGA resources and timing usage can be expected to vary from the results reported here.

The target FPGA was filled with logic to drive the LUT and block RAM utilization to approximately 60% and the I/O utilization to approximately 80%. Using the default tool options and the slowest speed grade for the target FPGA, the resulting target F_{MAX} numbers are shown in Table 10.

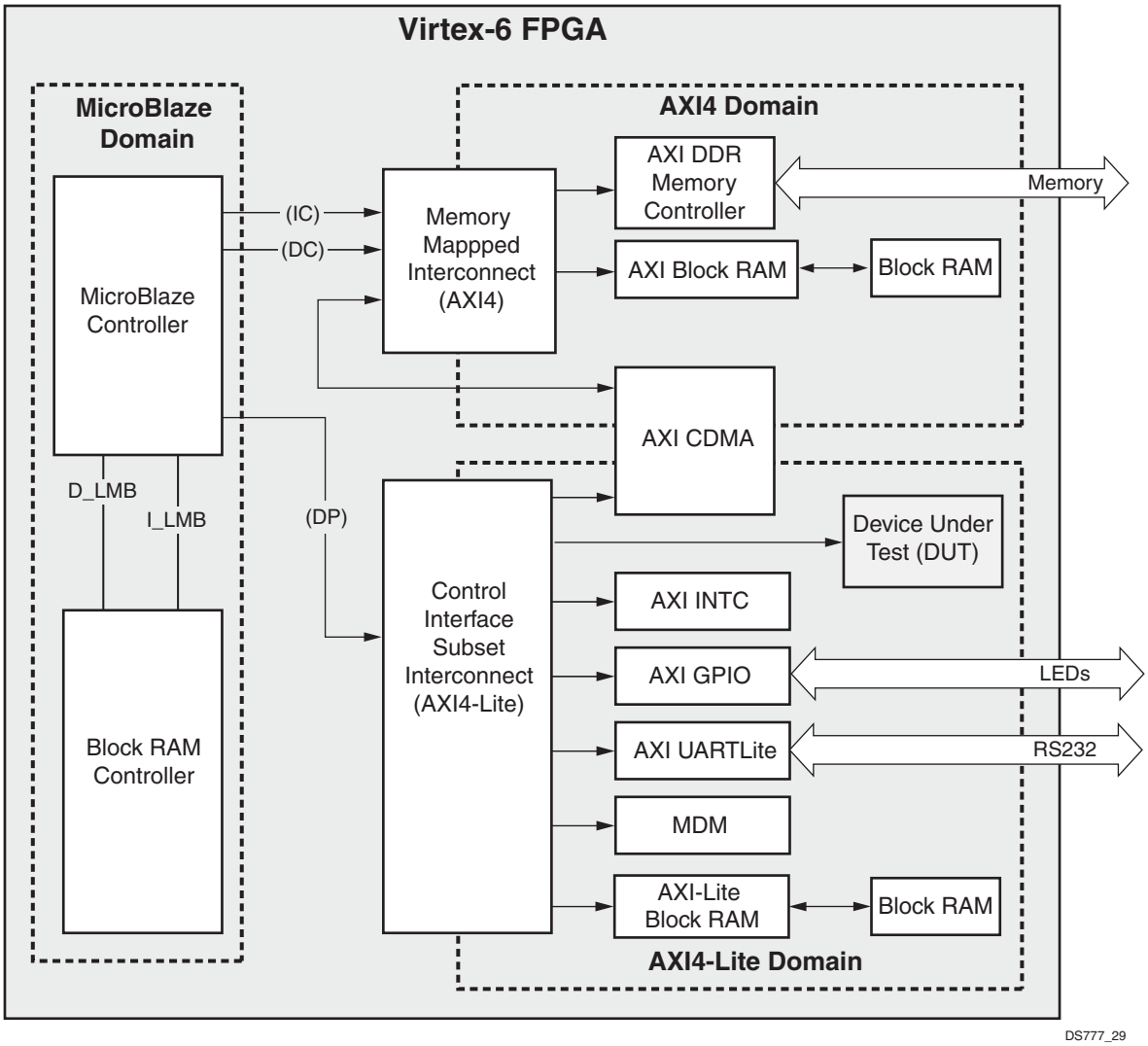

Figure 9: **Virtex-6 FPGA System with the AHB-Lite to AXI Bridge as the DUT**

The target FPGA was filled with logic to drive the LUT and block RAM utilization to approximately 70% and the I/O utilization to approximately 80%. Using the default tool options and the slowest speed grade for the target FPGA, the resulting target F_{MAX} numbers are shown in Table 10.

Table 10: **System Performance**

Target FPGA	Target F_{MAX} (MHz)		
	AXI4	AXI4-Lite	MicroBlaze™
xc6slx45t (1)	90 MHz	120 MHz	80
xc6vlx240t (2)	135 MHz	180 MHz	135

Notes:

1. Spartan-6 LUT utilization: 60%; block RAM utilization: 70%; I/O utilization: 80%; MicroBlaze not AXI4 interconnect; AXI4 interconnect configured with a single clock of 120MHz.
2. Virtex-6 LUT utilization: 70%; block RAM utilization: 70%; I/O utilization: 80%.

The target F_{MAX} is influenced by the exact system and is provided for guidance. It is not a guaranteed value across all systems.

Reference Documents

1. AMBA AXI and ACE Protocol Specification (ARM®)
2. 7 Series FPGAs Overview (DS180)
3. Virtex-6 Family Overview (DS150)
4. Spartan-6 Family Overview (DS160)
5. AXI Interconnect IP Data Sheet (DS768)

Support

Xilinx provides technical support for this LogiCORE™ IP when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

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Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
6/22/11	1.0	Initial Xilinx release.
1/18/12	1.1	C_AHB_AXI_DATA_WIDTH replaced by C_S_AHB_DATA_WIDTH; in Table 6 to Table 9 C_S_AHB_DATA_WIDTH replaced by C_M_AXI_DATA_WIDTH.
7/25/12	1.2	Updated for 14.2/2012.2. Corrections in System Performances section. Added Vivado support. Added Zynq.
10/16/12	1.3	Updated Vivado Design Suite to 2012.3, and Xilinx Platform Studio and ISE Design Suite to 14.3. Removed references to M_AXI_WID signal, which is not available in AXI4, in Table 1 and Table 3. Minor editorial updates.

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