LogiCORE IP AXI Timebase Watchdog Timer (axi_timebase_wdt) (v1.01.a)

DS763 July 25, 2012 **Product Specification**

Introduction

The Advanced eXtensible Lite (AXI) Timebase Watchdog Timer is a 32-bit peripheral that provides a 32-bit free-running timebase and watchdog timer.

Features

- Connects as a 32-bit slave on a AXI4-Lite Interface
- Watchdog timer (WDT) with selectable timeout period and interrupt
- Configurable WDT enable: enable-once or enable-disable
- One 32-bit free-running timebase counter with rollover interrupt-dual control register

LogiCORE IP Facts						
Core Specifics						
Supported Device Family (1)	Zynq™-7000(2), Artix™-7, Virtex®-7, Kintex™-7, Virtex-6, Spartan®-6					
Supported User Interfaces	AXI4-Lite Interface					
	Resources				Frequency	
	Slices	LUTs	FFs	Block RAMs	Max Freq	
	See Table 11 and Table 12			0	See Table 11 and Table 12	
Provided with Core						
Documentation	Product Specification					
Design Files	ISE: VHDL Vivado: Encrypted RTL					
Example Design	Not Provided					
Test Bench	Not Provided					
Constraints File	Not Provided					
Simulation Model	Not Provided					
Tested Design Tools(3)						
Design Entry Tools	Vivado™ Design Suite v2012.2(4) ISE™ Design Suite 14.2					
Simulation	Mentor Graphics ModelSim					
Synthesis Tools	Xilinx Synthesis Technology (XST) Vivado High-Level Synthesis (HLS)					
Support						
Provided by Xilinx, Inc.						

1. For a complete list of supported derivative devices, please see the IDS Embedded Edition Derivative Device Support.
2. Supported in ISE Design Suite implementations only.
3. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.
4. Supports only 7 series devices.

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Functional Description

The top level block diagram for the AXI Timebase Watchdog Timer is shown in Figure 1.

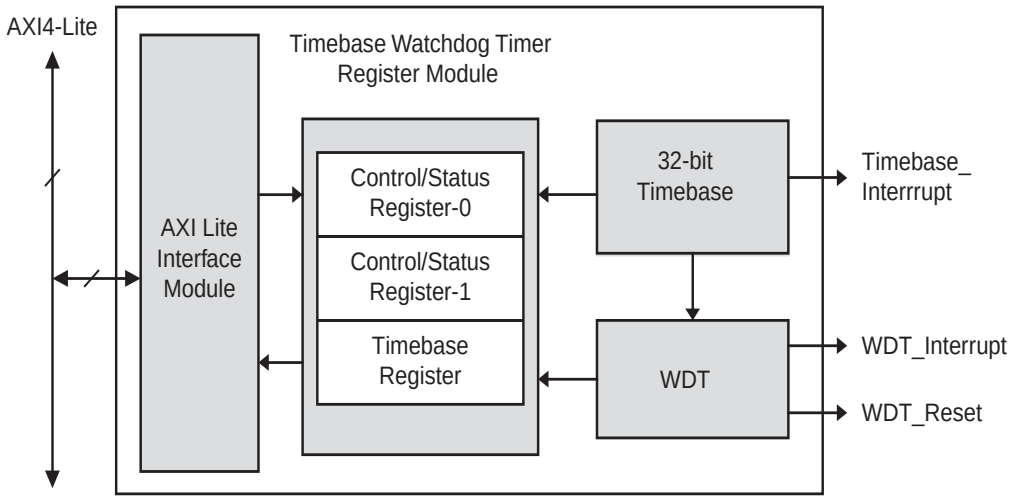

Figure 1: **Block Diagram of AXI Timebase Watchdog Timer**

The AXI Timebase Watchdog Timer modules are described in the following sections.

AXI Lite Interface Module: The AXI Lite Interface Module provides an AXI4-Lite interface. Read and write transactions from AXI are translated into equivalent IP Interconnect (IPIC) transactions. The register interfaces of the AXI Timebase Watchdog Timer connect to the IPIC. The AXI Lite Interface Module also provides an address decoding service. For additional details about the AXI4-Lite slave interface, see the Specification Usage section of the AXI Lite IPIF data sheet.

Timebase Watchdog Timer Register Module: The Timebase Watchdog Timer Register Module includes all memory-mapped registers (as shown in Figure 1). It interfaces to the IPIC. It consists of an 32-bit control/status register-0, an 32-bit control/status register-1 and an 32-bit timebase register (TBR).

32-bit Timebase: The 32-bit timebase consists of a free-running 32-bit timebase counter.

WDT: The Watchdog Timer (WDT) provides the timeout functionality.

AXI Timebase Watchdog Timer Characteristics

The AXI Timebase Watchdog Timer has the following characteristics:

- Consists of a free-running 32-bit timebase counter that is used for both the general purpose timing and the WDT facility
- The timebase counter always counts up from system reset and is read-only.
- The WDT timeout interval is set by the generic C_WDT_INTERVAL, which determines the bit in the timebase to be used as input to the WDT state machine.
- The WDT uses a dual-expiration architecture. After one expiration of the timeout interval, an interrupt is generated and the WDT state bit is set to '1' in the status register. If the state bit is not cleared (by writing a '1' to the state bit) before the next expiration of the timeout interval, a WDT reset is generated. A WDT reset, sets the WDT reset status bit in the status register so that the application code can determine if the last system reset was a WDT reset.
- The WDT can only be disabled by writing to two distinct addresses, reducing the possibility of inadvertently disabling the WDT in the application code.

Operation Overview

Timebase Operation

The timebase is a 32-bit up counter that is incremented by one on the rising edge of the clock provided to the Timebase Watchdog Timer. The counter is reset to zero when the reset input is high or when the WDT is enabled. The TBR contains the full timebase count value of 32 bits.

The TWCSR0 contains the most-significant 28 bits of the timebase count, as well as the WDT enable and status bits. The timing resolution from the upper 28 bits of the timebase count is T_{clk} x 16 (T_{clk} is the period of the input clock). As a result, a single access can be used to read the state of the watchdog timer, as well as a reduced resolution version of the timebase.

An interrupt signal is provided that pulses high for one clock period as the counter rolls over from `0xFFFFFFFF` to `0x00000000`. This interrupt can be used by the software to keep track of how many timebase rollovers have occurred.

WDT Operation

The WDT timeout interval is configured by a parameter to be $2^{C\_WDT\_INTERVAL}$ clock cycles, where C_WDT_INTERVAL is any integer from 8 to 31. The WDT interval is set at FPGA configuration time and cannot be modified dynamically through a control register. Figure 2 shows the WDT state diagram.

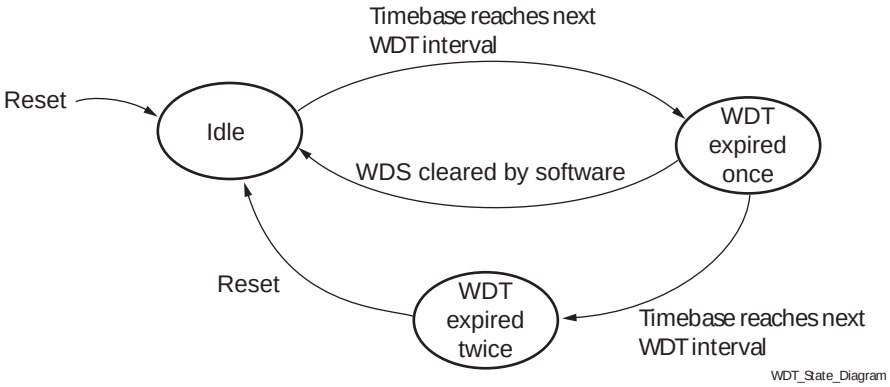

Figure 2: **Timebase Watchdog Timer State Diagram**

Design Parameters

To allow users to create the AXI Timebase Watchdog Timer that is uniquely tailored for their systems, certain features can be parameterized. This allows users to have designs that only utilize the resources required by the system and operate at the best possible performance. The AXI Timebase Watchdog Timer design parameters are shown in Table 1.

In addition to the parameters listed in this table, there are also parameters that are inferred for each AXI interface in the EDK tools. Through the design, these EDK-inferred parameters control the behavior of the AXI Interconnect. For a complete list of the interconnect settings related to the AXI interface, see DS768, *AXI Interconnect IP Data Sheet*.

Table 1: **Design Parameters**

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
System Parameter					
G1	Target FPGA family	C_FAMILY	virtex6, spartan6, virtex7, artix7, kintex7, zynq	virtex6	string
AXI Parameters					
G2	AXI address bus width	C_S_AXI_ADDR_WIDTH	4	4	integer
G3	AXI data bus width	C_S_AXI_DATA_WIDTH	32	32	integer
Timebase Watchdog Timer Parameters					
G4	Indicates the exponent for setting the length of the WDT interval. WDT interval = $2^{C\_WDT\_INTERVAL} \times T_{clk}$	C_WDT_INTERVAL	8 - 31	30	integer
G5	Indicates WDT enable behavior	C_WDT_ENABLE_ONCE	0 = WDT can be repeatedly enabled and disabled via software 1 = WDT can only be enabled once (no disable possible after initial enable)	1	integer

I/O Signals

The AXI Timebase Watchdog Timer I/O signals are listed and described in Table 2.

Table 2: **I/O Signals Description**

Port	Signal Name	Interface	I/O	Initial State	Description
System Signals					
P1	S_AXI_ACLK	System	I	-	AXI Clock
P2	S_AXI_ARESETN	System	I	-	AXI Reset, active LOW

Table 2: **I/O Signals Description *(Cont'd)***

Port	Signal Name	Interface	I/O	Initial State	Description
AXI Write Address Channel Signals					
P3	S_AXI_AWADDR[C_S_AXI_ADDR_WIDTH-1:0]	AXI	I	-	AXI Write address. The write address bus gives the address of the write transaction.
P4	S_AXI_AWVALID	AXI	I	-	Write address valid. This signal indicates that valid write address is available.
P5	S_AXI_AWREADY	AXI	O	0x0	Write address ready. This signal indicates that the slave is ready to accept an address.
AXI Write Channel Signals					
P6	S_AXI_WDATA[C_S_AXI_DATA_WIDTH - 1: 0]	AXI	I	-	Write data
P7	S_AXI_WSTB[C_S_AXI_DATA_WIDTH/8-1:0]	AXI	I	-	Write strobes. This signal indicates which byte lanes to update in memory.
P8	S_AXI_WVALID	AXI	I	-	Write valid. This signal indicates that valid write data and strobes are available.
P9	S_AXI_WREADY	AXI	O	0x0	Write ready. This signal indicates that the slave can accept the write data.
AXI Write Response Channel Signals					
P10	S_AXI_BRESP[1:0]	AXI	O	0x0	Write response. This signal indicates the status of the write transaction. "00" - OKAY (normal response) "10" - SLVERR (error condition)
P11	S_AXI_BVALID	AXI	O	0x0	Write response valid. This signal indicates that a valid write response is available.
P12	S_AXI_BREADY	AXI	I	-	Response ready. This signal indicates that the master can accept the response information.
AXI Read Address Channel Signals					
P13	S_AXI_ARADDR[C_S_AXI_ADDR_WIDTH -1:0]	AXI	I	-	Read address. The read address bus gives the address of a read transaction.
P14	S_AXI_ARVALID	AXI	I	-	Read address valid. This signal indicates, when HIGH, that the read address is valid and will remain stable until the address acknowledgement signal, S_AXI_ARREADY, is high.
P15	S_AXI_ARREADY	AXI	O	0x1	Read address ready. This signal indicates that the slave is ready to accept an address.
AXI Read Data Channel Signals					

Table 2: **I/O Signals Description *(Cont'd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P16	S_AXI_RDATA[C_S_AXI_DATA_WIDTH -1:0]	AXI	O	0x0	Read data
P17	S_AXI_RRESP[1:0]	AXI	O	0x0	Read response. This signal indicates the status of the read transfer. "00" - OKAY (normal response) "10" - SLVERR (error condition)
P18	S_AXI_RVALID	AXI	O	0x0	Read valid. This signal indicates that the required read data is available and the read transfer can complete
P19	S_AXI_RREADY	AXI	I	-	Read ready. This signal indicates that the master can accept the read data and response information
AXI Timebase Watchdog Timer Signals					
P20	WDT_Reset	Timebase Watchdog Timer	O	0	Asserted upon second expiration of the WDT timeout interval. (Active High = '1').
P21	Timebase_Interrupt	Timebase Watchdog Timer	O	0	Asserted as a one clock period wide pulse upon rollover of the timebase from 0xFFFFFFFF to 0x00000000.
P22	WDT_Interrupt	Timebase Watchdog Timer	O	0	Asserted high and stays high until the WDS bit is cleared in the TWCSR0 register.
P23	Freeze	Timebase Watchdog Timer	I	-	When High the watchdog timer counters will be stalled.

Parameter - I/O Signal Dependencies

The dependencies between the AXI Timebase Watchdog Timer core design parameters and I/O signals are described in Table 3. In addition, when certain features are parameterized out of the design, the related logic will no longer be a part of the design. The unused input signals and related output signals are set to a specified value.

Table 3: **Parameter- I/O Signal Dependencies**

Generic or Port	Name	Affects	Depends	Relationship Description
Design Parameters				
G2	C_S_AXI_ADDR_WIDTH	P3, P13	-	Defines the width of the ports
G3	C_S_AXI_DATA_WIDTH	P6, P7, P16	-	Defines the width of the ports
I/O Signals				
P3	S_AXI_AWADDR[C_S_AXI_ADDR_WIDTH-1:0]	-	G2	Port width depends on the generic C_S_AXI_ADDR_WIDTH.
P6	S_AXI_WDATA[C_S_AXI_DATA_WIDTH-1:0]	-	G3	Port width depends on the generic C_S_AXI_DATA_WIDTH.
P7	S_AXI_WSTB[C_S_AXI_DATA_WIDTH/8-1:0]	-	G3	Port width depends on the generic C_S_AXI_DATA_WIDTH.

Table 3: **Parameter- I/O Signal Dependencies *(Cont'd)***

Generic or Port	Name	Affects	Depends	Relationship Description
P13	S_AXI_ARADDR[C_S_AXI_ADDR_WIDTH -1:0]	-	G2	Port width depends on the generic C_S_AXI_ADDR_WIDTH.
P16	S_AXI_RDATA[C_S_AXI_DATA_WIDTH -1:0]	-	G3	Port width depends on the generic C_S_AXI_DATA_WIDTH.

Register Descriptions

Table 4 shows all the AXI Timebase Watchdog Timer registers and their addresses.

Table 4: **Registers**

Register Name	Address (hex)	Access Type	Reset Value (hex)	Description
TWCSR0	0x0	Read/Write	0x00000000	Control/Status register-0
TWCSR1	0x4	Write(1)	0x00000000	Control/Status register-1, state is mirrored in TWCSR0 for read.
TBR	0x8	Read(2)	0x00000000	Timebase register

1. Reading of this register returns undefined valued.
2. Writing into this register has no effect.

Control/Status Register - 0 (TWCSR0)

Control/Status Register-0 contains the watchdog timer reset status, watchdog timer state, and watchdog timer enables. The TWCSR0 bit definitions are shown in Figure 3 and explained in Table 5.

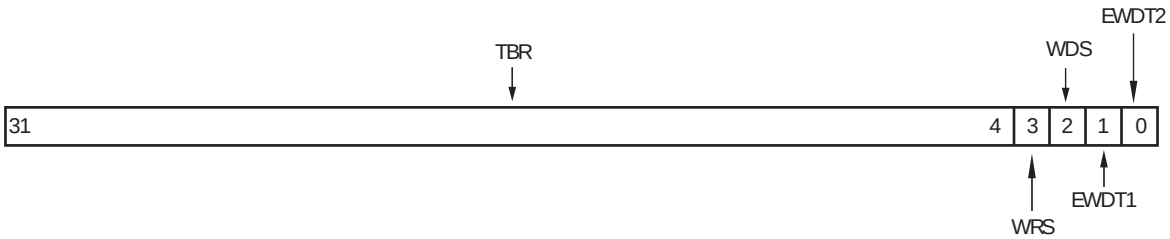

Figure 3: **Control/Status Register - 0 (TWCSR0)**

Table 5: **Control/Status Register - 0 Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31 - 4	TBR	Read	0	Timebase Register (Most significant 28 bits): This read-only field contains the most significant 28 bits of the timebase register. The timebase register is mirrored here so that a single read can be used to obtain the count value and the watchdog timer state if the upper 28 bits of the timebase provide sufficient timing resolution.
3	WRS	Read/Write	'0'	Watchdog Reset Status: Indicates the WDT reset signal was asserted. This bit is not cleared by a system reset so that it can be read after a system reset to determine if the reset was caused by a watchdog timeout. Writing a '1' to this bit clears the watchdog reset status bit. Writing a '0' to this bit has no effect. '0' = WDT reset has not occurred '1' = WDT reset has occurred
2	WDS	Read/Write	'0'	Watchdog Timer State: Indicates the WDT period has expired. The WDT_Reset signal will be asserted if the WDT period expires again before this bit is cleared by software. Writing a '1' to this bit clears the watchdog timer state. Writing a '0' to this bit has no effect. '0' = WDT period has not expired '1' = WDT period has expired, reset will occur on next expiration
1	EWDT1	Read/Write	'0'	Enable Watchdog Timer (Enable 1): This bit must be used in conjunction with the EWDT2 bit in the TWCSR1 register. Both bits must be 0 to disable the WDT. '0' = Disable WDT function if EWDT2 also equals '0' '1' = Enable WDT function
0	EWDT2	Read	'0'	Enable Watchdog Timer (Enable 2): This bit is read only and is the only place to read back a value written to bit 31 of TWCSR1.

Control/Status Register - 1 (TWCSR1)

Control/Status Register-1 contains the second Watchdog Timer (WDT) enable bit. The WDT enable must be cleared in both TWCSR0 and TWCSR1 to disable the WDT. If the WDT is configured as enable-once, then the WDT cannot be disabled after it has been enabled. The TWCSR1 bit definitions are shown in Figure 4 and explained in Table 6.

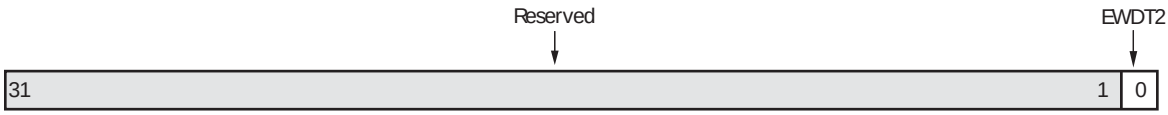

Figure 4: **Control/Status Register - 1 (TWCSR1)**

Table 6: **Control/Status Register - 1 Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31 - 1	Reserved	N/A	N/A	Reserved
0	EWDT2	Write (1)	'0'	Enable Watchdog Timer (Enable 2): This bit must be used in conjunction with the EWDT1 bit in the TWCSR0 register to disable the WDT. Both bits must be 0 to disable the WDT. The value of EWDT2 can be read back only in TWCSR1. '0' = Disable WDT function if EWDT1 also equals '0' '1' = Enable WDT function

1. Reading of this register returns undefined value.

Timebase Register (TBR)

The TBR bit definitions are shown in Figure 5 and explained in Table 7.

The Timebase Register is the output of a free-running incrementing counter that clocks at the input clock rate (no prescaling of the clock is done for this counter). This register is read-only and is reset by the following:

- A system reset
- Enabling the WDT after power on reset
- Enabling the WDT after the WDT has been disabled. (EWDT1 and EWDT2 must both be '0' to disable the WDT.) The WDT is enabled when either EWDT1 or EWDT2 are set to '1'. Note that when the WDT mode is enable-once, the TBR can only be reset when the WDT is first enabled.

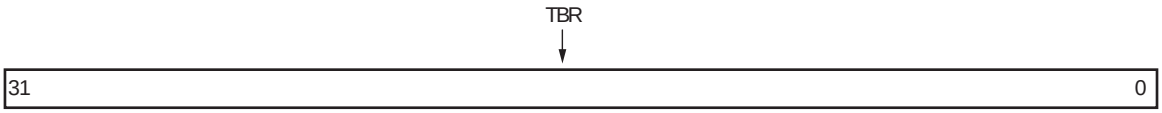

Figure 5: **Timebase Register (TBR)**

Table 7: **Timebase Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
31 - 0	TBR	Read (1)	0	Timebase register: This register indicates the free-running incrementing counter value.

1. Writing into this register has no effect.

Timing Diagrams

Figure 6 shows the WDT Expired Once operation waveform and Figure 7 shows the WDT Expired Twice operation waveform. The state of the WDT is given by the WDS bit in the TWCSR0 register. If the WDT interval expires while the WDS bit is '1', the WDT reset signal is asserted. An interrupt is provided when the WDS bit is set so that the software can clear the bit before the second expiration of the WDT. The WDS bit is cleared by writing a '1' to it. Writing a '0' to the WDS bit has no effect. Figure 6 shows the operation performed where WDS bit is cleared by the software before the second expiration occurs. Figure 7 shows the operation performed where WDS bit is not cleared

and WDT expired twice state is reached.

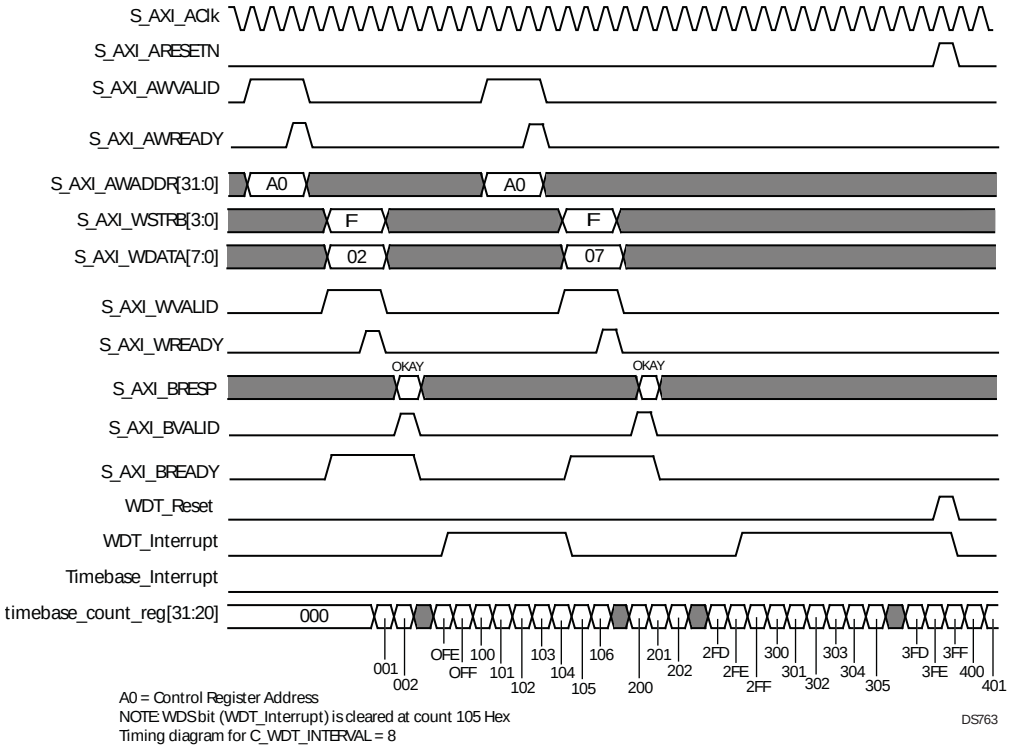

Figure 6: **WDT Expired Once Operation Waveform**

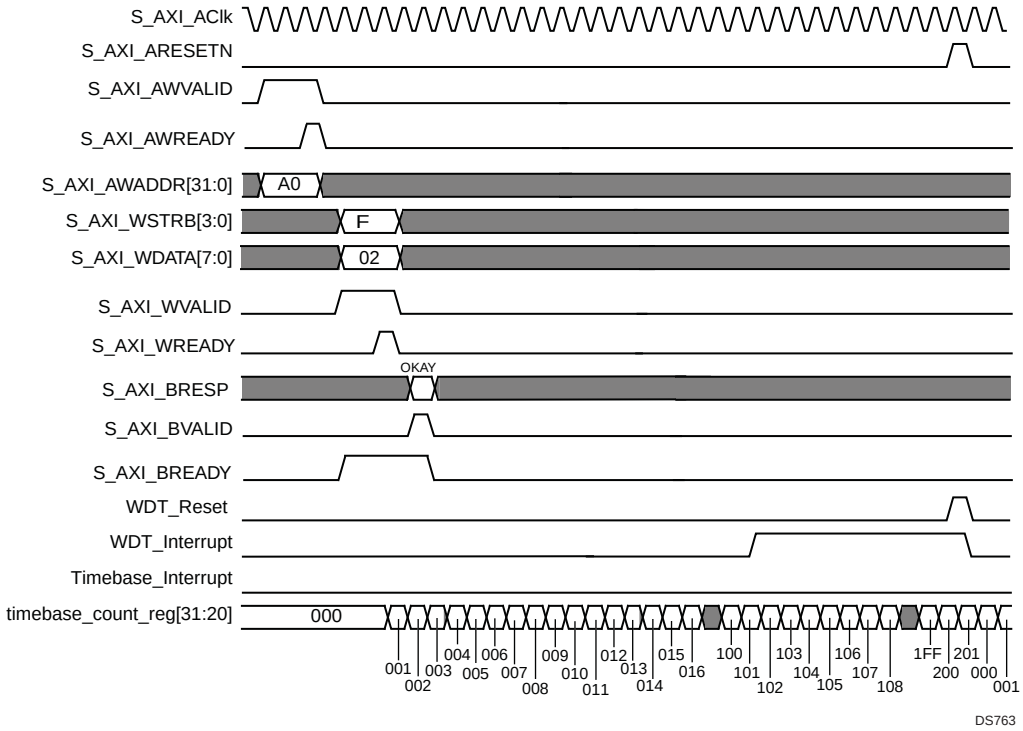

Figure 7: **WDT Expired Twice Operation Waveform**

Design Implementation

Target Technology

The intended target technologies are Artix™-7, Virtex®-7, Kintex™-7, Virtex-6 and Spartan®-6 FPGAs.

Device Utilization and Performance Benchmarks

Core Performance

Since the AXI Timebase Watchdog Timer core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When the AXI Timebase Watchdog Timer core is combined with other designs in the system, the utilization of FPGA resources and timing of the AXI Timebase Watchdog Timer design will vary from the results reported here.

The AXI Timebase Watchdog Timer resource utilization for various parameter combinations measured with a Artix-7 FPGA as the target device are detailed in Table 11.

Note: Resources numbers for Zynq-7000 devices are expected to be similar to 7 series device numbers.

Table 8: **Performance and Resource Utilization for Artix-7 (XC7A355TDIE) and Zynq-7000 Devices**

Parameter Values		Device Resources			Performance
C_WDT_INTERVAL	WDT_ENABLE_ONCE	Slice Flip-Flops	Slices	LUTs	$f_{MAX\ (MHz)}$
8	0	57	67	135	220.946
30	1	57	55	135	245.640
31	1	57	68	135	233.209

The AXI Timebase Watchdog Timer resource utilization for various parameter combinations measured with a Virtex-7 FPGA as the target device are detailed in Table 11.

Note: Resources numbers for Zynq-7000 devices are expected to be similar to 7 series device numbers.

Table 9: **Performance and Resource Utilization for Virtex-7 (XC7V855T-FFG1157-3) and Zynq-7000 Devices**

Parameter Values		Device Resources			Performance
C_WDT_INTERVAL	WDT_ENABLE_ONCE	Slice Flip-Flops	Slices	LUTs	$f_{MAX\ (MHz)}$
8	0	57	56	135	273.299
30	1	57	72	135	203.500
31	1	57	61	135	307.977

The AXI Timebase Watchdog Timer resource utilization for various parameter combinations measured with a Kintex-7 FPGA as the target device are detailed in Table 11.

Note: Resources numbers for Zynq-7000 devices are expected to be similar to 7 series device numbers.

Table 10: **Performance and Resource Utilization for Kintex-7 (XC7K410T-FFG676-3)and Zynq-7000 Devices**

Parameter Values		Device Resources			Performance
C_WDT_INTERVAL	WDT_ENABLE_ONCE	Slice Flip-Flops	Slices	LUTs	$f_{MAX\ (MHz)}$
8	0	57	46	135	398.724
30	1	57	62	134	295.334
31	1	57	63	136	270.929

The AXI Timebase Watchdog Timer resource utilization for various parameter combinations measured with a Virtex-6 FPGA as the target device are detailed in Table 11.

Table 11: **Performance and Resource Utilization Benchmarks Virtex-6 FPGA (XC6VLX130T-1-FF1156)**

Parameter Values		Device Resources			Performance
C_WDT_INTERVAL	WDT_ENABLE_ONCE	Slice Flip-Flops	Slices	LUTs	$f_{MAX\ (MHz)}$
8	0	97	47	133	220
30	1	97	50	133	224
31	1	97	53	132	214

The AXI Timebase Watchdog Timer resource utilization for various parameter combinations measured with a Spartan-6 FPGA as the target device are detailed in Table 12.

Table 12: **Performance and Resource Utilization Benchmarks Spartan-6 FPGA (XC6SLX45T-2-FGG484)**

Parameter Values		Device Resources			Performance
C_WDT_INTERVAL	WDT_ENABLE_ONCE	Slice Flip-Flops	Slices	LUTs	$f_{MAX\ (MHz)}$
8	0	97	47	133	182
30	1	97	50	133	183
31	1	97	46	133	175

System Performance

To measure the system performance (Fmax) of this core, this core was added to a Virtex-6 FPGA system and a Spartan-6 FPGA system as the Device Under Test (DUT).

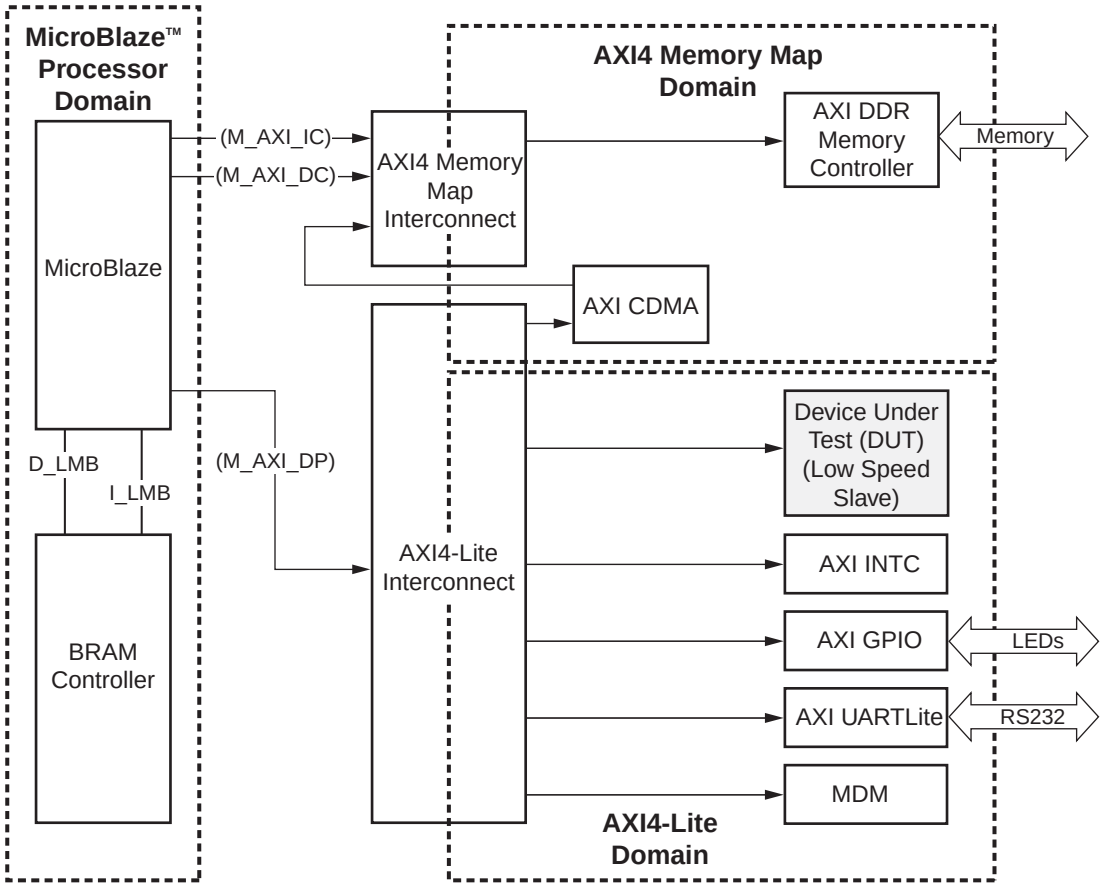

Figure 8: **Virtex-6 and Spartan-6 Devices F_{MAX} Margin System**

Because the AXI Timebase Watchdog Timer core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When this core is combined with other designs in the system, the utilization of FPGA resources and timing of the design will vary from the results reported here.

The target FPGA was then filled with logic to drive the LUT and block RAM utilization to approximately 70% and the I/O utilization to approximately 80%. Using the default tool options and the slowest speed grade for the target FPGA, the resulting target F_{MAX} numbers are shown in Table 13.

Table 13: **AXI Timebase Watchdog Timer System Performance**

Target FPGA	Target F_{MAX} (MHz)
Spartan-6	110
Virtex-6	180

Table 13: **AXI Timebase Watchdog Timer System Performance *(Cont'd)***

Target FPGA	Target F_{MAX} (MHz)
Virtex-7	180
Kintex-7	180
Artix-7	110

Design Constraints

No additional constraints are needed besides a PERIOD constraint on S_AXI_ACLK, which is usually propagated from a global clock input PERIOD.

Support

Xilinx provides technical support for this LogiCORE™ IP system when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx Vivado Design Suite and ISE Design Suite Embedded Edition software under the terms of the Xilinx End User License.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

Reference Documents

- *AXI4 AMBA® AXI Protocol Version: 2.0 Specification*
- DS765 *LogiCORE IP AXI Lite IPIF Data Sheet*
- DS768, *AXI Interconnect IP Data Sheet*

List of Acronyms

Acronym	Spelled Out
AMBA	Advanced Microcontroller Bus Architecture
ARM	Advanced RISC Machine
AXI	Advanced eXtensible Lite Interface
DUT	Device Under Test
EDK	Embedded Development Kit
FF	flip-flop
FPGA	Field Programmable Gate Array
IP	Intellectual Property

Acronym	Spelled Out
IPIC	IP Interconnect
ISE	Integrated Software Environment
LUT	Lookup Table
RAM	Random Access Memory
TBR	Timebase Register
VHDL	VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits)
WDT	Watchdog Timer
XST	Xilinx Synthesis Technology

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/21/10	1.0	First release of the core with AXI interface support. The previous release of this document was DS582.
09/21/10	1.0.1	Documentation only. Added inferred parameters text on page 4.
12/14/10	1.1	Updated for core version v1.01.a; updated to 12.4 tools.
06/22/11	2.0	Updated for Xilinx tools v13.2. Added support for Artix-7, Virtex-7, and Kintex-7 devices.
07/25/12	3.1	Added support for Vivado Design Suite. Added support for Zynq-7000 devices. Removed the AXI Base Address and AXI High Address parameters.

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