BFM Synchronization Bus

DS134 (v2.0) April 30, 2004 **Product Overview**

Introduction

The BFM Synchronization Bus is a simple bus that connects the various Bus Functional Models in a design and allows communication between them.

The BFM Synchronization bus is not a bus Bus Functional Model.

Features

- Configurable bus size
- Collects synchronization output signals from all Bus Functional Models
- Distributes a synchronization input signal to all Bus Functional Models

More Information

For detailed information on the IBM OPB and PLB Bus Functional Model Toolkits, you may register for the **CoreConnect Lounge** on the Xilinx web site to get access to the IBM CoreConnect documentation.

Core Facts

Core Specifics		
Supported Device Family	All	
Version of Core	bfm_synch	v1.00.a
Resources Used		
	Min	Max
I/O	N/A	N/A
LUTs	N/A	N/A
FFs	N/A	N/A
Block RAMs	N/A	N/A
Provided with Core		
Documentation	This document	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	EDK 6.2 or later ISE 6.2 or later	
Verification	N/A	
Simulation	ModelSim SE/EE 5.6e or later	
Synthesis	N/A	
Support		
Support provided by Xilinx, Inc.		

Implementation

The CoreConnect Bus Functional Models have a synchronization interface that allows backdoor communication between them so that events that they generate or respond to can be synchronized. Xilinx has created a simple bus that allows the connection of these signals between BFM components.

Figure 1 shows how the synchronization bus is used for a system that includes three BFM devices.

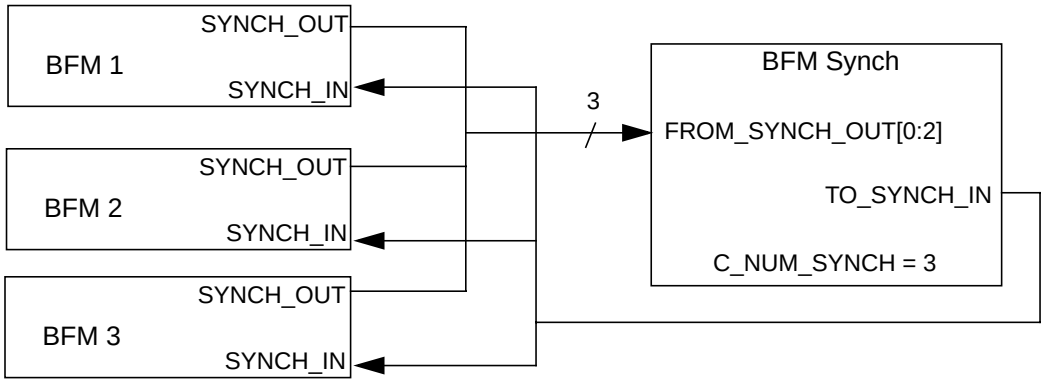

Figure 1: **BFM synchronization bus usage**

MPD Parameters

The associated MPD (Microprocessor Peripheral Definition) file contains a list of the peripheral s parameters that are fixed at FPGA configuration time. The parameters are described in Table 1.

Table 1: **MPD Parameters**

Parameter	Description	Allowable Values	Type
C_NUM_SYNCH	Number of synchronization inputs. This parameter defines the width of the FROM_SYNCH_OUT vector	1-16	integer

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
4/30/04	1.0	Initial Xilinx release