

Introduction

The LogiCORE™ IP Common Packet Radio Interface (CPRI™) core is a high-performance, low-cost flexible solution for implementation of the CPRI interface. This core uses state-of-the-art Zynq™-7000, Virtex-7, Kintex™-7 and Artix-7™ device GTXE2, GTPE2 and GTHE2 transceivers, Virtex-6 FPGA GTXE1 transceivers, Spartan®-6 FPGA GTPA1 transceivers, or Virtex®-5 Field Programmable Gate Array (FPGA) RocketIO™ GTP and GTX transceivers to implement the Physical Layer. A compact and customizable Data Link Layer is implemented in the FPGA logic.

Features

- Designs implemented on Zynq-7000, Virtex-7 and Kintex-7 devices operate at line rates of 614.4 Mb/s, 1228.8 Mb/s, 2457.6 and 3072 Mb/s, using GTXE2 and GTHE2 transceivers. Optionally line rates of 4915.2 Mb/s, 6144 Mb/s and 9830.4 Mb/s are supported in these devices.
- Designs implemented on Artix-7 devices operate at line rates of 614.4 Mb/s, 1228.8 Mb/s, 2457.6 Mb/s and 3072 Mb/s, using GTPE2 transceivers. Optionally line rates of 4915.2 Mb/s and 6144 Mb/s are supported in these devices.
- Designs implemented on Virtex-6 devices operate at line rates of 614.4 Mb/s, 1228.8 Mb/s, 2457.6 and 3072 Mb/s, using GTXE1 transceivers. Optionally line rates of 4915.2 Mb/s and 6144 Mb/s are supported in these devices.
- Designs implemented on Virtex-5 LXT/SXT and Spartan-6 LXT devices operate at line rates of 614.4 Mb/s, 1228.8 Mb/s, 2457.6 and 3072 Mb/s, using GTP and GTPA1 transceivers.
- Designs implemented on Virtex-5 FXT/TXT devices operate at line rates of 1228.8 Mb/s, 2457.6 and 3072 Mb/s, using GTX transceivers.
- Suitable for use in both Radio Equipment Controllers (RECs) and Radio Equipment (RE), including multi-hop system
- UTRA-FDD I/Q module supporting 1 to 48 Antenna-Carriers per core
- Automatic speed negotiation
- Supports both Fast (Ethernet) and Slow High-Level Data Link Control (HDLC) Control and Management (C&M) channels per [CPRI Specification v5.0](#).
- Designed to [CPRI Specification v5.0](#)

LogiCORE IP Facts	
Core Specifics	
Supported Device Family ¹	Zynq-7000 ² , Virtex-7, Kintex-7, Artix-7 ³ , Virtex-6 Spartan-6, Virtex-5 LXT ⁴ /SXT/FXT/TXT
Supported User Interfaces	Generic data, status, configuration and management interfaces. AXI4-Lite management interface
Provided with Core	
Design Files	ISE®: Native Generic Circuit (NGC) Netlist Vivado™: Encrypted RTL
Example Design	VHDL
Test Bench	VHDL
Constraints File	ISE: UCF Vivado: XDC
Simulation Models	VHDL, Verilog
Supported S/W Drivers	N/A
Tested Design Flows⁵	
Design Entry	ISE Design Suite 14.4 Vivado Design Suite 2012.4 ⁶
Simulation ⁷	Mentor Graphics ModelSim
Synthesis	Xilinx Synthesis Technology (XST) Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

1. For the complete list of supported devices, see the [release notes](#) for this core.
2. Supported in ISE Design Suite implementations only. Excludes the Zynq-7000 010 and 020 devices.
3. Excludes the Artix-7 100T device in CSG324 and FTG256 packages.
4. Excludes Virtex-5 LX20T FPGA.
5. For the supported versions of the tool, see the [Xilinx Design Tools: Release Notes Guide](#).
6. Supports only 7 series devices.
7. Requires a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator. For VHDL simulation, a mixed HDL license is required.

Features (Continued)

- Can be configured as master or slave at generation time
- Master core can be switched to operate as a slave through a configuration port
- Easy-to-use interface for in-phase (I) and quadrature-phase (Q) data and synchronization
- Supports vendor-specific data transport
- Delay measurement capability meets CPRI Requirement 21 per [CPRI Specification v5.0](#).

Overview

The CPRI core implements Layer 1 and Layer 2 of the CPRI specification in Zynq-7000, Virtex-7, Kintex-7, Artix-7, Virtex-6, Spartan-6 and Virtex-5 LXT/SXT/FXT devices. The CPRI core provides these client-side interfaces.

- **I/Q Interface.** Consists of a stream of radio data (I/Q samples) that is synchronized to the Universal Mobile Telecommunications System (UMTS) radio frame pulse.
- **Synchronization Interface.** Provides the means for the client logic to synchronize to the network time by transmitting the UMTS radio frame pulse and clock frequency.
- **High-Level Data Link Control (HDLC) Interface.** Transports management information between master and slave. The HDLC interface is serialized and synchronous.
- **Ethernet Interface.** When configured to support speeds of up to 3072 Mb/s, the Ethernet interface is presented as a Media Independent Interface (MII); this allows a 100 Mbit Ethernet Media Access Controller (MAC) to be attached to the core to provide a high-speed channel for management information. When speeds of up to 4915.2 Mb/s, 6144 Mb/s or 9830.4 Mb/s are supported a Gigabit Media Independent Interface (GMII) option is available. This allows a 1 Gbit Ethernet MAC to be attached to the core. The core includes an Ethernet frame buffer in both transmit and receive directions.
- **Vendor-Specific Data Interface.** Provides client logic access to the vendor-specific sub-channels in the CPRI stream.
- **Management Interface.** Provides control and status registers that allow management of the entire design from a supervisory processor.

The architecture of the core is shown in [Figure 1](#). In addition to the interfaces described previously, the core contains these blocks:

- **Status/Alarm Block.** Reflects the internal state of the core and the state of the link.
- **Start-up Sequencer.** Performs line-rate negotiation and Control and Management (C&M) parameter negotiation at link start-up. This block continuously monitors the state of the link and sends the status to the alarm block.
- **UMTS Terrestrial Radio Access - Frequency Division Duplexing (UTRA FDD) I/Q Module:** A pluggable I/Q module to support multiplexing and demultiplexing of I/Q samples in UTRA FDD systems (shown in [Figure 1](#)).
- **Evolved UMTS Terrestrial Radio Access (E-UTRA) I/Q Module:** A pluggable I/Q module to support multiplexing and demultiplexing of I/Q samples in E-UTRA systems (not shown in [Figure 1](#)).
- **Legacy raw I/Q Module:** A pluggable I/Q Module for backward compatibility with the raw interfacing timing for v1.x CPRI cores (not shown in [Figure 1](#)).

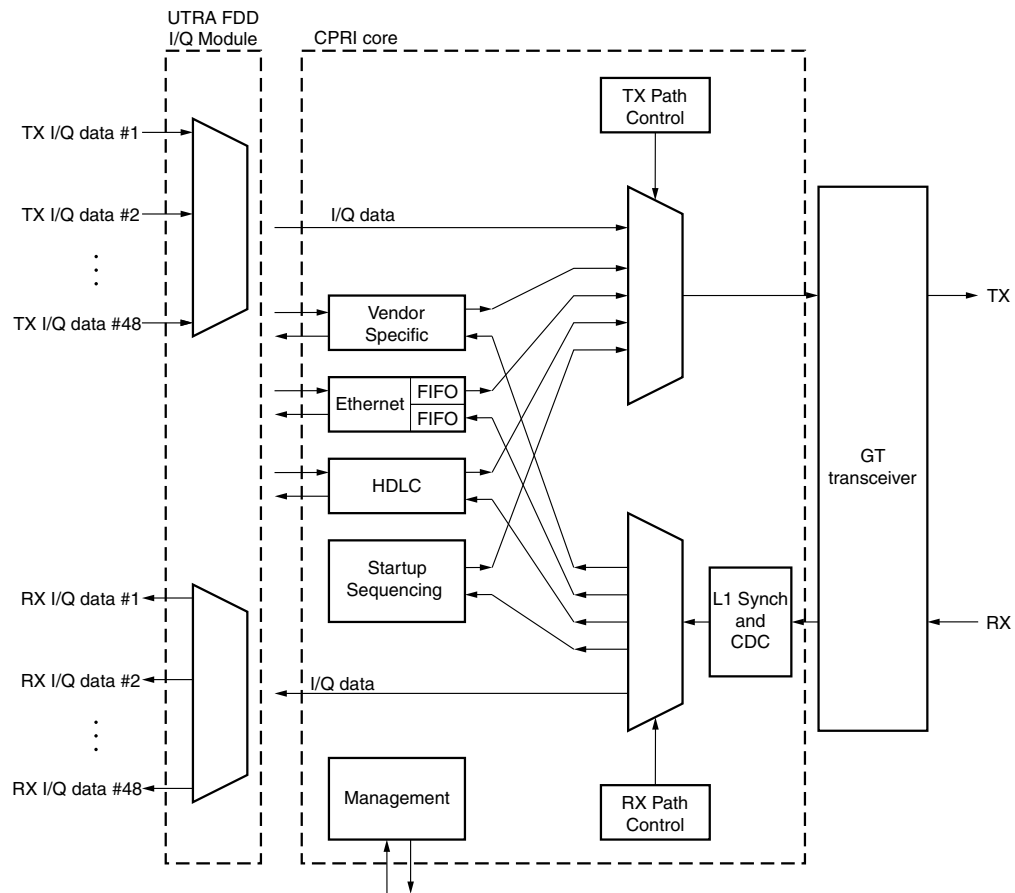


Figure 1: CPRI Top-Level Block Diagram

References

To search for Xilinx documentation, go to www.xilinx.com/support.

- [CPRI Specification v5.0](#), September 21, 2011
- [IEEE Standard 802.3-2005](http://standards.ieee.org/getieee802) (standards.ieee.org/getieee802)
- [Xilinx AXI Reference Guide \(UG761\)](#)

Support

Xilinx provides [technical support](#) for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices not listed in the documentation, or if customized beyond that allowed in the product documentation, or if any changes are made to the sections marked DO NOT MODIFY.

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Related Information

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Revision History

Date	Version	Revision
07/25/12	1.0	Initial Xilinx release. Replaces ds611. Data sheet information was incorporated into the new product guide, pg056.
12/18/12	2.0	Updated for ISE Design Suite 14.4, Vivado Design Suite 2012.4, and core version 6.1.

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