LogiCORE IP CPRI v3.2

DS611 July 23, 2010 **Product Specification**

Introduction

The LogiCORE™ IP CPRI™ core is a high-performance, low-cost flexible solution that implements the Common Packet Radio Interface (CPRI). This core uses state-of-the-art Virtex®-5 FPGA RocketIO™ GTP and GTX transceivers, Virtex-6 FPGA GTXE1 transceivers or Spartan®-6 GTPA1 transceivers to implement the Physical Layer, and a compact and customizable Data Link Layer is implemented in the FPGA fabric.

Features

- Designs implemented on Virtex-5 LXT/SXT and Spartan-6 LXT devices operate at line rates of 614.4 Mbps, 1228.8 Mbps, 2457.6 and 3072 Mbps, using GTP and GTPA1 transceivers.
- Designs implemented on Virtex-5 FXT/TXT devices operate at line rates of 1228.8 Mbps, 2457.6 and 3072 Mbps, using GTX transceivers.
- Designs implemented on Virtex-6 devices operate at line rates of 614.4 Mbps, 1228.8 Mbps, 2457.6 and 3072 Mbps, using GTXE1 transceivers. Optionally line rates of 4915.2 Mbps and 6144 Mbps are supported in these devices.
- Suitable for use in both Radio Equipment Controllers (RECs) and Radio Equipment (RE), including multi-hop systems
- Supports 1 to 24 Antenna-Carriers per core
- Automatic speed negotiation
- Can be configured as master or slave at generation time
- Easy-to-use interface for I/Q data and synchronization
- Supports vendor-specific data transport
- Delay measurement capability meets CPRI Requirement 21
- Supports both Fast (Ethernet) and Slow (HDLC) Control and Management (C&M) Channels
- Designed to *CPRI Specification v4.1*

LogiCORE IP Facts				
Core Specifics				
Supported Device Family[1]	Virtex-6[2] Spartan-6 Virtex-5 LXT[3]/SXT/FXT/TXT			
Resources Used (3072.0 Mbps default configuration)	**Slices**	**LUTs**	**FFs**	**Block RAMs**
	1115	1577	1937	6
Resources Used (6144.0 Mbps default configuration)	**Slices**	**LUTs**	**FFs**	**Block RAMs**
	1371	2269	2689	6
Provided with Core				
Documentation	Product Specification User Guide Getting Started Guide			
Design File Formats	NGC Netlist			
Constraints File	.ucf (user constraints file)			
Verification	VHDL Test Bench			
Example Design	VHDL			
Design Tool Requirements				
Xilinx® Implementation Tools	Xilinx ISE® v12.2 software			
Simulation[4]	Mentor Graphics ModelSim 6.5c and above			
Synthesis	XST			
Support				
Provided by Xilinx, Inc. @ www.xilinx.com				

1. For the complete list of supported devices, see the release notes for this core.
2. 6144 Mbps is only supported on -2 and -3 speed grades for Virtex-6 devices.
3. Excludes Virtex-5 LX20T.
4. Requires a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator. For VHDL simulation, a mixed HDL license is required.

Overview

The CPRI core implements Layer 1 and Layer 2 of the CPRI specification in Xilinx Virtex-6, Spartan-6 and Virtex-5 LXT/SXT/FXT devices. The CPRI core provides the following client-side interfaces.

- **I/Q Interface.** Consists of a stream of radio data (I/Q samples) that is synchronized to the Universal Mobile Telecommunications System (UMTS) radio frame pulse.
- **Synchronization Interface.** Provides the means for the client logic to synchronize to the network time by transmitting the UMTS radio frame pulse and clock frequency.
- **High-Level Data Link Control (HDLC) Interface.** Transports management information between master and slave. The HDLC interface is serialized and synchronous.
- **Ethernet Interface.** When configured to support speeds of up to 3072 Mbps, the Ethernet interface is presented as a Media Independent Interface (MII), this allows a 100 Mbit Ethernet Media Access Controller (MAC) to be attached to the core to provide a high-speed channel for management information. When speeds of up to 6144 Mbps are supported a Gigabit Media Independent Interface (GMII) option is available, this allows a 1 Gbit Ethernet MAC to be attached to the core. The core includes an Ethernet frame buffer in both transmit and receive directions.
- **Vendor-Specific Data Interface.** Provides client logic access to the vendor-specific sub-channels in the CPRI stream.
- **Management Interface.** Provides control and status registers that allow management of the entire design from a supervisory processor.

The architecture of the core is shown in Figure 1. In addition to the interfaces described previously, the core contains the following blocks:

- **Status/Alarm Block.** Reflects the internal state of the core and the state of the link.
- **Startup Sequencer.** Performs line-rate negotiation and Control and Management (C&M) parameter negotiation at link startup. This block continuously monitors the state of the link and sends the status to the alarm block.
- **UMTS Terrestrial Radio Access - Frequency Division Duplexing (UTRA FDD) I/Q Module:** A pluggable I/Q module to support multiplexing and demultiplexing of I/Q samples in UTRA FDD systems (shown in Figure 1).
- **Legacy raw I/Q Module**: A pluggable I/Q Module for backward compatibility with the raw interfacing timing for v1.x CPRI cores (not shown in Figure 1).

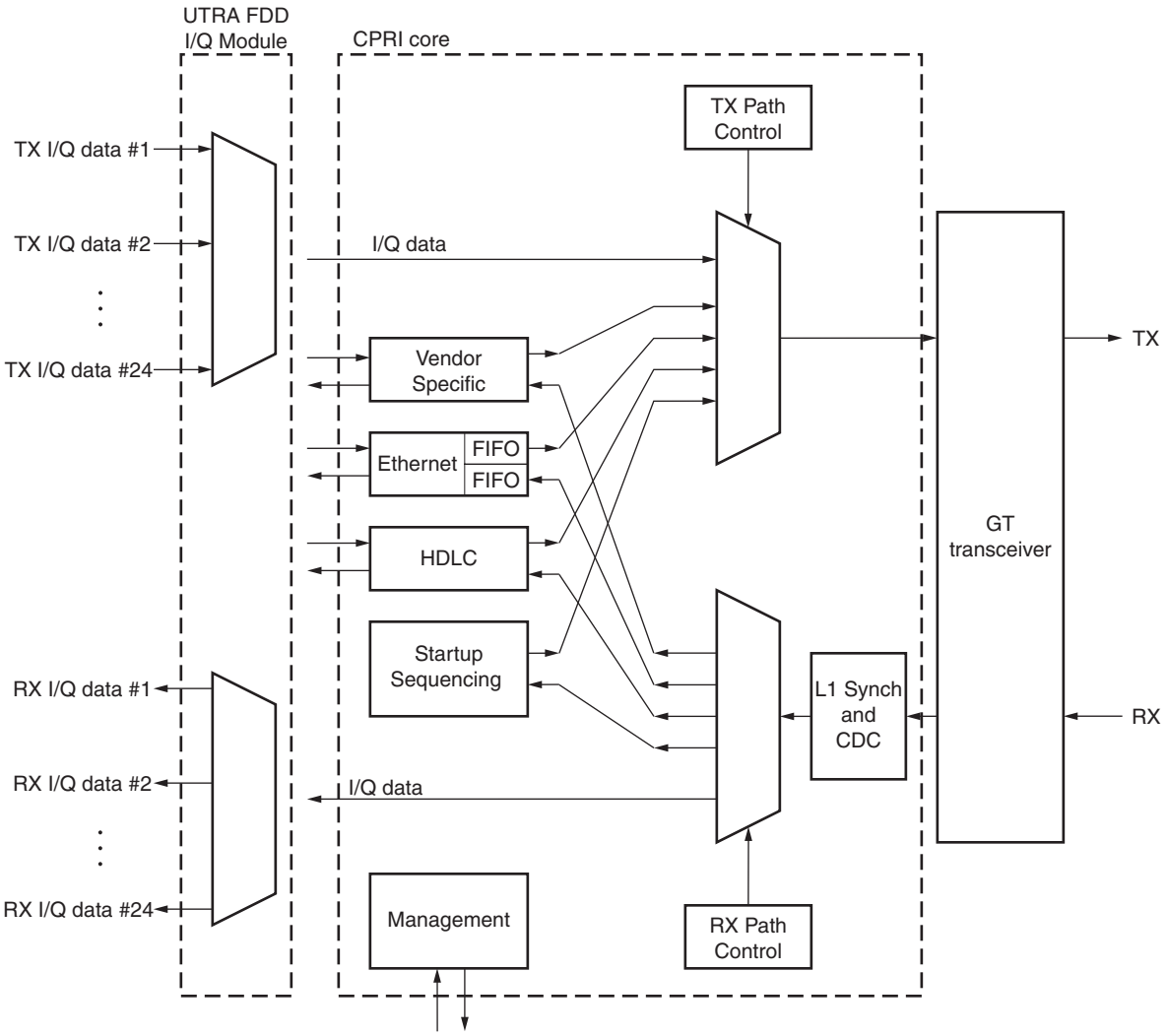

Figure 1: **CPRI Top-Level Block Diagram**

Applications

CPRI is an emerging standard for communication between a Radio Equipment Controller (REC) or Base Station and one or more Radio Equipment (RE) units in a 3G cellular network. The concept is to foster an independent technology evolution for cellular equipment products by defining a publicly available specification for the key internal interface between these units. Figure 2 shows the position of the interface in a cellular system.

The goal of the CPRI interface is to use one physical connection for the radio data (I/Q data), radio unit management (Automatic Gain Control, alarms, etc.) and synchronization (clock frequency control, frame synchronization). Table 1 shows the data rates supported by each Xilinx device. Data is transferred over a single serial link. This link is defined to be electrically compliant with existing high speed serial link standards such as the Gigabit Ethernet and 10 Gigabit Attachment Unit Interface (XAUI) standards.

Table 1: **Supported Data Rates**

	614 Mbps	1228.8 Mbps	2457.6 Mbps	3072.0 Mbps	4915.2 Mbps	6144.0 Mbps
Virtex-5						
LXT/SXT	Supported	Supported	Supported	Supported	Not supported	Not supported
FXT/TXT	Not supported	Supported	Supported	Supported	Not supported	Not supported
Virtex-6						
LXT/SXT (-1/-1L speed grade)	Supported	Supported	Supported	Supported [1]	Supported [1]	Not supported
LXT/SXT (-2/-3 speed grade)	Supported	Supported	Supported	Supported	Supported	Supported
CXT	Not supported	Supported	Supported	Supported	Not supported	Not supported
Spartan-6	Supported	Supported	Supported	Supported	Not supported	Not supported

1. Support for 3072.0 Mbps and 4915.2 Mbps are mutually exclusive in Virtex-6 LXT/SXT devices with speed grade -1/-1L

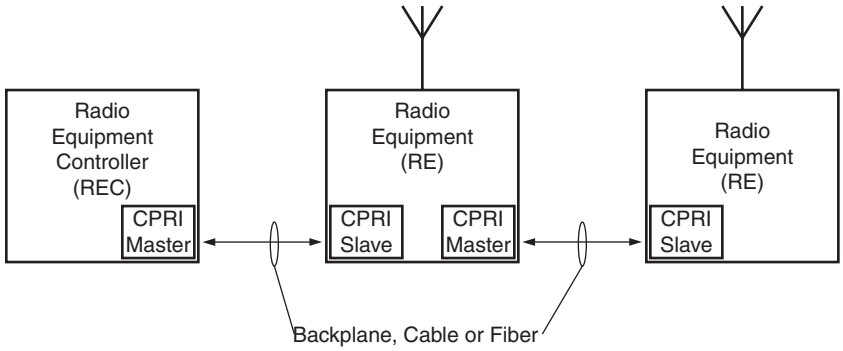

Figure 2: **Location of CPRI in a Cellular System**

Device Utilization

Virtex-5 Devices

Table 2 provides approximate device utilization figures for example configurations of the core in Virtex-5 devices. The values include the GTP/GTX control logic and the clock control logic.

Table 2: **Virtex-5 Core Device Utilization[1]**

Parameter Values				Device Resources					
Device	Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	PLLs	BUFRs	BUFGs
LXT/SXT	Yes	No	Slave	1428	1761	5	1	1	3
LXT/SXT	Yes	Yes	Slave	1552	1928	5	1	1	3
LXT/SXT	No	No	Slave	1172	1183	1	1	1	3
LXT/SXT	No	Yes	Slave	1123	1350	1	1	1	3
LXT/SXT	No	No	Master	998	1181	2	1	1	3
LXT/SXT	No	Yes	Master	1149	1359	2	1	1	3
LXT/SXT	Yes	No	Master	1427	1759	6	1	1	3
LXT/SXT	Yes	Yes	Master	1577	1937	6	1	1	3
FXT	No	No	Slave	1003	1154	1	1	1	2
FXT	No	Yes	Slave	1122	1321	1	1	1	2
FXT	Yes	No	Slave	1427	1732	5	1	1	2
FXT	Yes	Yes	Slave	1551	1899	5	1	1	2
FXT	No	No	Master	1002	1152	2	1	1	2
FXT	No	Yes	Master	1152	1330	2	1	1	2
FXT	Yes	No	Master	1426	1730	6	1	1	2
FXT	Yes	Yes	Master	1574	1908	6	1	1	2

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 2 and are external to the core which allows them to be shared.

Virtex-6 Devices (Supporting Speeds of up to 3072.0 Mbps)

Table 3 provides approximate device utilization figures for example configurations of the 3072.0 Mbps core in Virtex-6 devices. The values include the GTXE1 control logic and the clock control logic.

Table 3: **Virtex-6 Core Device Utilization[1]**

Parameter Values			Device Resources					
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFRs	BUFGs
Yes	No	Slave	1377	1699	5	1	1	1
Yes	Yes	Slave	1482	1866	5	1	1	1
No	No	Slave	946	1124	1	1	1	1
No	Yes	Slave	1050	1291	1	1	1	1
No	No	Master	940	1122	2	1	1	1
No	Yes	Master	1070	1300	2	1	1	1
Yes	No	Master	1370	1697	6	1	1	1
Yes	Yes	Master	1508	1875	6	1	1	1

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 3 and are external to the core which allows them to be shared.

Virtex-6 Devices (Supporting Speeds of up to 4915.2/6144.0 Mbps)

Table 4 provides approximate device utilization figures for example configurations of the 4915.2/6144.0 Mbps core in Virtex-6 devices. The values include the GTXE1 control logic and the clock control logic.

Table 4: **Virtex-6 Core Device Utilization[1]**

Parameter Values			Device Resources					
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	MMCMs	BUFRs	BUFGs
Yes	No	Slave	2148	2508	5	1	1	1
Yes	Yes	Slave	2272	2669	5	1	1	1
No	No	Slave	1693	1933	1	1	1	1
No	Yes	Slave	1824	2094	1	1	1	1
No	No	Master	1683	1931	2	1	1	1
No	Yes	Master	1838	2103	2	1	1	1
Yes	No	Master	2135	2506	6	1	1	1
Yes	Yes	Master	2287	2678	6	1	1	1

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 4 and are external to the core which allows them to be shared.

Spartan-6 Devices

Table 5 provides approximate device utilization figures for example configurations of the core in Spartan-6 devices. The values include the GTPA1 control logic and the clock control logic.

Table 5: **Spartan-6 Core Device Utilization[1]**

Parameter Values			Device Resources				
Ethernet	R21	Master or Slave	LUTs	FFs	Block RAMs	PLLs	BUFGs
Yes	No	Slave	1373	1661	7	1	4
Yes	Yes	Slave	1489	1828	7	1	4
No	No	Slave	928	1086	1	1	4
No	Yes	Slave	1047	1253	1	1	4
No	No	Master	927	1084	2	1	4
No	Yes	Master	1045	1262	2	1	4
Yes	No	Master	1374	1659	9	1	4
Yes	Yes	Master	1489	1837	9	1	4

1. Additional clocking resources will be required for `eth_ref_clk` (if Ethernet is selected), `hires_clk` (if R21 is selected) and `aux_clk`. These are not included in Table 5 and are external to the core which allows them to be shared.

References

1. *CPRI Specification v4.1*, February 18, 2009 (www.cpri.info).
2. *IEEE Standard 802.3-2005* (standards.ieee.org/getieee802).

Support

Xilinx provides technical support technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices not listed in the documentation, or if customized beyond that allowed in the product documentation, or if any changes are made to the sections marked DO NOT MODIFY.

Ordering Information

The CPRI core can be generated using the Xilinx CORE Generator™ system v12.2 or higher with the applicable service pack. The CORE Generator system is shipped with Xilinx ISE Design Suite Series Development software.

Related Information

Xilinx products are not intended for use in life-support appliances, devices, or systems. Use of a Xilinx product in such application without the written consent of the appropriate Xilinx officer is prohibited.

List of Acronyms

Acronym	Spelled Out
C&M	Control and Management
CPRI	Common Packet Radio Interface
FDD	Frequency Division Duplexing
FF	Flip-Flop
FPGA	Field Programmable Gate Array
GMII	Gigabit Media Independent Interface
HDLC	High-Level Data Link Control
I/Q	in-phase (I) and quadrature-phase (Q) data
IP	Intellectual Property
ISE	Integrated Software Environment
LUT	Lookup Table
MAC	Media Access Controller
NGC	Native Generic Circuit
PLL	Phase-Locked Loop
RAM	Random Access Memory
RE	Radio Equipment
REC	Radio Equipment Controller
UCF	User Constraints File
UMTS	Universal Mobile Telecommunications System
UTRA FDD	UMTS Terrestrial Radio Access - Frequency Division Duplexing
VHDL	VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits)
XAUI	eXtended Attachment Unit Interface
XST	Xilinx Synthesis Technology

Revision History

Date	Version	Revision
08/08/07	1.0	Initial Xilinx release.
3/24/08	1.5	Updated supported tools and performance numbers.
9/05/08	2.1	Early access release.
10/31/08	2.2	Early access release 2.
4/24/09	3.0	Updated to support ISE v11.1.
6/24/09	4.0	Updated to support ISE v11.2.
09/16/09	5.0	Updated to support ISE v11.3.
10/15/09	6.0	Early access release.
4/19/10	7.0	Updated to support ISE v12.1.
7/23/10	8.0	Updated to support ISE v12.2.

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