LogiCORE™ IP AXI External Slave Connector (v1.00.a)

DS805 January 18, 2012 **Product Specification**

Introduction

AXI External Slave Connector (axi_ext_slave_conn), lets you connect an AXI slave device outside of the embedded system module, using embedded module ports, to the master interface of an AXI Interconnect IP without intervening logic. The axi_ext_slave_conn IP core provides the necessary port connection points to represent the connectivity in the system, plus a set of parameters used to configure the master interface of an AXI Interconnect module.

Features

- A set of ports comprising a standard AXI master interface, modeled as an I/O interface of the IP. This can be made external using XPS tools, which provide the necessary signals to connect to an AXI slave device in a top-level system.
- One AXI slave bus-interface that connects to an AXI Interconnect in the embedded system.
- The external master interface ports directly connect to the AXI slave bus-interface, and contain no logic or storage.

LogiCORE IP Facts Table					
Core Specifics					
Core Name	axi_ext_slave_conn				
Supported Device Family(1)	Zynq™-7000, Artix™-7, Virtex®-7, Kintex™-7, Virtex-6, Spartan®-6				
Supported User Interfaces	AXI4, AXI4-Lite				
	Resources				**Frequency**
Configuration	**LUTs**	**FFs**	**DSP Slices**	**Block RAMs**	**Max. Freq.**
Config1	0	0	0	0	N/A
Provided with Core					
Documentation	Product Specification				
Design Files	Verilog, VHDL				
Example Design	Figure 1, page 2				
Test Bench	N/A				
Constraints File	N/A				
Simulation Model	Verilog, VHDL				
Tested Design Tools					
Design Entry Tools	XPS				
Simulation	N/A				
Synthesis Tools	XST				
Support					
Provided by Xilinx, Inc.					

1. For a complete listing of supported devices, see the release notes for this core.

Functional Description

Figure 1 illustrates the AXI external slave connection to an AXI Interconnect.

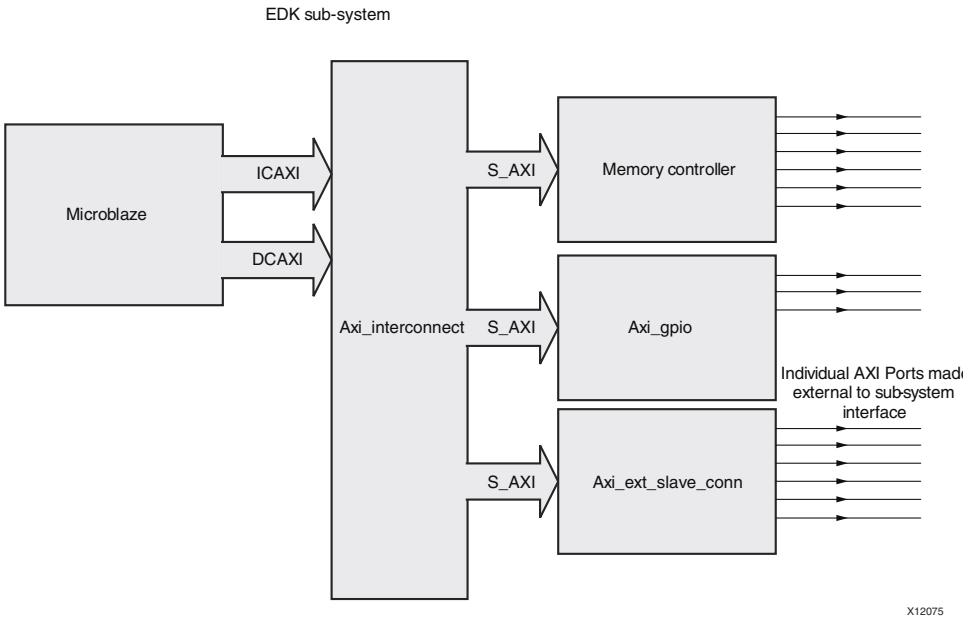

Figure 1: **System Using AXI External Slave Connector**

I/O Signals

AXI Slave Interface Signals

Table 1 lists the slave interface signals that can connect to an axi_interconnect IP in the embedded system.

Table 1: **AXI Slave Interface Signals**

Signal Name	Interface	Signal Type	Description
AXI Write Address Channel Signals (AW)			
S_AXI_AWID [C_S_AXI_ID_WIDTH-1:0]	AW	I	AXI address Write ID.
S_AXI_AWADDR [C_S_AXI_ADDR_WIDTH-1:0]	AW	I	AXI Write address.
S_AXI_AWLEN [7:0]	AW	I	AXI address write burst length.
S_AXI_AWSIZE [2:0]	AW	I	AXI address write burst size.
S_AXI_AWBURST [1:0]	AW	I	AXI address write burst type.
S_AXI_AWLOCK	AW	I	AXI write address lock signal.
S_AXI_AWCACHE [3:0]	AW	I	AXI write address cache control signal.
S_AXI_AWPROT [2:0]	AW	I	AXI write address protection signal.
S_AXI_AWREGION [3:0]	AW	I	Channel address region index
S_AXI_AWQOS [3:0]	AW	I	Channel Quality of Service (QoS).
S_AXI_AWUSER [C_S_AXI_AWUSER_WIDTH-1:0]	AW	I	User-defined AW Channel signals.

Table 1: **AXI Slave Interface Signals *(Cont'd)***

Signal Name	Interface	Signal Type	Description
S_AXI_AWVALID	AW	I	AXI write address valid.
S_AXI_AWREADY	AW	O	AXI write address ready.
AXI Write Data Channel Signals (W)			
S_AXI_WID [C_S_AXI_ID_WIDTH-1:0]	W	I	AXI3 Write ID.
S_AXI_WDATA [C_S_AXI_DATA_WIDTH-1:0]	W	I	AXI write data.
S_AXI_WSTRB [C_S_AXI_DATA_WIDTH/8-1:0]	W	I	AXI write data strobes.
S_AXI_WLAST	W	I	AXI write data last signal. Indicates the last transfer in a write burst.
S_AXI_WUSER [C_S_AXI_WUSER_WIDTH-1:0]	W	I	User-defined W Channel signals.
S_AXI_WVALID	W	I	AXI write data valid.
S_AXI_WREADY	W	O	AXI write data ready.
AXI Write Response Channel Signals (B)			
S_AXI_BID [C_S_AXI_ID_WIDTH-1:0]	B	O	AXI write response ID.
S_AXI_BRESP [1:0]	B	O	AXI write response code.
S_AXI_BUSER [C_S_AXI_BUSER_WIDTH-1:0]	B	O	User-defined B Channel signals.
S_AXI_BVALID	B	O	AXI write response valid.
S_AXI_BREADY	B	I	Write response ready.
AXI Read Address Channel Signals (AR)			
S_AXI_ARID [C_S_AXI_ID_WIDTH-1:0]	AR	I	AXI address read ID.
S_AXI_ARADDR [C_S_AXI_ADDR_WIDTH-1:0]	AR	I	AXI read address.
S_AXI_ARLEN [7:0]	AR	I	AXI address read burst length.
S_AXI_ARSIZE [2:0]	AR	I	AXI address read burst size.
S_AXI_ARBURST [1:0]	AR	I	AXI address read burst type.
S_AXI_ARLOCK	AR	I	AXI read address lock signal.
S_AXI_ARCACHE [3:0]	AR	I	AXI read address cache control signal.
S_AXI_ARPROT [2:0]	AR	I	AXI read address protection signal.
S_AXI_ARREGION [3:0]	AR	I	Channel address region index.
S_AXI_ARQOS [3:0]	AR	I	Channel Quality of Service.
S_AXI_ARUSER [C_S_AXI_ARUSER_WIDTH-1:0]	AR	I	User-defined AR Channel signals.
S_AXI_ARVALID	AR	I	AXI read address valid.
S_AXI_ARREADY	AR	O	AXI read address ready.
AXI Read Data Channel Signals (R)			
S_AXI_RID [C_S_AXI_ID_WIDTH-1:0]	R	O	AXI read data response ID.
S_AXI_RDATA [C_S_AXI_DATA_WIDTH-1:0]	R	O	AXI read data.
S_AXI_RRESP [1:0]	R	O	AXI read response code.
S_AXI_RLAST	R	O	AXI read data last signal.

Table 1: **AXI Slave Interface Signals *(Cont'd)***

Signal Name	Interface	Signal Type	Description
S_AXI_RUSER [C_S_AXI_RUSER_WIDTH-1:0]	R	O	User-defined R Channel signals.
S_AXI_RVALID	R	O	AXI read valid.
S_AXI_RREADY	R	I	Read ready.

External AXI Master I/O Signals

Table 2 lists the AXI Master interface signals that can connect to embedded system ports.

Table 2: **External AXI Master I/O Signals**

Signal Name	Signal Type	Init Status	Description
AXI Write Address Channel Signals (AW)			
M_AXI_AWID [C_S_AXI_ID_WIDTH-1:0]	AW	O	AXI address write ID.
M_AXI_AWADDR [C_S_AXI_ADDR_WIDTH-1:0]	AW	O	AXI Write address.
M_AXI_AWLEN [7:0]	AW	O	AXI address write burst length.
M_AXI_AWSIZE [2:0]	AW	O	AXI address write burst size.
M_AXI_AWBURST [1:0]	AW	O	AXI address write burst type.
M_AXI_AWLOCK	AW	O	AXI write address lock signal.
M_AXI_AWCACHE [3:0]	AW	O	AXI write address cache control signal. (1)
M_AXI_AWPROT [2:0]	AW	O	AXI write address protection signal. (1)
M_AXI_AWREGION [3:0]	AW	O	Write Address Channel address region index. (1)
M_AXI_AWQOS [3:0]	AW	O	Write Address Channel Quality of Service (QoS). (1)
M_AXI_AWUSER [C_S_AXI_AWUSER_WIDTH-1:0]	AW	O	User-defined AW Channel signals.
M_AXI_AWVALID	AW	O	AXI write address valid.
M_AXI_AWREADY	AW	I	AXI write address ready.
AXI Write Data Channel Signals (W)			
M_AXI_WID [C_S_AXI_ID_WIDTH-1:0]	W	O	AXI3 write ID.
M_AXI_WUSER [C_S_AXI_WUSER_WIDTH-1:0]	W	O	User-defined W Channel signals.
M_AXI_WDATA C_S_AXI_DATA_WIDTH-1:0]	W	O	AXI write data.
M_AXI_WSTRB [C_S_AXI_DATA_ WIDTH/8-1:0]	W	O	AXI write data strobes.
M_AXI_WLAST	W	O	AXI write data last signal.
M_AXI_WVALID	W	O	AXI write data valid.
M_AXI_WREADY	W	I	AXI write data ready.
AXI Write Response Channel Signals (B)			
M_AXI_BID [C_S_AXI_ID_WIDTH-1:0]	B	I	AXI write data response ID.
M_AXI_BRESP [1:0]	B	I	AXI write response code.

1. Advanced signal available for connection only when `C_USE_ADVANCED_PORTS=1`.

Table 2: **External AXI Master I/O Signals *(Cont'd)***

Signal Name	Signal Type	Init Status	Description
M_AXI_BUSER [C_S_AXI_BUSER_WIDTH-1:0]	B	I	User-defined B Channel signals.
M_AXI_BVALID	B	I	AXI write response valid.
M_AXI_BREADY	B	O	Write response ready.
AXI Read Address Channel Signals (AR)			
M_AXI_ARID [C_S_AXI_ID_WIDTH-1:0]	AR	O	AXI address read ID.
M_AXI_ARADDR [C_S_AXI_ADDR_WIDTH-1:0]	AR	O	AXI read address.
M_AXI_ARLEN [7:0]	AR	O	AXI address read burst length.
M_AXI_ARSIZE [2:0]	AR	O	AXI address read burst size.
M_AXI_ARBURST [1:0]	AR	O	AXI address read burst type.
M_AXI_ARLOCK	AR	O	AXI read address lock signal. (1)
M_AXI_ARCACHE [3:0]	AR	O	AXI read address cache control signal. (1)
M_AXI_ARPROT [2:0]	AR	O	AXI read address protection signal. (1)
M_AXI_ARREGION [3:0]	AR	O	Channel address region index. (1)
M_AXI_ARQOS [3:0]	AR	O	AR Channel Quality of Service (QoS). (1)
M_AXI_ARUSER [C_S_AXI_ARUSER_WIDTH-1:0]	AR	O	User-defined AR Channel signals.
M_AXI_ARVALID	AR	O	AXI read address valid.
M_AXI_ARREADY	AR	I	AXI read address ready. I
AXI Read Data Channel Signals (R)			
M_AXI_RID [C_S_AXI_ID_WIDTH-1:0]	R	I	AXI read data response ID.
M_AXI_RDATA [C_S_AXI_DATA_WIDTH-1:0]	R	I	AXI Read data.
M_AXI_RRESP [1:0]	R	I	AXI Read response code.
M_AXI_RLAST	R	I	AXI read data last signal.
M_AXI_RUSER [C_S_AXI_RUSER_WIDTH-1:0]	R	I	User-defined Channel Signals.
M_AXI_RVALID	R	I	AXI read valid.
M_AXI_RREADY	R	O	Read ready.

1. Advanced signal available for connection only when `C_USE_ADVANCED_PORTS=1`.

Global I/O Signals

Table 3 lists global signals of the IP.

Table 3: **Global I/O Signals**

Signal Name	Interface	Signal Type	Init Status	Description
Global Signals				
ACLK	Global	I		AXI Bus Clock.
ARESETN	Global	I		AXI active-Low reset.

Parameters

Table 4 lists the user-visible parameters for the IP. In addition to the parameters listed in this table, there are also inferred parameters for the S_AXI interface in the EDK tools. Through the design, these inferred parameters control the behavior of the AXI Interconnect. For a complete list of the interconnect settings related to the AXI interface, see the *AXI Interconnect IP Data Sheet* (DS768).

Table 4: **Parameters**

Parameter Name	Default Value	Allowable Values	Description
C_USE_ADVANCED_PORTS	0	0, 1	Controls whether the less-common (advanced) AXI signals are included in the external master interface.
C_S_AXI_PROTOCOL	AXI4	String (AXI3, AXI4, AXI4LITE)	AXI protocol used by the connected external slave device.
C_S_AXI_ADDR_WIDTH	32	constant (32)	Width of ADDR signals (both S and M interfaces).
C_S_AXI_DATA_WIDTH	32	Integer (32, 64, 128, 256)	Specifies the width of the WDATA and RDATA signals used by the connected external slave device (applies to both S and M interfaces).
C_S_AXI_SUPPORTS_READ	1	0,1	Specifies whether the connected external slave device performs Reads.
C_S_AXI_SUPPORTS_WRITE	1	0,1	Specifies whether the connected external slave device performs Writes.
C_S_AXI_ID_WIDTH	1	1-16	Specifies the number of ID bits produced by the AXI Interconnect to all connected slave devices.
C_S_AXI_SUPPORTS_NARROW_BURST	1	0,1	Specifies whether the connected external slave device supports “narrow bursts” (transfer SIZE less than data width for any multi-beat bursts).
C_S_AXI_SUPPORTS_USER_SIGNALS	0	0,1	Specifies whether the connected external slave device has any USER signals on any AXI channels.
C_S_AXI_AWUSER_WIDTH	1	Integer (1-2147483647	Specifies the number of AWUSER bits produced by the connected external slave device.
C_S_AXI_BUSER_WIDTH	1	Integer (1-2147483647	Specifies the number of BUSER bits on the connected external slave device.
C_S_AXI_ARUSER_WIDTH	1	Integer (1-2147483647	Specifies the number of ARUSER bits on the connected external slave device.
C_S_AXI_WUSER_WIDTH	1	Integer (1-2147483647	Specifies the number of WUSER bits on the connected external slave device.
C_S_AXI_RUSER_WIDTH	1	Integer (1-2147483647	Specifies the number of RUSER bits on the connected external slave device.
C_S_AXI_RNG0-3_BASEADDR	0xFFFFFFFF (2)	Valid Address (1)	Base address of register-type address range 0-3.
C_S_AXI_RNG0-3_HIGHADDR	0x00000000 (2)	Valid Address (1)	High address of register-type address range 0-3.
C_S_AXI_MEM_RNG0-3_BASEADDR	0xFFFFFFFF (2)	Valid Address (1)	Base address of memory-type address range 0-3.
C_S_AXI_MEM_RNG0-3_HIGHADDR	0x00000000 (2)	Valid Address(1)	High address of memory-type address range 0-3.
C_S_AXI_NUM_ADDR_RANGES	1	0-4	Number of register-type address ranges.

Table 4: **Parameters *(Cont'd)***

Parameter Name	Default Value	Allowable Values	Description
C_S_AXI_NUM_MEM_ADDR_RANGES	0	0-4	Number of memory-type address ranges (allows caching).

1. The user must set the values of at least `C_S_AXI_RNG0_BASEADDR` and `C_S_AXI_RNG0_HIGHADDR`. When used, each `C_S_AXI_RNGn_BASEADDR` must be a multiple of the range size (aligned), where the range size is `C_S_AXI_RNGn_HIGHADDR - C_S_AXI_RNGn_BASEADDR + 1`. Each range size must be a power of 2 and at least 4K.
2. Default values indicate unused address ranges.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/21/2010	1.00	Initial Xilinx release.
01/18/2012	1.1	Added the following parameters: • C_S_AXI_MEM_RNG0-3_BASEADDR • C_S_AXI_MEM_RNG0-3_HIGHADDR • C_S_AXI_NUM_ADDR_RANGES • C_S_AXI_NUM_MEM_ADDR_RANGES

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