FCB to FSL Bridge (v1.00a)

DS309 April 24, 2009 **Product Specification**

Introduction

The FCB to FSL Bridge combines the power of the Virtex®-4 PowerPC® APU controller with the ease of use of the Fast Simplex Link (FSL) protocol. The core connects FSL interfaced co-processor cores to the PowerPC 405 processore via the Fabric Co-processor Bus (FCB). This makes it easy to extend the PowerPC processing unit with application specific functions. The FSL protocol is fully compatible with the FSL ports on MicroBlaze™.

For more information on the APU Controller see the *PowerPC 405 Processor Block Reference Guide* [Ref1].

For more information on the FSL protocol see *Fast Simplex Link* [Ref2]

For more information on the FCB core see the *Fabric Co-processor Bus* [Ref3].

Features

- Support for between 1 and 32 FSL master-slave pairs
- Support for all 8 FSL instructions:
  - get: data read from slave FSL
  - cget: control read from slave FSL
  - nget: non-blocking data read from slave FSL
  - ncget: non-blocking control read from slave FSL
  - put: data write to master FSL
  - cput: control write to master FSL
  - nput: non-blocking data write to master FSL
  - ncput: non-blocking control write to master FSL
- Support for both APU controller decoding using User Defined Instructions (UDI), and Fabric Co-processor Module (FCM) decoding
- FSL control error flagged as XEROV
- Failed non-blocking FSL access is flagged as XERCA

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	See EDK Supported Device Families.	
Version of Core	FCB2FSL_bridge	v1.00a
Resources Used		
	Min	Max
Slices	N.A.	N.A.
LUTs	31	145[1]
FFs	48	89[1]
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	N/A	
Design Tool Requirements		
Xilinx Implementation Tools	See Tools for requirements.	
Verification		
Simulation		
Synthesis		
Support		
Provided by Xilinx, Inc.		

1.Assuming 3 FSL pairs. Size depends on number of pairs enabled, and width of FSL data connected to the core.

FCB to FSL Bridge Parameters.

Table 1: **FCB to FSL Bridge Parameters**

Parameter Name	Feature/Description	Allowable Values	Default Value	VHDL Type
C_USE_UDI	0= Decode FSL instructions locally in the FCB to FSL bridge 1= Decode UDI defined FSL instructions in the APU controller	0, 1	1	integer
C_FSL_LINKS	Number of FSL master-slave pairs supported by the bridge	1 to 32	1	integer
C_FSL_DWIDTH	Data width on the FSL ports	32	32	integer
C_FCB_DWIDTH	Data width on the FCB port	32	32	integer
C_PIPELINE_FSL_ACCESS	Increase Fmax by adding one cycle extra latency to FSL accesses	0, 1	0	integer
C_FSL_OFFSET	Reserved for testing purposes	-1	-1	integer

Allowable Parameter Combinations

There are no restrictions on allowable parameter combinations.

FCB to FSL Bridge I/O Signals

The I/O signals for the FCB to FSL Bridge are listed in Table 2

Table 2: **FCB to FSL Bridge I/O Signals**

Signal Name	Interface	I/O	Description
FCB_CLK	system	I	Fabric Co-processor Bus clock
FCB_RST	SFCB	I	Fabric Co-processor Bus reset
FCB_DECODED	SFCB	I	See [Ref1] description of APUFCMDECODED
FCB_DECUDI(0:2)	SFCB	I	See [Ref1] description of APUFCMDECUDI
FCB_DECUDIVALID	SFCB	I	See [Ref1] description of APUFCMDECUDIVALID
FCB_ENDIAN	SFCB	I	Not used.
FCB_FLUSH	SFCB	I	See [Ref1] description of APUFCMFLUSH
FCB_INSTRUCTION(0:C_FCB_DWIDTH-1)	SFCB	I	See [Ref1] description of APUFCMINSTRUCTION
FCB_INSTRVALID	SFCB	I	See [Ref1] description of APUFCMINSTRVALID
FCB_LOADBYTEEN(0:C_FCB_DWIDTH/8-1)	SFCB	I	Not used.
FCB_LOADDATA(0:C_FCB_DWIDTH-1)	SFCB	I	Not used.
FCB_LOADDVALID	SFCB	I	Not used.
FCB_OPERANDVALID	SFCB	I	See [Ref1] description of APUFCMOPERANDVALID
FCB_RADATA(0:C_FCB_DWIDTH-1)	SFCB	I	See [Ref1] description of APUFCMRADATA
FCB_RBDATA(0:C_FCB_DWIDTH-1)	SFCB	I	Not used.
FCB_WRITEBACKOK	SFCB	I	See [Ref1] description of APUFCMWRITEBACKOK

Table 2: **FCB to FSL Bridge I/O Signals *(Continued)***

Signal Name	Interface	I/O	Description
FCB_XERCA	SFCB	I	See [Ref1] description of APUFCMXERCA
FCB_ABORTDECODE	SFCB	I	A slave on the FCB has acknowledged the instruction. Deassert SI_DECODEBUSY in next cycle.
SI_CR(0:3)	SFCB	O	Tied to '0'
SI_DCDCREN	SFCB	O	Tied to '0'
SI_DCDFORCEALIGN	SFCB	O	Tied to '0'
SI_DCDFORCEBESTEERING	SFCB	O	Tied to '0'
SI_DCDFPUOP	SFCB	O	Tied to '0'
SI_DCDGPRWRITE	SFCB	O	See [Ref1] description of FCMAPUDCDGPRWRITE
SI_DCDLDSTBYTE	SFCB	O	Tied to '0'
SI_DCDLDSTDW	SFCB	O	Tied to '0'
SI_DCDLDSTHW	SFCB	O	Tied to '0'
SI_DCDLDSTQW	SFCB	O	Tied to '0'
SI_DCDLDSTWD	SFCB	O	Tied to '0'
SI_DCDLOAD	SFCB	O	Tied to '0'
SI_DCDPRIVOP	SFCB	O	Tied to '1'
SI_DCDRAEN	SFCB	O	See [Ref1] description of FCMAPUDCDRAEN
SI_DCDRBEN	SFCB	O	Tied to '0'
SI_DCDSTORE	SFCB	O	Tied to '0'
SI_DCDTRAPBE	SFCB	O	Tied to '0'
SI_DCDTRAPLE	SFCB	O	Tied to '0'
SI_DCDUPDATE	SFCB	O	Tied to '0'
SI_DCDXERCAEN	SFCB	O	See [Ref1] description of FCMAPUDCDXERCAEN
SI_DCDXEROVEN	SFCB	O	See [Ref1] description of FCMAPUDCDXEROVEN
SI_DECODEBUSY	SFCB	O	Tied to '0'. Single cycle FSL instruction decode
SI_DONE	SFCB	O	See [Ref1] description of FCMAPUDONE
SI_EXCEPTION	SFCB	O	Tied to '0'
SI_EXEBLOCKINGMCO	SFCB	O	Tied to '0'
SI_EXECRFIELD(0:2)	SFCB	O	Tied to "000"
SI_EXENONBLOCKINGMCO	SFCB	O	Tied to '1'
SI_INSTRACK	SFCB	O	See [Ref1] description of FCMAPUINSTRACK
SI_LOADWAIT	SFCB	O	Tied to '0'
SI_RESULT(0:C_FCB_DWIDTH-1)	SFCB	O	See [Ref1] description of FCMAPURESULT
SI_RESULTVALID	SFCB	O	See [Ref1] description of FCMAPURESULTVALID

Table 2: **FCB to FSL Bridge I/O Signals *(Continued)***

Signal Name	Interface	I/O	Description
SI_SLEEPNOTREADY	SFCB	O	See [Ref1] description of FCMAPUSLEEPNOTREADY
SI_XERCA	SFCB	O	See [Ref1] description of FCMAPUXERCA. Used to flag a failed non-blocking FSL access (nget, ncget, nput, ncput)
SI_XEROV	SFCB	O	See [Ref1] description of FCMAPUXEROV. Used to flag an FSL access control error.
FSL#_M_Clk	MFSL#	O	See [Ref2] description of FSL_M_Clk
FSL#_M_Data(0:C_FSL_DWIDTH-1)	MFSL#	O	See [Ref2] description of FSL_M_Data
FSL#_M_Control	MFSL#	O	See [Ref2] description of FSL_M_Control
FSL#_M_Write	MFSL#	O	See [Ref2] description of FSL_M_Write
FSL#_M_Full	MFSL#	I	See [Ref2] description of FSL_M_Full
FSL#_S_Clk	SFSL#	O	See [Ref2] description of FSL_S_Clk
FSL#_S_Data(0:C_FSL_DWIDTH-1)	SFSL#	I	See [Ref2] description of FSL_S_Data
FSL#_S_Control	SFSL#	I	See [Ref2] description of FSL_S_Control
FSL#_S_Read	SFSL#	O	See [Ref2] description of FSL_S_Read
FSL#_S_Exists	SFSL#	I	See [Ref2] description of FSL_S_Exists

Parameter - Port Dependencies

Table 3: **Parameter-Port Dependencies**

Name	Affects	Depends	Relationship Description
Design Parameters			
C_FCB_DWIDTH	FCB_INSTRUCTION FCB_LOADDATA FCB_RADATA FCB_RBDATA FCB_LOADBYTEEN	0 to C_FCB_DWIDTH -1 0 to C_FCB_DWIDTH -1 0 to C_FCB_DWIDTH -1 0 to C_FCB_DWIDTH -1 0 to C_FCB_DWIDTH/8-1	Width of PowerPC processor APU instruction Width of APU load instruction data Width of APU instruction RA operand Width of APU instruction RB operand Width of APU load instruction byte enable
C_FSL_DWDITH	FSL#_M_Data FSL#_S_Data	0 to C_FSL_DWIDTH -1	Width of the FSL data port
C_FSL_LINKS	FSL#_*	0 to C_FSL_LINKS -1	Number of FSL ports that are enabled
I/O Signals			
FCB_INSTRUCTION		C_FCB_DWIDTH	Width required to be 32 bits
FCB_LOADDATA		C_FCB_DWIDTH	Width required to be 32 bits
FCB_RADATA		C_FCB_DWIDTH	Width required to be 32 bits
FCB_RBDATA		C_FCB_DWIDTH	Width required to be 32 bits
FCB_LOADBYTEEN		C_FCB_DWIDTH	Width required to be 4 bits

Table 3: **Parameter-Port Dependencies *(Continued)***

Name	Affects	Depends	Relationship Description
FSL#_M_Data		C_FSL_DWIDTH	Width required to be 32 bits
FSL#_S_Data		C_FSL_DWIDTH	Width required to be 32 bits
FSL#_*		C_FSL_LINKS	Between 1 and 32 FSL master-slave pair ports can be enabled. starting from FSL0.

FCB to FSL Bridge Register Descriptions

There are no registers on the core.

FCB to FSL Bridge Interrupt Descriptions

There are no interrupt signals on the core.

FCB to FSL Bridge Block Diagram

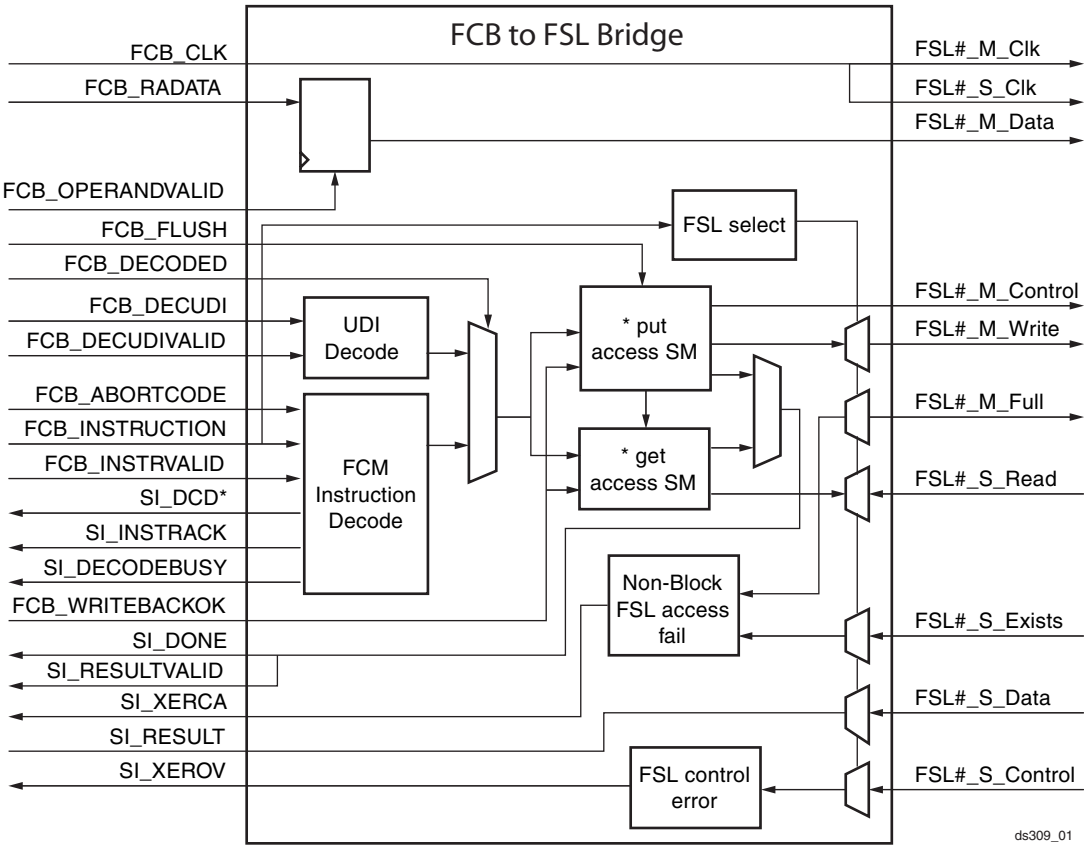

Figure 1: **FCB to FSL Bridge Block Diagram**

Design Implementation

Design Tools

Not applicable.

Target Technology

The target technology is an FPGA listed in EDK Supported Device Families.

Device Utilization and Performance Benchmarks

The FCB to FSL Bridge Fmax depends on the number of FSL ports enabled. For C_FSL_LINKS=1 the core operates in excess of 200 MHz (speed grade -11).

Specification Exceptions

Not applicable.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Reference Documents

1. UG018 PowerPC 405 Processor Block Reference Guide
2. DS449 Fast Simplex Link Data Sheet
3. DS308 Fabric Co-processor Bus Data Sheet

Revision History

Date	Version	Revision
11/15/04	1.0	Initial Xilinx release.
4/24/09	1.1	Replaced references to supported device families and tool name(s) with hyperlink to PDF file.

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