Fabric Co-processor Bus (FCB) (v1.00a)

DS308 April 24, 2009 **Product Specification**

Introduction

The Fabric Co-processor Bus (FCB) connects one or more FPGA fabric accelerator slaves to the Auxiliary Processor Unit (APU) controller in a Virtex®-4 PowerPC® 405.

The slave access decoding is based on the APU instruction code. Each slave must decode a unique set of instructions.

Features

- Single master support
- Multiple slave support
- Slave access selection based on instruction code
- No arbitration between slaves
- Implements the full Fabric Co-processor Module (FCM) interface of the APU controller
- Developed for use with the FCB2FSL_bridge core, and the PPC405_virtex4 wrapper

For more information on the PowerPC APU interface, see [Ref 1].

LogiCORE™ IP Facts		
Core Specifics		
Supported Device Family	Virtex®-4	
Version of Core	fcb_v10	v1.00a
Resources Used		
	Min	Max
Slices	N/A	N/A
LUTs	0	214(1)
FFs	0	0
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	ISE® 11.1 or higher	
Verification	N/A	
Simulation	Mentor Graphics® ModelSim® 6.4b or later	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

1. Assuming three full feature FCB slaves. Actual size depends on number of slaves and the portion of the FCM interface signals they use.

Functional Description

The Fabric Co-processor Bus (FCB) is shown in Figure 1. The core signal names are listed and described in Table 1.

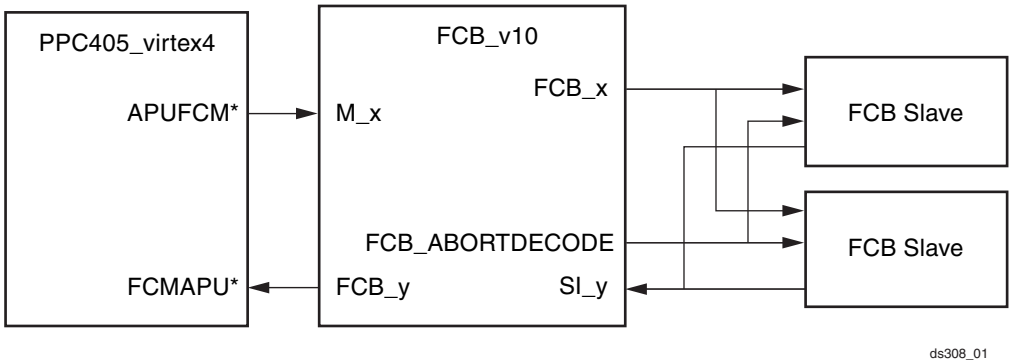

Figure 1: **Typical PowerPC System Using an Fabric Co-processor Bus**

Fabric Co-processor Bus I/O Signals

Table 1: **Fabric Co-processor Bus I/O Ports**

Port Name	MSB:LSB	I/O	Description
FCB_CLK		I	FCB Clock
SYS_Rst		I	External System Reset
FCB_Rst		O	FCB Reset
M_DECODED	[0:(C_FCB_NUM_MASTERS-1)]	I	See [Ref1] description of signal APUFCMDECODED
M_DECUDI	[0:((3*C_FCB_NUM_MASTERS)-1)]	I	See [Ref1] description of signal APUFCMDECUDI
M_DECUDIVALID	[0:(C_FCB_NUM_MASTERS-1)]	I	See [Ref1] description of signal APUFCMDECUDIVALID
M_ENDIAN	[0:(C_FCB_NUM_MASTERS-1)]	I	See [Ref1] description of signal APUFCMENDIAN
M_FLUSH	[0:(C_FCB_NUM_MASTERS-1)]	I	See [Ref1] description of signal APUFCMFLUSH
M_INSTRUCTION	[0:((C_DATA_WIDTH*C_FCB_NUM_MASTERS)-1)]	I	See [Ref1] description of signal APUFCMINSTRUCTION
M_INSTRVALID	[0:(C_FCB_NUM_MASTERS-1)]	I	See [Ref1] description of signal APUFCMINSTRVALID
M_LOADBYTEEN	[0:((C_DATA_WIDTH/8*C_FCB_NUM_MASTERS)-1)]	I	See [Ref1] description of signal APUFCMLOADBYTEEN
M_LOADDATA	[0:((C_DATA_WIDTH*C_FCB_NUM_MASTERS)-1)]	I	See [Ref1] description of signal APUFCMLOADDATA
M_LOADDVALID	[0:(C_FCB_NUM_MASTERS-1)]	I	See [Ref1] description of signal APUFCMLOADDVALID
M_OPERAND VALID	[0:(C_FCB_NUM_MASTERS-1)]	I	See [Ref1] description of signal APUFCMOPERANDVALID

Table 1: **Fabric Co-processor Bus I/O Ports *(Cont'd)***

Port Name	MSB:LSB	I/O	Description
M_RADATA	[0:((C_DATA_WIDTH* C_FCB_NUM_ MASTERS)-1)]	I	See [Ref1] description of signal APUFCMRADATA
M_RBDATA	[0:((C_DATA_WIDTH* C_FCB_NUM_ MASTERS)-1)]	I	See [Ref1] description of signal APUFCMRBDATA
M_WRITEBACK OK	[0:(C_FCB_NUM_ MASTERS-1)]	I	See [Ref1] description of signal APUFCMWRITEBACKOK
M_XERCA	[0:(C_FCB_NUM_ MASTERS-1)]	I	See [Ref1] description of signal APUFCMXERCA
FCB_CR	[0:3]	O	See [Ref1] description of signal FCMAPUCR
FCB_DCDCREN		O	See [Ref1] description of signal FCMAPUDCDCREN
FCB_DCDFORCE ALIGN		O	See [Ref1] description of signal FCMAPUDCDFORCEALIGN
FCB_DCDFORCE BESTEERING		O	See [Ref1] description of signal FCMAPUDCDFORCEBESTEERING
FCB_DCDFPUOP		O	See [Ref1] description of signal FCMAPUDCDFPUOP
FCB_DCDGPR WRITE		O	See [Ref1] description of signal FCMAPUDCDGPRWRITE
FCB_DCDLDST BYTE		O	See [Ref1] description of signal FCMAPUDCDLDSTBYTE
FCB_DCDLDS TDW		O	See [Ref1] description of signal FCMAPUDCDLDSTDW
FCB_DCDLDS THW		O	See [Ref1] description of signal FCMAPUDCDLDSTHW
FCB_DCDLDS TQW		O	See [Ref1] description of signal FCMAPUDCDLDSTQW
FCB_DCDLDS TWD		O	See [Ref1] description of signal FCMAPUDCDLDSTWD
FCB_DCDLOAD		O	See [Ref1] description of signal FCMAPUDCDLOAD
FCB_DCDPRI VOP		O	See [Ref1] description of signal FCMAPUDCDPRIVOP
FCB_DCDRAEN		O	See [Ref1] description of signal FCMAPUDCDRAEN
FCB_DCDRBEN		O	See [Ref1] description of signal FCMAPUDCDRBEN
FCB_DCDSTORE		O	See [Ref1] description of signal FCMAPUDCDSTORE
FCB_DCDTRAP BE		O	See [Ref1] description of signal FCMAPUDCDTRAPBE
FCB_DCDTRAP LE		O	See [Ref1] description of signal FCMAPUDCDTRAPLE
FCB_DCDUP DATE		O	See [Ref1] description of signal FCMAPUDCDUPDATE
FCB_DCDXERCA EN		O	See [Ref1] description of signal FCMAPUDCDXERCAEN

Table 1: **Fabric Co-processor Bus I/O Ports *(Cont'd)***

Port Name	MSB:LSB	I/O	Description
FCB_DCDXEROV EN		O	See [Ref1] description of signal FCMAPUDCDXEROVEN
FCB_DECODE BUSY		O	See [Ref1] description of signal FCMAPUDECODEBUSY
FCB_DONE		O	See [Ref1] description of signal FCMAPUDONE
FCB_EXCEPTION		O	See [Ref1] description of signal FCMAPUEXCEPTION
FCB_EXE BLOCKINGMCO		O	See [Ref1] description of signal FCMAPUEXEBLOCKINGMCO
FCB_EXECR FIELD	[0:2]	O	See [Ref1] description of signal FCMAPUEXECRFIELD
FCB_EXENON BLOCKINGMCO		O	See [Ref1] description of signal FCMAPUEXENONBLOCKINGMCO
FCB_INSTRACK		O	See [Ref1] description of signal FCMAPUINSTRACK
FCB_LOADWAIT		O	See [Ref1] description of signal FCMAPULOADWAIT
FCB_RESULT	[0:C_DATA_WIDTH-1]	O	See [Ref1] description of signal FCMAPURESULT
FCB_RESULT VALID		O	See [Ref1] description of signal FCMAPURESULTVALID
FCB_SLEEP NOTREADY		O	See [Ref1] description of signal FCMAPUSLEEPNOTREADY
FCB_FCM_ XERCA		O	See [Ref1] description of signal FCMAPUXERCA
FCB_XEROV		O	See [Ref1] description of signal FCMAPUXEROV
FCB_DECODED		O	Slave side version of M_DECODED
FCB_DECUDI	[0:2]	O	Slave side version of M_DECUDI
FCB_DECUDI VALID		O	Slave side version of M_DECUDIVALID
FCB_ENDIAN		O	Slave side version of M_ENDIAN
FCB_FLUSH		O	Slave side version of M_FLUSH
FCB_ INSTRUCTION	[0:C_DATA_WIDTH-1]	O	Slave side version of M_INSTRUCTION
FCB_INSTRVALID		O	Slave side version of M_INSTRVALID
FCB_LOADBYTEE N	[0:C_DATA_WIDTH/8-1]	O	Slave side version of M_LOADBYTEEN
FCB_LOADDATA	[0:C_DATA_WIDTH-1]	O	Slave side version of M_LOADDATA
FCB_LOADD VALID		O	Slave side version of M_LOADDVALID
FCB_OPERAND VALID		O	Slave side version of M_OPERANDVALID
FCB_RADATA	[0:C_DATA_WIDTH-1]	O	Slave side version of M_RADATA
FCB_RBDATA	[0:C_DATA_WIDTH-1]	O	Slave side version of M_RBDATA
FCB_WRITE BACKOK		O	Slave side version of M_WRITEBACKOK

Table 1: **Fabric Co-processor Bus I/O Ports *(Cont'd)***

Port Name	MSB:LSB	I/O	Description
FCB_APU_ XERCA		O	Slave side version of M_XERCA
FCB_ABORT DECODE		O	Signal to slaves that are still asserting the SI_DECODEBUSY that the instruction has already been successfully decoded and that they should deassert SI_DECODEBUSY
SI_CR	[0:((4*C_FCB_NUM_ SLAVES)-1)]	I	Slave side version of signal FCB_CR.
SI_DCDCREN	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDCREN.
SI_DCDFORCE ALIGN	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDFORCEALIGN.
SI_DCDFORCE BESTEERING	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDFORCEBESTEERING.
SI_DCDFPUOP	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDFPUOP.
SI_DCDGPR WRITE	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDGPRWRITE.
SI_DCDLDST BYTE	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDLDSTBYTE.
SI_DCDLDSTDW	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDLDSTDW.
SI_DCDLDSTHW	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDLDSTHW.
SI_DCDLDSTQW	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDLDSTQW.
SI_DCDLDSTWD	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDLDSTWD.
SI_DCDLOAD	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDLOAD.
SI_DCDPRIVOP	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDPRIVOP.
SI_DCDRAEN	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDRAEN.
SI_DCDRBEN	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDRBEN.
SI_DCDSTORE	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDSTORE.
SI_DCDTRAPBE	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDTRAPBE.
SI_DCDTRAPLE	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDTRAPLE.
SI_DCDUPDATE	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDUPDATE.
SI_DCDXERCA EN	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDXERCAEN.

Table 1: **Fabric Co-processor Bus I/O Ports *(Cont'd)***

Port Name	MSB:LSB	I/O	Description
SI_DCDXER OVEN	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DCDXEROVEN.
SI_EXE BLOCKINGMCO	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_EXEBLOCKINGMCO.
SI_EXECRFIELD	[0:((3*C_FCB_NUM_SLAVE S)-1)]	I	Slave side version of signal FCB_EXECRFIELD.
SI_EXENON BLOCKINGMCO	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_EXENONBLOCKINGMCO.
SI_INSTRACK	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_INSTRACK
SI_DECODE BUSY	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DECODEBUSY. Must be raised by slave in cycle after FCB_ABORTDECODE is asserted
SI_DONE	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_DONE
SI_EXCEPTION	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_EXCEPTION
SI_LOADWAIT	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_LOADWAIT
SI_RESULT	[0:((C_DATA_WIDTH* C_FCB_NUM_SLAVES)-1)]	I	Slave side version of signal FCB_RESULT
SI_RESULT VALID	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_RESULTVALID
SI_SLEEP NOTREADY	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_SLEEPNOTREADY
SI_XERCA	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_XERCA
SI_XEROV	[0:(C_FCB_NUM_ SLAVES-1)]	I	Slave side version of signal FCB_XEROV

Fabric Co-processor Bus Parameters

Table 2: **Fabric Co-processor Bus Design Parameters**

Parameter Name	Feature/Description	Allowable Values	Default Value	VHDL Type
C_FCB_NUM_ MASTERS	Number of FCB Masters	1	1	integer
C_FCB_NUM_ SLAVES	Number of FCB Slaves	1–16	1	integer
C_DATA_WIDTH	FCB Data Bus Width	32	32	integer
C_EXT_RESET_ HIGH	Level of external reset	0 = Active low reset 1 = Active high reset	1	integer

Allowable Parameter Combinations

There are no restrictions on parameter combinations.

Parameter - Port Dependencies

The parameter-port dependencies for the Fabric Co-processor Bus are listed in Table 3.

Table 3: **Fabric Co-processor Bus Parameter - Port Dependencies**

Parameter Name	Ports (Port width depends on parameter)
C_FCB_NUM_ MASTERS	M_*
C_FCB_NUM_SLAVES	Sl_*
C_DATA_WIDTH	*_INSTRUCTION, *_LOADDATA, *_LOADBYTEEN, *_RADATA, *_RBDATA, *_RESULT
C_EXT_RESET_HIGH	none

Fabric Co-processor Bus Register Descriptions

Not applicable.

Fabric Co-processor Bus Interrupt Descriptions

Not applicable.

Design Implementation

Design Tools

The Fabric Co-processor Bus design is hand written.

XST is the synthesis tool used for synthesizing the Fabric Co-processor Bus. The NGC netlist output from XST is then input to the Xilinx ISE tool suite for actual device implementation.

Target Technology

The intended target technology is an FPGA in one of the following families: Virtex-4.

Device Utilization and Performance Benchmarks

Not applicable.

Specification Exceptions

Not applicable.

Reference Documents

1. UG018, *PowerPC 405 Processor Block Reference Guide*

Support

Xilinx provides technical support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/12/04	1.0	Initial Xilinx release.
8/2/05	1.1	Converted to the new DS template.
9/25/07	1.2	Fixed parameter name C_DATA_WIDTH.
4/24/09	1.5	Updated to support ISE 11.1.

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