Fabric Coprocessor Bus for the Virtex-5 FPGA Embedded Processor Block (v1.00a)

DS725 April 24, 2008 **Product Specification**

Introduction

The Fabric Co-processor Bus for the PowerPC® 440 Processor (FCB V20) connects one or more FPGA fabric accelerator slaves to the Auxiliary Processor Unit (APU) controller in a Virtex®-5FX FPGA with a PowerPC 440 processor.

The slave access decoding is based on the APU instruction code. Each slave must decode a unique set of instructions.

Features

- Single master support
- Multiple slave support
- Slave access selection based on instruction code
- No arbitration between slaves
- Implements the full Fabric Co-processor Module (FCM) interface of the APU controller

LogiCORE™ IP Facts		
Core Specifics		
Supported Device Family	See EDK Supported Device Families.	
Resources Used		
	Min	Max
Slices	N/A	N/A
LUTs	0	214(1)
FFs	0	0
Block RAMs	0	0
Special Features		Add if applicable
Provided with Core		
Documentation		Product Specification
Design File Formats		VHDL
Constraints File		N/A
Verification		N/A
Instantiation Template		N/A
Additional Items		None
Design Tool Requirements		
Xilinx Implementation Tools	See Tools for requirements.	
Verification		
Simulation		
Synthesis		
Support		
Provided by Xilinx, Inc.		

1. Assuming three full feature FCB slaves. The actual size depends on the number of slaves and the portion of the FCM interface signals that they use.

I/O Signals

The FCB V20 I/O signal names and descriptions are shown in Table 1.

Table 1: **FCB V20 I/O Signals**

Port Name	MSB:LSB	I/O	Description
FCB_CLK		I	FCB Clock
SYS_Rst		I	External System Reset
FCB_Rst		O	FCB Reset
M_DECUDI	[0:3]	I	Connects to APUFCMDECUDI of PPC440
M_DECUDIVALID		I	Connects to APUFCMDECUDIVALID of PPC440
M_ENDIAN		I	Connects to APUFCMENDIAN of PPC440
M_FLUSH		I	Connects to APUFCMFLUSH of PPC440
M_INSTRUCTION	[0:31]	I	Connects to APUFCMINSTRUCTION of PPC440
M_INSTRVALID		I	Connects to APUFCMINSTRVALID of PPC440
M_LOADBYTEADDR	[0:3]	I	Connects to APUFCMLOADBYTEADDR of PPC440
M_LOADDATA	[0:127]	I	Connects to APUFCMLOADDATA of PPC440
M_LOADDVALID		I	Connects to APUFCMLOADDVALID of PPC440
M_OPERANDVALID		I	Connects to APUFCMOPERANDVALID of PPC440
M_RADATA	[0:31]	I	Connects to APUFCMRADATA of PPC440
M_RBDATA	[0:31]	I	Connects to APUFCMRBDATA of PPC440
M_WRITEBACKOK		I	Connects to APUFCMWRITEBACK OK of PPC440
M_DECFPUOP		I	Connects to APUFCMDECFPUOP of PPC440
M_DECLOAD		I	Connects to APUFCMDECLOAD of PPC440
M_DECSTORE		I	Connects to APUFCMDECSTORE of PPC440
M_DECLDSTXFERSIZE	[0:2]	I	Connects to APUFCMDECLDSTXFERSIZE of PPC440
M_DECNONAUTON		I	Connects to APUFCMDECNONAUTON of PPC440
M_NEXTINSTRREADY		I	Connects to APUFCMNEXTINSTRREADY of PPC440
M_MSRFE0		I	Connects to APUFCMMSRFE0 of PPC440
M_MSRFE1		I	Connects to APUFCMMSRFE1 of PPC440
FCB_CR	[0:3]	O	Multiplexed from SI_CR as selected by SI_RESULTVALID
FCB_DONE		O	Logical OR of DONE signals from all slaves
FCB_EXCEPTION		O	Logical OR of EXCEPTION signals from all slaves
FCB_RESULT	[0:31]	O	Multiplexed from SI_RESULT as selected by SI_RESULTVALID
FCB_RESULTVALID		O	Logical OR of RESULTVALID signals from all slaves
FCB_SLEEPNOTREADY		O	Logical OR of SLEEPNOTREADY signals from all slaves
FCB_STOREDATA	[0:127]	O	Multiplexed from SI_STOREDATA as selected by SI_RESULTVALID

Table 1: **FCB V20 I/O Signals *(Cont'd)***

Port Name	MSB:LSB	I/O	Description
FCB_CONFIRMINSTR		O	Logical OR of CONFIRMINSTR signals from all slaves
FCB_FPSCRFEX		O	Logical OR of FPSCRFEX signals from all slaves
FCB_DECUDI	[0:3]	O	Slave side version of M_DECUDI
FCB_DECUDIVALID		O	Slave side version of M_DECUDIVALID
FCB_ENDIAN		O	Slave side version of M_ENDIAN
FCB_FLUSH		O	Slave side version of M_FLUSH
FCB_INSTRUCTION	[0:31]	O	Slave side version of M_INSTRUCTION
FCB_INSTRVALID		O	Slave side version of M_INSTRVALID
FCB_LOADBYTEADDR	[0:3]	O	Slave side version of M_LOADBYTEADDR
FCB_LOADDATA	[0:127]	O	Slave side version of M_LOADDATA
FCB_LOADDVALID		O	Slave side version of M_LOADDVALID
FCB_OPERANDVALID		O	Slave side version of M_OPERANDVALID
FCB_RADATA	[0:31]	O	Slave side version of M_RADATA
FCB_RBDATA	[0:31]	O	Slave side version of M_RBDATA
FCB_WRITEBACKOK		O	Slave side version of M_WRITEBACKOK
FCB_DECFPUOP		O	Slave side version of signal FCB_DECFPUOP.
FCB_DECLOAD		O	Slave side version of signal FCB_DECLOAD.
FCB_DECSTORE		O	Slave side version of signal FCB_DECSTORE.
FCB_DECLDSTXFERSIZE	[0:2]	O	Slave side version of signal FCB_DECLDSTXFERSIZE.
FCB_DECNONAUTON		O	Slave side version of signal FCB_DECNONAUTON.
FCB_NEXTINSTRREADY		O	Slave side version of signal FCB_NEXTINSTRREADY.
FCB_MSRFE0		O	Slave side version of signal FCB_MSRFE0.
FCB_MSRFE1		O	Slave side version of signal FCB_MSRFE1.
SI_CR	[0:4*C_FCB_NUM_SLAVES-1]	I	CR value from each slave
SI_DONE	[0:C_FCB_NUM_SLAVES-1]	I	DONE signal from each slave
SI_EXCEPTION	[0:C_FCB_NUM_SLAVES-1]	I	EXCEPTION signal from each slave
SI_RESULT	[0:32*C_FCB_NUM_SLAVES-1]	I	RESULT value from each slave
SI_RESULTVALID	[0:C_FCB_NUM_SLAVES-1]	I	RESULTVALID signal from each slave; indicates which slave is responding
SI_SLEEPNOTREADY	[0:C_FCB_NUM_SLAVES-1]	I	SLEEPNOTREADY signal from each slave
SI_STOREDATA	[0:128*C_FCB_NUM_SLAVES-1]	I	STOREDATA value from each slave

Table 1: **FCB V20 I/O Signals *(Cont'd)***

Port Name	MSB:LSB	I/O	Description
SI_CONFIRMINSTR	[0:C_FCB_NUM_SLAVES-1]	I	CONFIRMINSTR signal from each slave
SI_FPSCRFEX	[0:C_FCB_NUM_SLAVES-1]	I	FPSCRFEX signal from each slave

FCB V20 Parameters

The FCB V20 parameters names and descriptions are shown in Table 2.

Table 2: **FCB V20 Design Parameters**

Parameter Name	Feature/Description	Allowable Values	Default Value	VHDL Type
C_FCB_NUM_MASTERS	Number of FCB Masters	1	1	integer
C_FCB_NUM_SLAVES	Number of FCB Slaves (automatically set by tools)	1–16	1	integer
C_DATA_WIDTH	FCB Data Bus Width (for operands and result)	32	32	integer
C_EXT_RESET_HIGH	Level of external reset	0 = Active low reset 1 = Active high reset	1	integer
C_DECUDI_WIDTH	Width of UDI decode vector	4	4	integer
C_LBA_WIDTH	LOADBYTEADDR width	4	4	integer
C_LDSDATA_WIDTH	Load and store data bus width	128	128	integer

Reference Documents

1. UG200 Embedded Processor Block in Virtex-5 FPGAs Reference Guide

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Revision History

Date	Version	Description of Revisions
1/17/08	1.0	Initial Xilinx release
4/24/09	1.1	Replaced references to supported device families and tool name(s) with hyperlink to IP_details file; converted to current DS template.

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