Local Memory Bus (LMB) v1.0 (v1.00a)

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Product Specification

Introduction

The LMB_V10 module is used as the LMB interconnect for Xilinx FPGA based embedded processor systems. The LMB is a fast, local bus for connecting MicroBlaze™ instruction and data ports to high-speed peripherals, primarily on-chip block RAM (BRAM).

Features

- Efficient, single master bus (requires no arbiter)
- Separate read and write data buses
- Low FPGA resource utilization
- 125 MHz operation

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	QPro™-R Virtex™-II, QPro Virtex-II, Spartan™-II, Spartan-IIE, Spartan-3, Virtex, Virtex-II, Virtex-II Pro, Virtex-4, Virtex-E	
Version of Core	lmb_v10	v1.00a
Resources Used		
	Min	Max
Slices	N/A	N/A
LUTs	0	353
FFs	0	0
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	ISE 6.3i or higher	
Verification	N/A	
Simulation	ModelSim SE/PE 5.7b or later	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

Local Memory Bus Parameters

Table 1: **LMB_V20 Design Parameters**

Parameter Name	Feature/Description	Allowable Values	Default Value	VHDL Type
C_LMB_NUM_SLAVES	Number of LMB Slaves	1–16	4	integer
C_LMB_AWIDTH	LMB Address Bus Width	32	32	integer
C_LMB_DWIDTH	LMB Data Bus Width	32	32	integer
C_EXT_RESET_HIGH	Level of external reset	0 = Active low reset 1 = Active high reset	1	integer

Allowable Parameter Combinations

There are no restrictions on parameter combinations.

LMB_V10 I/O Signals

The I/O ports for the LMB_V10 are listed in Table 2.

Table 2: **LMB_V10 I/O Ports**

Port Name	MSB:LSB	I/O	Description
LMB_CLK		I	LMB Clock
SYS_Rst		I	External System Reset
LMB_Rst		O	LMB Reset
M_ABus	0:C_LMB_AWIDTH-1	I	Master Address Bus
M_ReadStrobe		I	Master Read Strobe
M_WriteStrobe		I	Master Write Strobe
M_AddrStrobe		I	Master Address Strobe
M_DBus	0:C_LMB_DWIDTH-1	I	Master Databus
M_BE	0:C_LMB_DWIDTH/8-1	I	Master Byte Enables
Sl_DBus	0:C_LMB_DWIDTH*C_LMB_NUM_SLAVES-1	O	Slave Data Bus
Sl_Ready	0:C_LMB_NUM_SLAVES-1	O	Slave Data Ready
LMB_ABus	0:C_LMB_AWIDTH-1	O	LMB Address Bus
LMB_ReadStrobe		O	LMB Read Strobe
LMB_WriteStrobe		O	LMB Write Strobe
LMB_AddrStrobe		O	LMB Address Strobe
LMB_ReadDBus	0:C_LMB_DWIDTH-1	O	LMB Read Data Bus
LMB_WriteDBus	0:C_LMB_DWIDTH-1	O	LMB Write Data Bus
LMB_Ready		O	LMB Data Ready
LMB_BE	0:C_LMB_DWIDTH/8-1	O	LMB Byte Enables

Parameter - Port Dependencies

The parameter-port dependencies for the LMB_V10 are listed in Table 3.

Table 3: **LMB_V10 Parameter - Port Dependencies**

Parameter Name	Ports (Port width depends on parameter)
C_LMB_NUM_SLAVES	SI_DBus, SI_Ready
C_LMB_AWIDTH	M_ABus, LMB_ABus
C_LMB_DWIDTH	M_DBus, M_BE, SI_DWIDTH, LMB_ReadDBus, LMB_WriteDBus, LMB_BE
C_EXT_RESET_HIGH	none

LMB_V10 Register Descriptions

Not applicable.

LMB_V10 Interrupt Descriptions

Not applicable.

LMB_V10 Block Diagram

A typical MicroBlaze system using two LMB_V10s is shown below in Figure 1. This system illustrates the use of both I and D side LMB buses connecting to a dual-ported BRAM Block via separate LMB BRAM interface controllers.

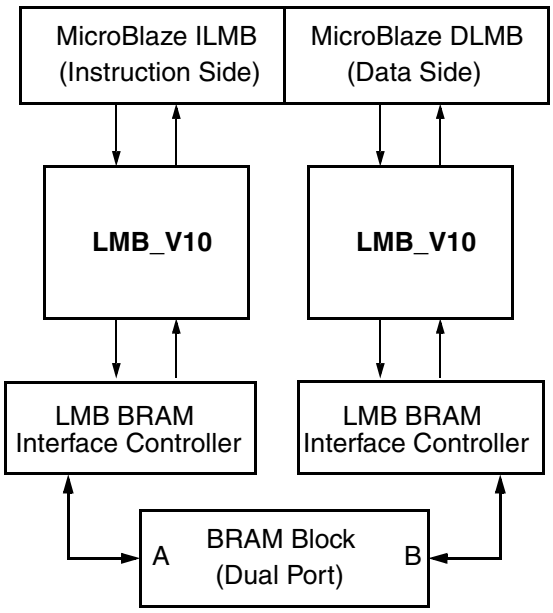

Figure 1: **Typical MicroBlaze System Using Two LMB_V10s**

Design Implementation

Design Tools

The LMB_V10 design is hand written.

XST is the synthesis tool used for synthesizing the LMB_V10. The NGC netlist output from XST is then input to the Xilinx Alliance tool suite for actual device implementation.

Target Technology

The intended target technology is an FPGA in one of the following families: Virtex, Virtex-E, Spartan-II, Spartan-IIE, Spartan--3, Virtex-II, QPro Virtex-II, QPro-R Virtex-II, Virtex-II Pro, or Virtex-4.

Device Utilization and Performance Benchmarks

A comparison of the LMB with the other major bus types used in Xilinx embedded processor systems is shown below in Table 4.

Table 4: **Buses used in Xilinx Embedded Processor systems**

Feature	CoreConnect Buses			Other Buses	
	PLB	OPB	DCR	OCM	LMB
Processor family	PPC405	PPC405, MicroBlaze	PPC405	PPC405	MicroBlaze
Data bus width	64	32	32	32	32
Address bus width	32	32	10	32	32
Clock rate, MHz (max)[1]	100	125	125	375	125
Masters (max)	16	16	1	1	1
Masters (typical)	2-8	2-8	1	1	1
Slaves (max)[2]	16	16	16	1	16
Slaves (typical)	2-6	2-8	1-8	1	1
Data rate (peak)[3]	800 MB/s	500 MB/s	500 MB/s	1500 MB/s	500 MB/s
Concurrent read/write	Yes	No	No	No	No
Address pipelining	Yes	No	No	No	No
Bus locking	Yes	Yes	No	No	No
Retry	Yes	Yes	No	No	No
Timeout	Yes	Yes	No	No	No
Fixed burst	Yes	No	No	No	No
Variable burst	Yes	No	No	No	No
Cache fill	Yes	No	No	No	No
Target word first	Yes	No	No	No	No
FPGA resource usage	High	Medium	Low	Low	Low
Compiler support for load/store	Yes	Yes	No	Yes	Yes

Notes:
1. Maximum clock rates are estimates and are presented for comparison only. The actual maximum clock rate for each bus is dependent on device family, device speed grade, design complexity, and other factors.
2. Maximum value set by maximum allowed parameter value specified in the core. Actual bus specification does not limit this value.
3. Peak data rate is the maximum theoretical data transfer rate at the clock rate shown for each bus.

Specification Exceptions

Not applicable.

Reference Documents

None.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/12/02	1.0	Initial Xilinx release.
01/07/03	1.2	Update for SP3
07/08/03	1.3	Update to new template
01/26/04	1.4	Updates to TM and copyright
08/13/04	1.5	Updated for Gmm; updated content format, reviewed and updated trademarks and supported device family listing
4/4/05	1.6	Updated for EDK 7.1.1 SP1 release; updated trademarks and supported device listing.