LogiCORE IP 3GPP LTE Channel Estimator v1.1

XMP119 October 16, 2012 **Product Brief**

Overview

The Xilinx LogiCORE™ IP 3GPP LTE Channel Estimator v1.1 implements AXI4-Stream compliant, channel estimation functionality suitable to support decoding of the Physical Uplink Shared Channel (PUSCH) in LTE eNodeB applications as defined in 3GPP TS 36.211 specification. It represents one IP component in the Xilinx broader LTE Baseband Targeted Design Platform (TDP).

Features

- Drop-in module for Zynq™-7000, Virtex®-7, Kintex™-7, Virtex-6, Virtex-6L and Virtex-5 devices
- AXI4-Streaming-compliant interfaces
- Support of channel estimation for 3GPP LTE Physical Uplink Shared Channel (PUSCH) with Single-Input, Single-Output (SISO) and Single-Input, Multiple-Output (SIMO) communication modes, Multi-User Multiple Input Multiple Output (MU-MIMO) communication modes
- Compliance with 3GPP-LTE TS 36.211 v.8.9 (Release 8) and v9.0 (Release 9) standard specifications
- Support of Xilinx LTE Uplink Targeted Design Platform (TDP)
- Parameterizable input/output data precision
- Bit accurate C-Language simulation model for system level modeling
- Optimized for Xilinx high performance Virtex-6 FPGAs

Applications

Base station applications implementing eNodeB following the LTE specifications (3GPP TS 36.211). The 3GPP LTE Channel Estimator v1.0 can perform the channel estimation function required for decoding of the PUSCH uplink data transmission in SISO and MU-MIMO modes of communication.

Additional Documentation and Supporting Materials

A full data sheet and additional supporting materials (C models and accompanying user guide documentation) are available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/chest_lte_eval/index.htm.

Technical Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Refer to the IP Release Notes Guide (XTP025) for more information on this core. There will be a link to all DSP IP and then to the relevant core. For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core Site License Agreement. The module is shipped as part of the Vivado Design Suite and ISE Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information on pricing and availability. of Xilinx LogiCORE IP modules. Information about additional modules is also available at the Xilinx IP Center.

For more information, visit the 3GPP LTE Channel Estimator web page.

Information about other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
09/21/10	1.0	Initial Xilinx release
08/15/11	1.1	Updated to include web registration information
10/19/11	1.2	Updated for Release 13.3. Version 1.1 of Channel Estimator. Updated to include Virtex-7, Kintex-7 and Zynq-7000 support
10/16/12	2.0	Minor document updates for 2012.3/14.3

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