

Introduction

The Xilinx® LogiCORE™ IP LTE RACH Detector core decodes PRACH data encoded according to the 3GPP TS 36.211 v9.0 (2009-12) Physical Channels and Modulation specification.

Additional Documentation

A full product guide is available for this core. Access to this material may be requested by clicking on this registration link:

www.xilinx.com/member/lte_rach_detector_eval/index.htm

Features

- Channel detection for 3GPP TS 36.211 v9.0.0 (2009-12)
- Supports Formats 0-4
- Supports up to 64 roots
- Supports up to 4 antennas
- Supports multiplexing in frequency, for up to 6 frequency channels
- Supports 5, 10, 15 and 20 MHz bandwidth.
- C model available for the core
- Fully optimized for speed and area
- Fully synchronous design using a single clock

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family ⁽¹⁾	UltraScale+™ UltraScale™ Zynq®-7000 All Programmable SoC 7 Series
Supported User Interfaces	Native ⁽²⁾
Provided with Core	
Design Files	VHDL and Netlist ⁽³⁾
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	C Model ⁽³⁾
Tested Design Tools⁽⁴⁾	
Design Entry	Vivado® Design Suite
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide .
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. Interface similar to AXI and can be connected to an AXI4-Stream interface.
3. Design files and C model available in the core [lounge](#) (registration required).
4. For the supported versions of the tools, see the [Xilinx Design Tools: Release Notes Guide](#).

Overview

The LTE RACH detector core provides a RACH detection solution for the 3GPP TS 36.211 v9.0.0 (2009-12) specification. The LTE RACH detector searches through the received antenna samples and correlates against one or more (up to 64) RACH preamble sequences. The sequences are generated from Zadoff-Chu sequences, as defined in section 5.7 of 3GPP TS 36.211 v9.0.0 (2009-12).

At the eNode-B, the correlation results from the RACH detector are used to detect UE access attempts and compute/update UE transmission timing advance to ensure that the signals received from all UEs are time synchronized within the cyclic prefix (CP).

The RACH detector core performs a cyclic correlation for each Zadoff-Chu root it is configured to detect. This identifies all of the peaks resulting from each cyclic shifted copy of the root.

The architecture has been designed to provide efficient use of the FPGA. All processing-intensive and timing-critical operations are performed by the FPGA. The interface to the core can be attached to any bus-based system. The memory-mapped interface allows for simple integration and validation within the system.

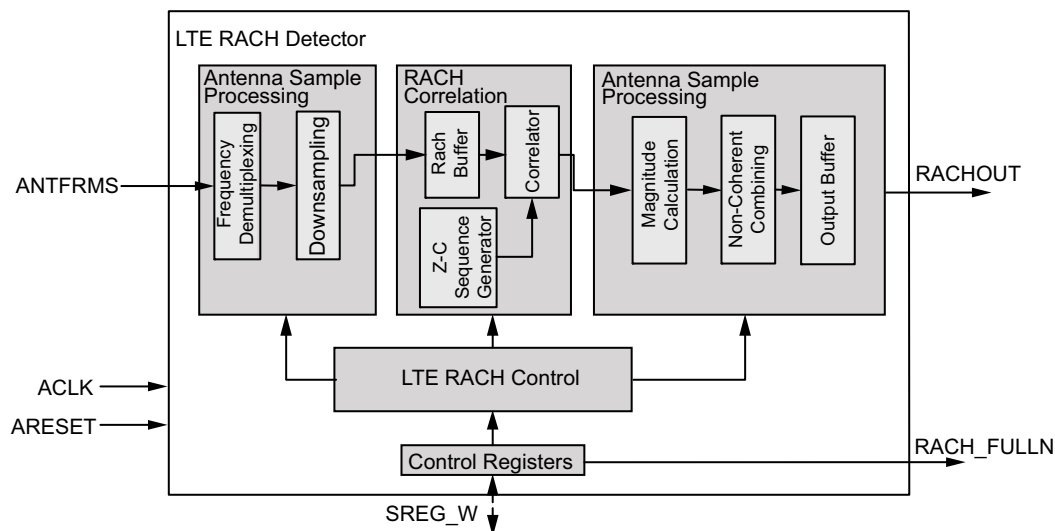


Figure 1: Internal Structure of the LTE RACH Detector Core

Technical Support

Xilinx provides technical support at the [Xilinx Support web page](#) for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the [Xilinx Support web page](#).

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the [Xilinx Core License Agreement](#). The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your [local Xilinx sales representative](#) for information about pricing and availability.

For more information, visit the LTE RACH Detector [product page](#).

Information about other Xilinx LogiCORE IP modules is available at the [Xilinx Intellectual Property](#) page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your [local Xilinx sales representative](#).

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
10/05/2016	2.0	Aligned to Product Guide update.
11/18/2015	2.0	Added support for UltraScale+ families.
06/04/2014	2.0	Initial Xilinx release. This document replaces XMP041.

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