# LTE UL Channel Decoder v2.0

XMP024 June 24, 2009 **Product Brief**

## Introduction

The Xilinx® LTE UL Channel Decoder core provides designers with an LTE Uplink Channel Decoding block for the *3GPP TS 36.212 v8.5.0 Multiplexing and Channel Coding* specification.

## Features

- Available for Virtex®-6, Virtex-5, Virtex-4 and Spartan®-6 FPGAs
- Channel decoding for 3GPP TS 36.212 supports UL-SCH and UL-CCH
- Bit-accurate C model available for the core
- Fully optimized for speed and area
- Fully synchronous design using a single clock
- For use with the Xilinx CORE Generator™ software v11.2 and higher
- New Features - PUCCH Chain, PUSCH Channel Interleaver, PUSCH CQI Channel, PUSCH ACK Channel and PUSCH RI Channel.

## Overview

The LTE UL Channel Decoder core provides a channel decoding solution for the 3GPP 36.212 specification. Figure 1 illustrates the main blocks in the LTE uplink decoding chain for the UL-SCH channel type that is supported by the core. Figure 2 illustrates the main blocks in the LTE uplink decoding chain for the UL-CCH channel type that is supported by the core.

The architecture has been designed to provide efficient use of the FPGA and offers a low bandwidth interface to an external processor to reduce processor-to-core interaction overhead. All processing intensive and timing critical operations are performed by the FPGA.

The interface to the core can be easily attached to any bus-based system. The memory mapped interface allows for simple integration and validation within the system.

Specific processing is applied on the input block, which is indicated as part of the control signaling provided by the MAC layer.

The following functions are supported by the core:

- Transport Block-based configuration on a channel basis to minimize processor interaction
- Transport Block-based data transfer on a channel basis to minimize FPGA memory requirements while still minimizing processor interaction
- Code Block Reassembly Calculation - Internal calculation performed to determine the breakup of a transport block into code blocks based on configured TB size
- Redundancy Version Calculation - Offset start position calculation based on RV index configuration
- Rate De-matching - Applied on a code-block basis to UL-SCH Data and UL-SCH CQI channels. This function performs de-interleaving and matrix null removal based on the configured code block (CB) size according to the configuration parameters.
- Decoding - Turbo decoding applied to UL-SCH Data channel. Viterbi decoding applied to UL-SCH CQI channel. Block Decoding applied to UL-SCH CQI channel and UL-CCH UCI channel
- Reassembly - Code block reassembly applied to UL-SCH code blocks (that is, data which are turbo decoded) in creation of transport blocks with an additional 24-bit CRC check performed on each code-block (in the cases where segmentation produces more than one code-block) and filler null removal of first CB of TB.
- CRC - 24-bit CRC checking applied to UL-SCH transport blocks. 8-Bit CRC checking applied to UL-SCH CQI blocks. Parity checking applied to ACK and RI 2-bit blocks
- HARQ - HARQ support on UL-SCH Data Blocks. Combined HARQ Data provided with a Block Identifier to ensure block synchronization.
- Scalable performance of Turbo Decoder and Block Decoder functions.

## UL-SCH Channel Processing

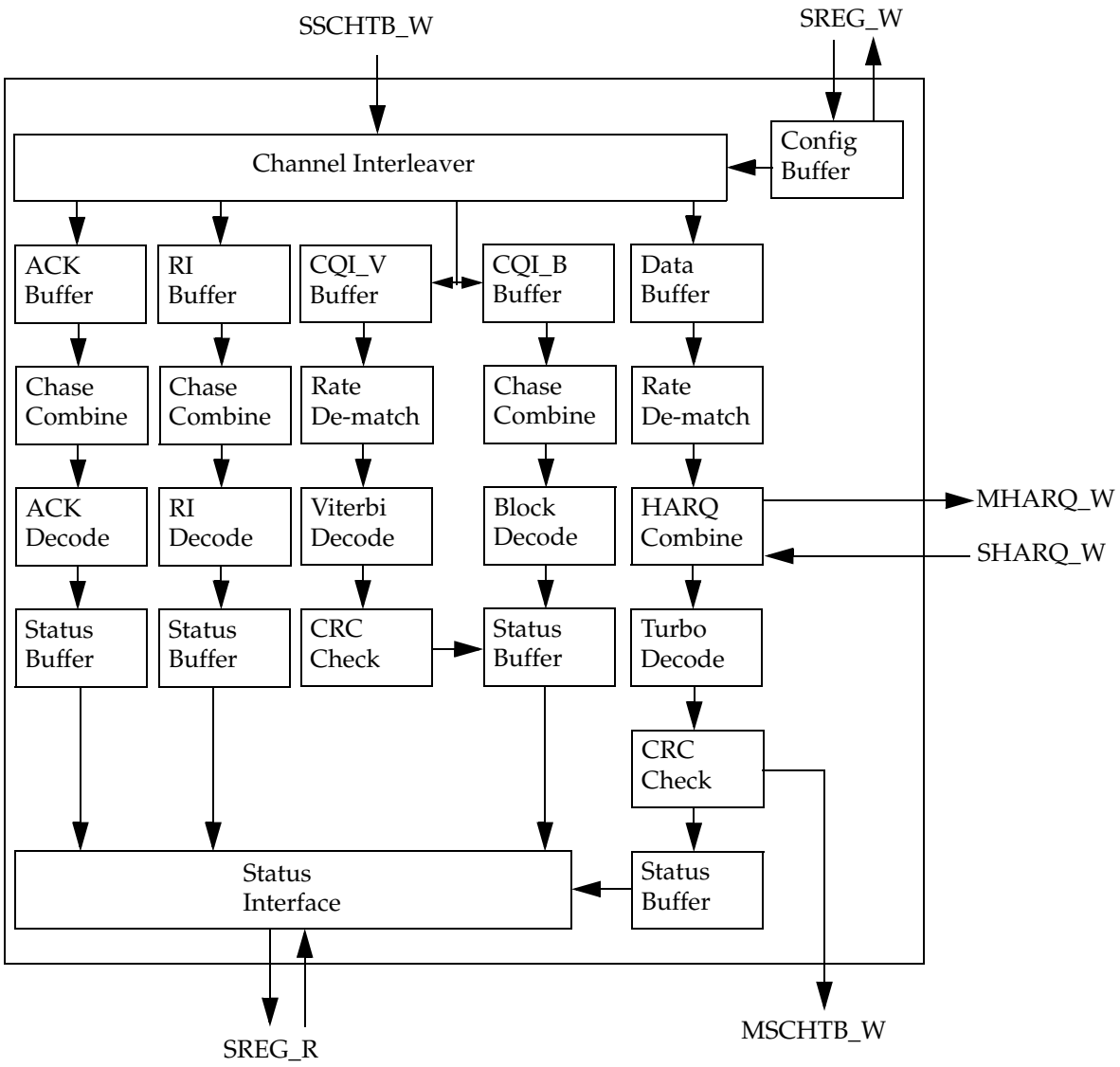


*Figure 1:* **Uplink Channel Decoder for SCH Channel**

## UL-CCH Channel Processing

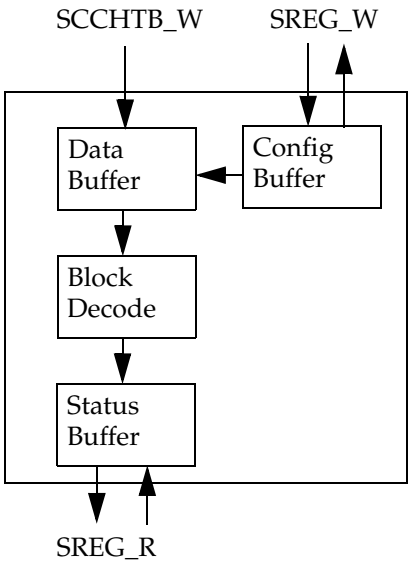


*Figure 2:* **Uplink Channel Decoder for CCH Channel**

# Ordering Information

The LTE UL Channel Decoder core is provided under the SignOnce IP Site License and can be generated using the Xilinx CORE Generator software v11.2 or higher. The CORE Generator software is shipped with Xilinx ISE® Foundation™ Series Development software.

To access the full functionality of the core, including simulation and FPGA bitstream generation, a full license must be obtained from Xilinx. For more information, visit the LTE UL Channel Decoder product page.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE™ IP modules and software. Information about additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

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## Abbreviations

For the purposes of this document, the following abbreviations apply:

| Acronym | Description |
|---|---|
| ACK | Acknowledgement |
| CB | Code Block |
| CCH | Control CHannel - UL-CCH |
| CQI | Channel Quality Indicator |
| HARQ | Hybrid Automatic Repeat reQuest |
| MHARQ_W | Master HARQ Write interface |
| MSCHTB_W | Master Shared CHannel Transport Block Write interface |
| RI | Rank Indicator |
| SCH | Shared CHannel - UL-SCH |
| SCCHTB_W | Slave Control CHannel Transport Block Write interface |
| SHARQ_W | Slave HARQ Write interface |
| SREG_R | Slave REGister Read interface |
| SREG_W | Slave REGister Write interface |
| SSCHTB_W | Slave Shared CHannel Transport Block Write interface |
| TB | Transport Block |
| UCI | Uplink Control Information |

## Revision History

| Date | Version | Revision |
|---|---|---|
| 09/19/08 | 1.0 | Xilinx initial release. |
| 06/24/09 | 2.0 | Updated to version 2 of the core. |

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