OPB Monitor BFM

DS130 (v2.0) April 30, 2004 **Product Overview**

Introduction

The CoreConnect Toolkit OPB Monitor Bus Functional Model is a simulation hardware component that connects to the OPB and continuously samples the bus signals.

The monitor checks for bus compliance or violations of the OPB architectural specifications and reports warnings and errors.

Features

- Xilinx OPB bus interface
- Checks for bus compliance or violations
- Reports warnings and errors
- Behavior configured in a Bus Functional Language (BFL) file

More Information

For detailed information on the IBM OPB Bus Functional Model Toolkit, you may register for the **CoreConnect Lounge** on the Xilinx web site to get access to the IBM CoreConnect documentation.

Core Facts

Core Specifics		
Supported Device Family	All	
Version of Core	opb_monitor_bfm	v1.00.a

Resources Used		
	Min	Max
I/O	N/A	N/A
LUTs	N/A	N/A
FFs	N/A	N/A
Block RAMs	N/A	N/A

Provided with Core	
Documentation	This document
Design File Formats	VHDL
Constraints File	N/A
Verification	N/A
Instantiation Template	N/A
Reference Designs	None

Design Tool Requirements	
Xilinx Implementation Tools	EDK 6.2 or later ISE 6.2 or later
Verification	N/A
Simulation	ModelSim SE/EE 5.6e or later
Synthesis	N/A

Support
Support provided by Xilinx, Inc.

Implementation

The OPB is a full-featured bus architecture with many features that increase bus performance. To obtain an efficient use of FPGA resource, Xilinx uses a subset of the OPB for Xilinx-developed OPB devices.

The CoreConnect OPB monitor model has an interface to a full-featured OPB bus. Xilinx has created an interface to the CoreConnect Toolkit components for them to be used within the Xilinx implementation of the OPB bus.

The CoreConnect OPB CoreConnect Toolkit contains standard Bus Functional Models and a Bus Functional Compiler for a rich Bus Functional Language specification. Xilinx utilizes these to provide the functionality and encapsulates the models around a customized interface that performs the translation between the two bus implementations domains. Figure 1 shows how this is done for the OPB monitor model.

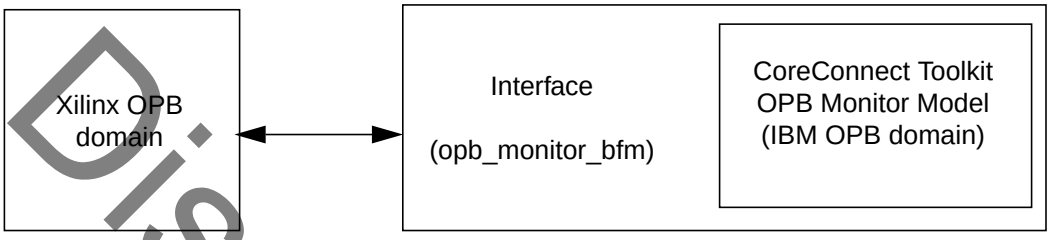

Figure 1: **Xilinx to IBM OPB domain interface**

MPD Parameters

The associated MPD (Microprocessor Peripheral Definition) file contains a list of the peripheral s parameters that are fixed at FPGA configuration time. The parameters are described in Table 1.

Table 1: **MPD Parameters**

Parameter	Description	Allowable Values	Type
NAME	Name	Any string	string
C_NUM_MASTERS	Number of Masters in the OPB bus	1-16	integer
C_NUM_SLAVES	Number of Slaves in the OPB bus	1-16	integer
C_OPB_DWIDTH	OPB bus width	32	integer

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
4/27/04	1.0	Initial Xilinx release