OPB Timebase WDT (v1.00a)

DS423 December 2, 2005 Product Specification

Introduction

This document describes the specifications for a 32-bit free-running timebase and watchdog timer core for the On-Chip Peripheral Bus (OPB). The TimeBase WatchDog Timer (TBWDT) is a 32-bit peripheral that attaches to the OPB.

Features

- OPB V2.0 bus interface with byte-enable support
- Supports 32-bit, 16-bit, and 8-bit bus interfaces
- Watchdog timer (WDT) with selectable timeout period and interrupt
- Configurable WDT enable: enable-once or enable-disable
- One 32-bit free-running timebase counter with rollover interrupt

Functional Description

The OPB Timebase WatchDog Timer (TBWDT) shown in Figure 1 consists of a free-running 32-bit timebase, read-only counter that always counts up from system reset. It is used for both general purpose timing and the WDT facility. The WDT timeout interval is determined by which bit in the timebase is used as input to the WDT state machine.

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	QPro™-R Virtex™-II, QPro Virtex-II, Spartan™-II, Spartan-IIE, Spartan-3, Spartan-3E, Virtex, Virtex-II, Virtex-II Pro, Virtex-4, Virtex-E	
Version of Core	opb_timebase_wdt	v1.00a
Resources Used		
	Min	Max
Slices	N/A	N/A
LUTs	63	63
FFs	111	111
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	5.1i or later	
Verification	N/A	
Simulation	ModelSim SE/EE 5.6e or later	
Synthesis	XST	
Support		
Support provided by Xilinx, Inc.		

The WDT uses a dual-expiration architecture. After one expiration of the timeout interval, an interrupt is generated and the WDT state bit is set to one in the status register. If the state bit is not cleared (by writing a 1 to the state bit) before the next expiration of the timeout interval, a WDT reset is generated. A WDT reset sets the WDT reset status bit in the status register so that the application code can determine if the last system reset was a WDT reset.

The WDT can only be disabled by writing to two distinct addresses, thereby reducing the possibly of inadvertently disabling the WDT in the application code.

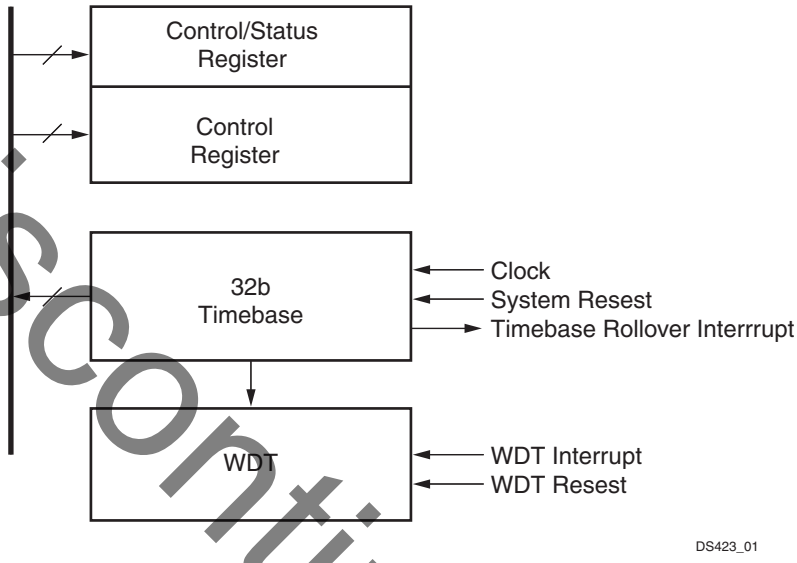

Figure 1: **OPB Timebase WDT Block Diagram**

The OPB Timebase WatchDog Timer has the following characteristics:

- Consists of a free-running 32-bit timebase counter that is used for both general purpose timing and the WDT facility
- The timebase counter always counts up from system reset and is read-only
- The WDT timeout interval is determined by which bit in the timebase is used as input to the WDT state machine
- The WDT uses a dual-expiration architecture. After one expiration of the timeout interval an interrupt is generated and the WDT state bit is set to one in the status register. If the state bit is not cleared (by writing a 1 to the state bit) before the next expiration of the timeout interval, a WDT reset is generated. A WDT reset sets the WDT reset status bit in the status register so that the application code can determine if the last system reset was a WDT reset.
- The WDT can only be disabled by writing to two distinct addresses, reducing the possibly of inadvertently disabling the WDT in the application code.

Operation

Timebase Operation

The timebase is a 32-bit up counter that is incremented by one on the rising edge of the clock provided to the TBWDT. This counter is reset to zero when the Reset input is high or when the WDT is enabled. The TBR contains the full timebase count value (32 bits).

The TWCSR0 contains the most-significant 28 bits of the timebase count, as well as the WDT enable and status bits. The timing resolution from the upper 28 bits of the timebase count is T_{clk} x 16 (T_{clk} is the period of the input clock). As a result, a single access can be used to read the state of the watchdog times, as well as a reduced resolution version of the timebase.

An interrupt signal is provided that pulses high for one clock period as the counter rolls over from 0xFFFFFFFF to 0x00000000. This interrupt can be used by the software to keep track of how many timebase rollovers have occurred.

WDT Operation

The WDT timeout interval is configured by a parameter to be 2^{WDT_CLOCKS} clock cycles, where WDT_CLOCKS is any integer from 8 to 31. The WDT interval is set at FPGA configuration time and cannot be modified dynamically through a control register.

The state of the WDT is given by the WDS bit in the TWCSR0 register. If the WDT interval expires while the WDS bit is 1, the WDT reset signal is asserted. An interrupt is provided when the WDS bit is set so that the software can clear the bit before the second expiration of the WDT. The WDS bit is cleared by writing a 1 to it. Writing a 0 to the WDS bit has no effect. The WDT state diagram is shown in Figure 2.

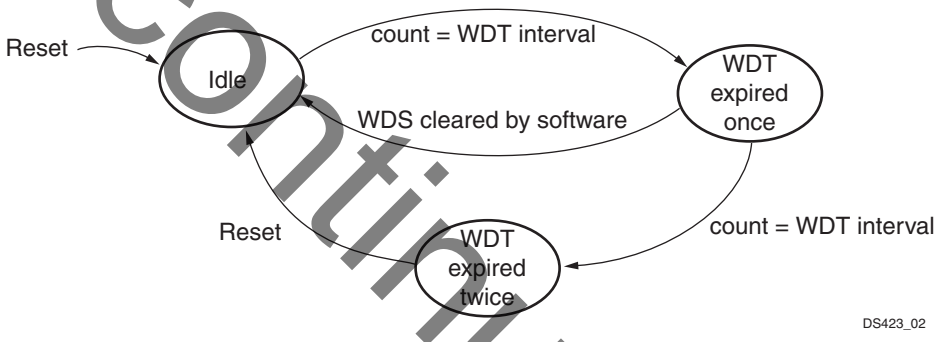

Figure 2: **WDT State Diagram**

I/O Signals

The TBWDT I/O signals are listed and described in Table 1.

Table 1: **Timebase WDT Core I/O Signals**

Signal	Interface	I/O	Description
OPB_Clk	OPB	I	OPB Clock
OPB_Rst	OPB	I	OPB Reset
OPB_ABus[0:31]	OPB	I	OPB Address Bus
OPB_BE[0:3]	OPB	I	OPB Byte Enables
OPB_DBus[0:31]	OPB	I	OPB Data Bus
OPB_RNW	OPB	I	OPB Read, Not Write
OPB_select	OPB	I	OPB Select
OPB_seqAddr	OPB	I	OPB Sequential Address
TBWDT_DBus[0:31]	OPB	O	TBWDT Data Bus

Table 1: **Timebase WDT Core I/O Signals *(Contd)***

Signal	Interface	I/O	Description
TBWDT_errAck	OPB	O	TBWDT Error Acknowledge
TBWDT_retry	OPB	O	TBWDT Retry
TBWDT_toutSup	OPB	O	TBWDT Timeout Suppress
TBWDT_xferAck	OPB	O	TBWDT Transfer Acknowledge
WDT_Reset	Ext.	O	Watchdog Timer Reset. Asserted upon second expiration of the WDT timeout interval. (Active High = "1")
Timebase_Interrupt	Ext.	O	Timebase Rollover Interrupt. Asserted as a one clock period wide pulse upon rollover of the timebase from 0xFFFFFFFF to 0x00000000.
WDT_Interrupt	Ext.	O	Watchdog Timer Interrupt. Goes high and stays high until the WDS bit is cleared in the TWCSR0 register.

Parameterization

The following characteristics of the TBWDT can be parameterized:

- Base address for the TBWDT registers
- Behavior of WDT enable: enable-once or enable-many
- WDT interval
- Future parameterization: Bus interface — 8-bit, 16-bit, or 32-bit. The internal architecture of the watchdog timer/WDT remains the same across bus interface sizes.

MPD File Parameters

The opb_timebase_wdt.mpd (Microprocessor Peripheral Definition) file contains a list of the parameters of the peripheral that are fixed at FPGA configuration time. The parameters are described in Table 2.

Table 2: **MPD Parameters**

Parameter	Description	Type
C_WDT_INTERVAL	Indicates the exponent for setting the length of the WDT interval. WDT interval = $2^{C\_WDT\_INTERVAL} \times T_{clk}$	integer
C_WDT_ENABLE_ONCE	Indicates WDT enable behavior. 0: WDT can be repeatedly enabled and disabled via software. 1: WDT can only be enabled once (no disable possible after initial enable).	integer
C_OPB_AWIDTH	The width of the address bus attached to the peripheral.	integer

Table 2: **MPD Parameters**

Parameter	Description	Type
C_OPB_DWIDTH	The width of the data bus attached to the peripheral.	integer
C_BASEADDR	Indicates the base address of this peripheral expressed as a std_logic_vector. C_BASEADDR must be a multiple of the range, where the range is C_HIGHADDR - C_BASEADDR +1.	std_logic_vector (0 to C_AWIDTH -1)
C_HIGHADDR	Indicates the highest address occupied by this peripheral expressed as a standard logic vector.	std_logic_vector (0 to C_AWIDTH -1)

Programming Models

Register Data Types and Organization

TBWDT registers are accessed as one of the following types:

- Byte (8 bits)
- Half word (2 bytes)
- Word (4 bytes)

Configuration

Table 3 shows TBWDT configurations and access type.

Table 3: **TBWDT Configuration and Access Type**

Configuration	Access Type
32-bit slave OPB peripheral	Word
16-bit peripheral	Half word
8-bit peripheral	Byte
32-bit, 16-bit, or 8-bit peripheral	All register accesses are on word boundaries to conform to the OPB-IPIF register location convention

Table 4 shows the addresses of the TBWDT registers when configured as a 32-bit OPB slave.

Table 4: **TBWDT Register Address Map**

Register	Address (Hex)	Size	Type	Description
TCSR0	0x00	Word	Read/Write	Control/Status Register 0
TCSR1	0x04	Word	Write	Control/Status Register 1 - state is mirrored in TCSR0 for read
TBR	0x08	Word	Read	Timebase Register

The TBWDT registers are organized as big-endian data. The bit and byte labeling for the big-endian data types is shown in Figure 3.

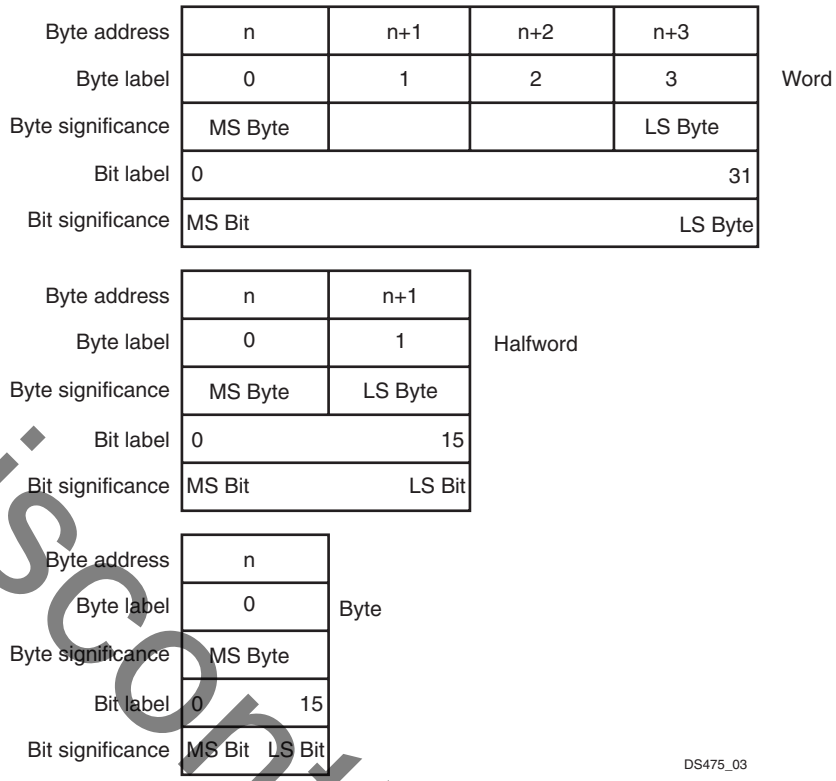

Figure 3: **Big-Endian Data Types**

Registers of the Timebase / Watchdog Timer

Registers used in assembly language programming are described in this section. The OPB Timebase WDT register set is shown in Figure 4.

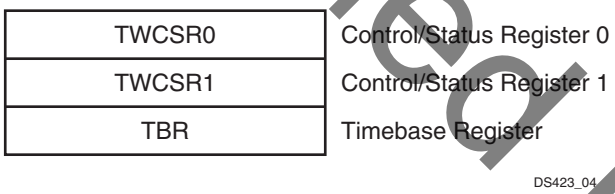

Figure 4: **TBWDT Register Set**

Address Map

Table 5: **TBWDT Register Address Map**

Register	Address (Hex)	Size	Type	Description
TCSR0	0x00	Word	Read/Write	Control/Status Register 0
TCSR1	0x04	Word	Write	Control/Status Register 1 - state is mirrored in TCSR0 for read
TBR	0x08	Word	Read	Timebase Register

Timebase Register (TBR)

The Timebase Register is the output of a free-running incrementing counter that clocks at the input clock rate (no prescaling of the clock is done for this counter). This register is read-only and is reset by the following:

- A system reset
- Enabling the WDT after power on reset
- Enabling the WDT after the WDT has been disabled (EWDT1 and EWDT2 must both be 0 to disable the WDT). The WDT is enabled when either EWDT1 or EWDT2 are set to 1. Note that when the WDT mode is enable-once, the TBR can only be reset when the WDT is first enabled.

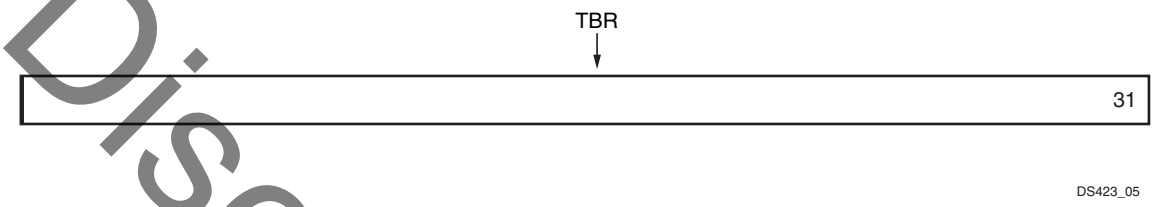

Figure 5: **Timebase Register (TBR)**

Control/Status Register 0 (TCSR0)

Control/Status Register 0 contains the watchdog timer reset status, watchdog timer state, and watchdog timer enables.

Figure 6: **Control/Status Register 0 (TCSR0)**

Table 6: **Control/Status Register 0 (TCSR0)**

Bits	Name	Description	Reset Value
0:27	TBR(0:27)	Timebase Register (Most significant 28 bits) This read-only field contains the most significant 28 bits of the timebase register. The timebase register is mirrored here so that a single read can be used to obtain the count value and the watchdog timer state if the upper 28 bits of the timebase provide sufficient timing resolution.	
28	WRS	Watchdog Reset Status Indicates the WDT reset signal was asserted. This bit is not cleared by a system reset so that it can be read after a system reset to determine if the reset was caused by a watchdog timeout. Writing a 1 to this bit clears the watchdog reset status bit. Writing a 0 to this bit has no effect. 0 WDT reset has not occurred 1 WDT reset has occurred	
29	WDS	Watchdog Timer State Indicates the WDT period has expired. The WDT_Reset signal will be asserted if the WDT period expires again before this bit is cleared by software. Writing a 1 to this bit clears the watchdog timer state. Writing a 0 to this bit has no effect. 0 WDT period has not expired 1 WDT period has expired, reset will occur on next expiration	
30	EWDT1	Enable Watchdog Timer (Enable 1) This bit must be used in conjunction with the EWDT2 bit in the TWCSR1 register. BOTH bits must be 0 to disable the WDT. 0 Disable WDT function 1 Enable WDT function	0
31	EWDT2	Enable Watchdog Timer (Enable 2) This bit must be used in conjunction with the EWDT1 bit in the TCSR0 register to disable the WDT. BOTH bits must be 0 to disable the WDT. This bit is READ-ONLY in this register. The value of EWDT2 can be modified only in TWCSR1. 0 WDT function is disabled 1 WDT function is enabled	0

Control/Status Register 1 (TCSR1)

Control/Status Register 1 contains the second Watch Dog Timer (WDT) enable bit.The WDT enable must be cleared in both TCSR0 and TCSR2 to disable the WDT. If the WDT is configured as enable-once, then the WDT cannot be disabled after it has been enabled.

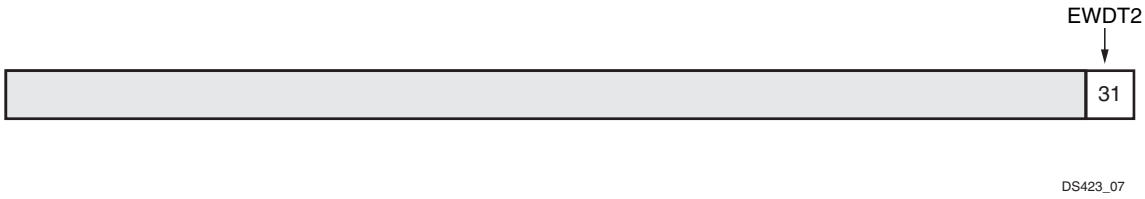

Figure 7: **Control/Status Register 1 (TCSR1)**

Table 7: **Control/Status Register 1 (TCSR1)**

Bits	Name	Description	Reset Value
0:30	Reserved		
31	EWDT2	Enable Watchdog Timer (Enable 2) This bit must be used in conjunction with the EWDT1 bit in the TCSR0 register to disable the WDT. BOTH bits must be 0 to disable the WDT. This bit is WRITE-ONLY in this register. The value of EWDT2 can be read back only in TWCSR1. 0 WDT function is disabled 1 WDT function is enabled	0

Device Utilization and Performance Benchmarks

The following table shows approximate resource utilization and performance benchmarks for the OPB Timer/Counter. The estimates shown are not guaranteed and can vary with FPGA family and speed grade, parameters selected for implementation, user timing constraints, and implementation tool version. Only parameters that affect resource utilization are shown in Table 8.

Table 8: **OPB Timebase/WDT Performance and Resource Utilization Benchmarks (Virtex-II 2V1000-5)**

Parameter Values		Device Resources			f_{MAX} (MHz)
Address Bits in Decode	C_AWIDTH	Slices	Slice Flip-Flops	4-input LUTs	f_{MAX}
24	32	111	63	155	

Revision History

Date	Version	Revision
05/25/01	1.0	Initial Xilinx release.
03/20/02	2.0	Updated for MDK 2.2
05/27/02	2.1	Update for EDK 1.0
07/23/02	2.2	Add XCO parameters for System Generator
01/08/03	2.3	Update for EDK SP3
07/14/03	2.4	Update table 6; update to new template
07/29/03	2.4.1	Change DS211 to DS423 because of duplications
09/24/03	2.4.2	Update trademarks
8/19/04	2.5	Updated for Gmm; updated trademarks and supported device family listing.
4/6/05	2.6	Updated for EDK 7.1.1 SP1.
9/27/05	2.7	Converted to new DS template; updated figures to Xilinx graphic standards; performed overall review.
12/2/05	2.8	Added Spartan-3E to supported device families listing.