LogiCORE IP Peak Cancellation Crest Factor Reduction v3.0

PB008 June 22, 2011 **Product Brief**

Introduction

Crest Factor Reduction (CFR) is used to limit the dynamic range of the signals being transmitted in Wireless Communications and other applications. Multi-user and multi-carrier signals often have a high peak-to-average ratio (PAR). This places high demands on the data converters and especially limits the efficiency of operation of the Power Amplifiers (PAs) used in cellular base stations. Reducing the PAR is therefore beneficial in increasing PA efficiency by allowing higher average power to be transmitted before saturation occurs.

Features

- Multiple air interface standards supported - MC-GSM, WCDMA, TD-SCDMA, WiMAX, LTE, CDMA2000, Mixed mode (for example, GSM + LTE, TD-SCDMA + LTE, WCDMA + LTE)
- Tx BW support of up to 145 MHz
- Various multi-carrier configurations supported
- Meets performance requirements (EVM, PAPR and ACLR) of all air interfaces
- Configurable clock-to-sample ratio of 1 to 4 for resource optimization
- Configurable number of Cancellation Pulse Generators (CPGs) of 1 to 8 per iteration
- Multiple antenna support for 1, 2, 4 and 8 antennas
- Multiple iteration support for 1 to 8 iterations
- Variable quantization support for 11 to 18 bits
- Configurable latency support for 66 to 10106 samples
- User-selectable cancellation pulse loading mode: single-pulse fixed coefficients, single-pulse configurable coefficients, two-pulses configurable coefficients
- Cancellation pulse read back support (in configurable coefficients modes only)
- AXI4-Stream compliant for data interface and AXI4-Lite compliant for control interface
- MATLAB® simulator available for system-level verification
- Bit accurate C model available

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Virtex-7, Kintex-7, Artix-7, Zynq-7000, Virtex-6, Spartan-6
Supported User Interfaces	AXI4-Stream, AXI4-Lite
Provided with Core	
Documentation	Product Brief Product Specification C Model User Guide
Design Files	Netlist
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided
Simulation Model	Verilog, VHDL, C Model and MATLAB Model
Tested Design Tools	
Design Entry Tools	CORE Generator 13.2
Simulation(2)	Mentor Graphics ModelSim ISim
Synthesis Tools	XST 13.2
Support	
Provided by Xilinx, Inc.	

1. For a complete listing of supported devices, see the release notes for this core.
2. For the supported version of the tools, see the ISE Design Suite 13: Release Notes Guide

Overview

Crest Factor Reduction (CFR) is used to limit the dynamic range of the signals being transmitted in Wireless Communications and other applications. Multi-user and multi-carrier signals often have a high peak-to-average ratio (PAR). This places high demands on the data converters and especially limits the efficiency of operation of the Power Amplifiers (PAs) used in cellular base stations. Reducing the PAR is therefore beneficial in increasing PA efficiency by allowing higher average power to be transmitted before saturation occurs.

In a modern transmit chain, CFR is also often incorporated with Digital Predistortion (DPD), which acts to linearize the PA, allowing operation at maximum efficiency with spectral compliance. CFR is helpful to DPD because it levels the signal peaks, making accurate correction estimation easier [Ref 1].

The Xilinx® PC-CFR core is an efficient, flexible and easy-to-use implementation that supports Virtex®-7, Kintex™-7, Artix™-7, Zynq™-7000, Virtex-6, and Spartan®-6 FPGA families. It is configurable both in function, to support all major cellular wireless air interfaces, and in usage, to support a variety of clocking and resource requirements.

Features and General Description

The Peak Cancellation-CFR core processes control and data through industry-standard AXI4 interfaces that allow immediate logic-free connection to other Xilinx IP components and to any general environment. The control interface is AXI4-Lite compliant and the data interface is AXI4-Stream compliant. The control interface provides access to a set of configuration registers and a pulse coefficient RAM and the data interface is used for streaming data in/out of the core. The data flow is unidirectional with no rate or bit-width change. A typical CFR application consists of multiple iterations and multiple antennas that can be configured through the GUI. The core is configured for a particular application through the control interface. In particular, the contents of the pulse coefficient RAM are related to the spectrum of the signal being transmitted. In the product data sheet (DS846) it is shown how to produce these coefficients, and specific details are given for the WCDMA, CDMA2000, WiMAX, TD-SCDMA, GSM and E-UTRAN (LTE) air interfaces. Mixed-mode signal operation is also supported. Pulse coefficients can be pre-configured at generation time through a .coe file or configured in operation via the control interface. There is also provision for a shadow bank of coefficients to be loaded, and then activated with a select signal, to cater to applications where fast dynamic switching is required. Functions that can be run with MATLAB® are supplied for simulation and design of the cancellation pulse.

The core can be configured for clock-to-sample ratios between 1 and 4, and for algorithmic complexity, allowing FPGA fabric resources to be minimized for a given application. The algorithmic complexity is the number of hardware resources available to cancel the signal peaks. These are called Cancellation Pulse Generators.

Resource Requirements and Performance

This section provides data on the resource requirements and performance of the core. Characterization has been done on Virtex-7, Kintex-7, Virtex-6, and Spartan-6 FPGAs. Table 1 lists the devices used for characterization.

Table 1: **Devices Used for Characterization**

Virtex-7	Kintex-7	Virtex-6	Spartan-6
xc7v585t-1	xc7k325t-1	xc6vlx130t-1	xc6slx100-2

Resource requirements and performance are dependent mainly on the Data-Rate, Number of Cancellation Pulse Generators per Iteration, Number of Antennas, Number of Iterations and Max Cancellation Pulse Length. They are also susceptible to the version of implementation tools used. Therefore, these example figures should be used as a

guide only and verified before specific use. Maximum clock frequencies quoted do not take clock jitter into account and should be derated by an amount appropriate to the clock source jitter specification.

Table 2 to 5 provide resource requirements and performance for the Virtex-7, Kintex-7, Virtex-6 and Spartan-6 FPGA families respectively. For all configurations, the default datawidth of 16 bits has been used with the coefficient setup selected as 'Single pulse configurable coefficients'.

Table 2: **Virtex-7 Resource Requirements and Performance**

Antennas	Iterations	Data-Rate (clks/sample)	CPGs/ Iteration	Max CP Length	Block RAMs (36k/18k)	DSP48s	Slices	LUT/FF	F_{max} (MHz)
1	1	1	4	511	4/3	18	845	1860/2198	390
1	1	2	4	511	2/3	10	796	1557/1850	380
1	1	3	6	511	2/3	10	797	1788/2006	400
1	1	4	4	511	1/3	6	690	1427/1681	360
1	1	4	4	1023	2/2	6	811	1401/1697	390
1	1	4	4	2047	4/2	6	702	1411/1715	380
2	2	3	6,3	511	6/12	32	2622	6077/6631	400
2	4	3	6,6,3,3	511	12/24	64	4956	12010/12877	350
4	2	3	6,3	511	12/24	64	5329	12190/13124	380
4	4	3	6,6,3,3	511	24/48	128	9766	23966/25621	320
8	2	3	6,3	511	24/48	128	10384	22664/26109	320
8	4	3	6,6,3,3	511	48/96	256	20275	44808/51103	300

Table 3: **Kintex-7 Resource Requirements and Performance**

Antennas	Iterations	Data-Rate (clks/sample)	CPGs/ Iteration	Max CP Length	Block RAMs (36k/18k)	DSP48s	Slices	LUT/FF	F_{max} (MHz)
1	1	1	4	511	4/3	18	843	1822/2198	350
1	1	2	4	511	2/3	10	734	1573/1850	370
1	1	3	6	511	2/3	10	920	1766/2006	380
1	1	4	4	511	1/3	6	691	1465/1681	390
1	1	4	4	1023	2/2	6	699	1420/1697	390
1	1	4	4	2047	4/2	6	698	1426/1715	390
2	2	3	6,3	511	6/12	32	2470	6128/6632	400
2	4	3	6,6,3,3	511	12/24	64	4651	12065/12877	370
4	2	3	6,3	511	12/24	64	4889	12293/13124	350
4	4	3	6,6,3,3	511	24/48	128	8054	24044/25621	370
8	2	3	6,3	511	24/48	128	9984	22702/26109	350
8	4	3	6,6,3,3	511	48/96	256	18793	44852/51103	310

Table 4: **Virtex-6 Resource Requirements and Performance**

Antennas	Iterations	Data-Rate (clks/sample)	CPGs/ Iteration	Max CP Length	Block RAMs (36k/18k)	DSP48s	Slices	LUT/FF	F_{max} (MHz)
1	1	1	4	511	4/3	18	802	1808/2189	400
1	1	2	4	511	2/3	10	704	1563/1825	400
1	1	3	6	511	2/3	10	857	1793/1965	400
1	1	4	4	511	1/3	6	634	1466/1649	400
1	1	4	4	1023	2/2	6	631	1398/1665	400
1	1	4	4	2047	4/2	6	683	1684/2171	400
2	2	3	6,3	511	6/12	32	2529	6098/6514	400
2	4	3	6,6,3,3	511	12/24	64	3935	12007/12636	350
4	2	3	6,3	511	12/24	64	4546	12171/12959	370
4	4	3	6,6,3,3	511	24/48	128	8928	24045/25198	360
8	2	3	6,3	511	24/48	128	9919	22655/25621	370
8	4	3	6,6,3,3	511	48/96	256	16445	45040/50110	330

Table 5: **Spartan-6 Resource Requirements and Performance**

Antennas	Iterations	Data-Rate (clks/sample)	CPGs/ Iteration	Max CP Length	Block RAMs (18k/9k)	DSP48s	Slices	LUT/FF	F_{max} (MHz)
1	1	1	4	511	6/1	18	783	1855/2247	250
1	1	2	4	511	4/1	10	709	1569/1900	250
1	1	3	6	511	4/1	10	782	1794/2042	250
1	1	4	4	511	3/1	6	710	1419/1721	250
1	1	4	4	1023	5/1	6	697	1426/1765	240
1	1	4	4	2047	9/1	6	728	1418/1780	230
2	2	1	4,4	511	24/4	72	2936	7223/8516	240
2	4	2	4,4,4,4	511	32/8	80	5070	11878/13707	200
4	2	2	4,4	511	32/8	80	6089	11005/14133	200
4	4	4	4,4,4,4	511	48/16	96	9838	19627/63288	200

References

1. Xilinx Application Note, XAPP1128, “Digital Predistortion v2.0”

Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

See the *IP Release Notes Guide* (XTP025) for further information on this core. There is a link to *All DSP IP* and then to the relevant core.

For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core Site License and the core is generated using the Xilinx ISE® CORE Generator™ software. The CORE Generator software is shipped with the Xilinx ISE Design Suite software.

For full access to all core functionality in simulation and in hardware, you must purchase a license for the core. Contact your local Xilinx sales representative for information on pricing and availability of Xilinx LogiCORE IP modules. Information about additional modules is also available at the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/22/11	1.0	Initial Xilinx release. Previous version of this Product Brief is XMP039.

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