

Introduction

Crest Factor Reduction (CFR) is used to limit the dynamic range of the signals being transmitted in Wireless Communications and other applications.

Additional Documentation

A product guide is available for this core. Access to this material may be requested by clicking on this registration link:

www.xilinx.com/member/pc_cfr_eval/index.htm.

Features

- Multiple air interface standards supported - MC-GSM, WCDMA, TD-SCDMA, WiMAX, LTE, CDMA2000, Mixed mode (GSM + LTE, TD-SCDMA + LTE, WCDMA + LTE)
- TX BW support of up to 145 MHz
- Dynamic Cancellation Pulse (CP) computation mode to support dynamic power and frequency variations
- Meets performance requirements (EVM, PAPR and ACLR) of all air interfaces
- Configurable clock-to-sample ratio
- Configurable number of Cancellation Pulse Generators (CPGs) of 1 to 12 per iteration
- Support for 1, 2, 4 and 8 antennas
- Iteration support for 1 to 8 iterations
- Variable quantization support for 11 to 18 bits
- Configurable latency support
- User-selectable cancellation pulse loading mode
- Cancellation pulse read back support

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family ⁽¹⁾	Zynq® -7000, 7 Series
Supported User Interfaces	AXI4-Stream, AXI4-Lite
Resources	See Table 1
Provided with Core	
Design Files	Encrypted RTL
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Vivado: XDC
Simulation Model	VHDL and Verilog Structural Simulation Model C Model and MATLAB® Model
Supported S/W Driver	N/A
Tested Design Flows⁽²⁾	
Design Entry	Vivado® Design Suite IP Integrator
Simulation	For supported simulators, see the Xilinx Design Tools: Release Notes Guide .
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx @ www.xilinx.com/support	

Notes:

1. For a complete listing of supported devices, see the Vivado IP catalog.
2. For the supported versions of the tools, see the [Xilinx Design Tools: Release Notes Guide](#).

Overview

Crest Factor Reduction (CFR) is used to limit the dynamic range of the signals being transmitted in Wireless Communications and other applications. Multi-user and multi-carrier signals often have a high peak-to-average ratio (PAR). This places high demands on the data converters and especially limits the efficiency of operation of the Power Amplifiers (PAs) used in cellular base stations. Reducing the PAR is therefore beneficial in increasing PA efficiency by allowing higher average power to be transmitted before saturation occurs.

In a modern transmit chain, CFR is often incorporated with Digital Pre-distortion (DPD), which acts to linearize the PA, allowing operation at maximum efficiency with spectral compliance. CFR complements DPD because it levels the signal peaks, making accurate correction estimation easier.

The Xilinx Peak Cancellation -CFR (PC-CFR) core is an efficient, flexible and easy-to-use implementation that supports Virtex[®]-7, Kintex[®]-7, Artix[®]-7, and Zynq-7000 FPGA families. It is configurable both in function, supporting all major cellular wireless air interfaces, and in use, supporting many clocking and resource requirements. It can also handle dynamic power and frequency variations in the incoming data by computing the cancellation pulse coefficients dynamically.

Features and General Description

The PC-CFR core processes control and data through industry-standard AXI4 interfaces that allow immediate logic-free connection to other Xilinx IP components and to any general environment. The control interface is AXI4-Lite compliant and the data interface is AXI4-Stream compliant. The control interface provides access to a set of configuration registers and a pulse coefficient RAM and the data interface is used for streaming data in/out of the core. The data flow is unidirectional with no rate or bit-width change. A typical CFR application consists of multiple iterations and multiple antennas that can be configured through the Vivado Integrated Design Environment (IDE). The core is configured for a particular application through the control interface. In particular, the contents of the pulse coefficient RAM are related to the spectrum of the signal being transmitted. In the *PC-CFR Product Guide* (PG097) it is shown how to produce these coefficients, and specific details are given for the WCDMA, CDMA2000, WiMAX, TD-SCDMA, GSM and E-UTRAN (LTE) air interfaces. Mixed-mode signal operation is also supported. Pulse coefficients can be pre-configured at generation time through a .coe file or configured in operation through the control interface. There is also provision for a shadow bank of coefficients to be loaded, and then activated with a select signal, to cater to applications where fast dynamic switching is required. Functions that can be run with MATLAB[®] are supplied for simulation and design of the cancellation pulse.

The core can be configured for clock-to-sample ratios between 1 and 4, and for algorithmic complexity, allowing FPGA resources to be minimized for a given application. The algorithmic complexity is the number of hardware resources available to cancel the signal peaks. These are called Cancellation Pulse Generators.

Resource Requirements and Performance

This section provides data on the resource requirements and performance of the core. Characterization has been done on Virtex-7 and Kintex-7 FPGAs. Resource requirements and performance are dependent mainly on the Data Rate, Number of Cancellation Pulse Generators per Iteration, Number of Antennas, Number of Iterations and Max Cancellation Pulse Length. They are also susceptible to the version of implementation tools used. Therefore, these example figures should be used as a guide only and verified before specific use. Maximum clock frequencies quoted do not take clock jitter into account and should be derated by an amount appropriate to the clock source jitter specification.

Table 1 provides resource requirements and performance for the Virtex-7 and Kintex-7 FPGA families. Resource figures for other configurations can be found in the PC-CFR Product Guide (see [Additional Documentation](#)). For all configurations, a default data width of 16 is used. All Static mode configurations are used with Coefficient Selection selected as "Single pulse configurable coefficients" in the Vivado IDE.

Table 1: Device Utilization for Kintex-7, Virtex-7 and Artix-7

Antennas	Iterations	Data-Rate (clks/sample)	CPGs/ Iteration	Max CP Length	CP Coeff (0-Real, 1-Cmplx)	HARD CLIPPER (1-Enable, 0 Disable)	MODE (1 Dynamic, 0-Static)	CP Compute (1-Fast, 0-Slow)	Block RAMs (36k/18k)	DSP48s	Slices	LUT/FF	F _{max} (MHz)
Kintex-7 (XC7K325T-2FBG676)													
4	4	3	6,6,3,3	511	1	0	0	NA	24 36	128	13368	27149 46552	495
8	2	3	6,3	511	1	0	0	NA	24 40	128	13757	27490 47297	505
Kintex-7 (XC7K325T-1FBG676)													
2	2	3	6,3	511	1	0	0	NA	6 10	32	3571	6980 11942	450
2	4	3	6,6,3,3	511	1	0	0	NA	12 18	64	6875	13655 23332	440
Virtex-7 (XC7V585T-2FFG1157)													
4	4	3	6,6,3,3	511	1	0	0	NA	24 36	128	13174	27149 46552	495
8	2	3	6,3	511	1	0	0	NA	24 40	128	13495	27476 47297	505
Virtex-7 (XC7V585T-1FFG1157)													
2	2	3	6,3	511	1	0	0	NA	6 10	32	3547	6978 11942	450
2	4	3	6,6,3,3	511	1	0	0	NA	12 18	64	7066	13658 23332	435
Artix-7 (XC7A200T-2FBG676)													
1	1	1	4	511	0	0	0	NA	0 6	10	1073	1552 3601	400
2	2	3	6,3	511	0	0	0	NA	0 16	20	3189	6253 10502	345

Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled DO NOT MODIFY.

Licensing and Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the [Xilinx Core License Agreement](#). The module is shipped as part of the Vivado Design Suite. For full access to all core functionalities in simulation and in hardware, you must purchase a license for the core. Contact your [local Xilinx sales representative](#) for information about pricing and availability.

For more information, visit the PC-CFR [product web page](#).

Information about other Xilinx LogiCORE IP modules is available at the [Xilinx Intellectual Property](#) page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your [local Xilinx sales representative](#).

Evaluation

An evaluation license is available for this core. The evaluation version operates in the same way as the full version for several hours, dependant on clock frequency. Allocation of the cancellation pulse generators is then completely disabled, and the data output comprises a delayed version of the data input. If you notice this behavior in hardware, it probably means you are using an evaluation version of the core. The Xilinx tools warn that an evaluation license is being used during netlist implementation. If a full license is installed, delete the old XCO file, reconfigure and regenerate the core.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
06/22/2011	1.0	Initial Xilinx release. Previous version of this Product Brief is XMP039.
12/18/2012	2.0	Updated for 2012.4/14.4. <ul style="list-style-type: none"> • Real/Complex CP selection added • Number of CPGs/iteration increased to 12 • Core is fully supported in Vivado 2012.4 • Peak detect window is used in place of allocator spacing
03/20/2013	3.0	PC-CFR v4.0 is available only with Vivado; other changes are <ul style="list-style-type: none"> • Improved f_{max}, core can be clocked at 491.52 MHz for -2 devices • Core latency has changed
12/18/2013	5.0	<ul style="list-style-type: none"> • Revision number advanced to 5.0 to align with core version number. • Added dynamic support (dynamic power variation and frequency hopping) • Hard clipper support • Change in tool settings for characterization • New TUSER port added in Dynamic mode

Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at <http://www.xilinx.com/warranty.htm>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: <http://www.xilinx.com/warranty.htm#critapps>.