LogiCORE IP Peak Cancellation Crest Factor Reduction v2.0

XMP039 December 2, 2009 **Product Brief**

Introduction

Crest Factor Reduction (CFR) is used to limit the dynamic range of the signals being transmitted in Wireless Communications and other applications. Multi-user and multi-carrier signals often have a high peak-to-average ratio (PAR). This places high demands on the data converters and especially limits the efficiency of operation of the Power Amplifiers (PAs) used in cellular base stations. Reducing the PAR is therefore beneficial in increasing PA efficiency by allowing higher average power to be transmitted before saturation occurs.

In a modern transmit chain, CFR is also often incorporated with Digital Predistortion (DPD), which acts to linearize the PA, allowing operation at maximum efficiency with spectral compliance. CFR is helpful to DPD because it levels the signal peaks, making accurate correction estimation easier [Ref 1].

The Xilinx PC-CFR core is an efficient, flexible and easy-to-use implementation that supports Virtex®-5, Virtex-6, and Spartan®-6 FPGA families. It is configurable both in function, to support all major cellular wireless air interfaces, and in usage, to support a variety of clocking and resource requirements.

Features and General Description

The Peak Cancellation-CFR core processes control and data through standardized interfaces that allow immediate logic-free connection to other Xilinx IP components and, through simple rules, to any general environment. The data flow is unidirectional with no rate or bit-width change. The control interface consists of constant parallel register inputs and an optional memory-mapped interface to a pulse coefficient RAM. A typical CFR application consists of more that one instance of the core chained in series and in parallel (where multiple transmit paths are to be serviced). The core is configured for a particular application through the control interfaces. In particular, the contents of the pulse coefficient RAM are related to the spectrum of the signal being transmitted. In the product data sheet it is shown how to produce these coefficients for the WCDMA, CDMA2000, WiMAX, TD-SCDMA, GSM and E-UTRAN (LTE) air interfaces. Mixed-mode signal operation is also supported. Pulse coefficients may be pre-configured at generation time through a .coe file or configured in operation via the control interface. There is also provision for a shadow bank of coefficients to be loaded, then and activated with an immediate signal, to cater to applications where fast dynamic switching is required. Functions that can be run with MATLAB® are supplied for simulation and design of the cancellation pulse.

The core may be configured for clock-to-sample ratios between 1 and 8, and for algorithmic complexity, allowing FPGA fabric resources to be minimized for a given application. The algorithmic complexity is the number of hardware resources available to cancel the signal peaks. These are called Cancellation Pulse Generators.

Resource Requirements and Performance

Resource requirements and performance are dependent mainly on the Data-Rate and Number of Cancellation Pulse Generators used in the configuration. They are also susceptible to the version of implementation tools used. Therefore, these example figures should be used as a guide only and verified before specific use. Maximum clock frequencies quoted do not take clock jitter into account and should be derated by an amount appropriate to the clock source jitter specification.

Table 1, Table 2 and Table 3 provide resource requirements and performance for the families Virtex-5, Spartan-6 and Virtex-6 respectively. For all configurations, the default data width of 16 bits has been used with the coefficient setup selected as 'Single pulse configurable coefficients.'

Table 1: **Virtex-5 Resource Requirements and Performance**

Device	Data-Rate (clks/sample)	Pulse Generators	Block RAM (36k/18k)	DSP48s	LUT/FF Pairs	LUT/FF	Max. Freq. (MHz)
xc5vlx110-1	1	4	0/7	18	2040	1310/1913	335
xc5vlx110-1	2	4	0/5	10	1646	1092/1542	403
xc5vlx110-1	3	3	0/4	6	1402	947/1312	388
xc5vlx110-1	4	4	0/4	6	1466	971/1372	387
xc5vlx110-1	8	8	0/4	6	1696	1103/1614	387

Table 2: **Spartan-6 Resource Requirements and Performance**

Device	Data-Rate (clks/sample)	Pulse Generators	Block RAM (16k/8k)	DSP48s	LUT/FF Pairs	LUT/FF	Max. Freq. (MHz)
xc6slx100-2	1	4	6/1	18	1690	1686/1910	193
xc6slx100-2	2	4	4/1	10	1355	1345/1539	198
xc6slx100-2	3	3	3/1	6	1238	1217/1310	206
xc6slx100-2	4	4	3/1	6	1212	1201/1369	196
xc6slx100-2	8	8	3/1	6	1431	1424/1607	189

Table 3: **Virtex-6 Resource Requirements and Performance**

Device	Data-Rate (clks/sample)	Pulse Generators	Block RAM (36k/18k)	DSP48s	LUT/FF Pairs	LUT/FF	Max. Freq. (MHz)
xc6vlx130t-1	1	4	4/3	18	1737	1733/1914	400
xc6vlx130t-1	2	4	2/3	10	1363	1360/1542	400
xc6vlx130t-1	3	3	1/3	6	1187	1175/1312	400
xc6vlx130t-1	4	4	1/3	6	1245	1235/1372	400
xc6vlx130t-1	8	8	1/3	6	1522	1503/1614	400

Note: The size and performance of the core depend on the specific customer application and the tool version used. These sizes and clock rates are obtained with a single core placed in an otherwise empty Xilinx FPGA and should be used as a guide only.

References

1. XAPP1128, “Digital Predistortion v2.0”

Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Refer to the *IP Release Notes Guide* (XTP025) for further information on this core. There will be a link to all the DSP IP and then to the relevant core being designed with.

For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

Ordering Information

This Xilinx LogiCORE IP module is provided under the terms of the Xilinx Core Site License and the core is generated using the Xilinx ISE® CORE Generator software. The CORE Generator software is shipped with the Xilinx ISE Design Suite software.

For full access to all core functionality in simulation and in hardware, you must purchase a license for the core. Please contact your local Xilinx sales representative for information on pricing and availability of Xilinx LogiCORE IP modules. Information about additional modules is also available at the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/02/09	1.0	Initial Xilinx release.

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