PLB to FSL Bridge v1.00a

Introduction

The PLB to FSL Bridge can be used to provide FSL interface connection to any PLB v4.6 master. Both FSL master and slave interfaces are available for bi-directional transfer of data.

Features

- PLB interface is based on PLB v4.6 specification
- FSL interface is based on FSL v2.0 specification

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Spartan™-3E, Spartan-3, Spartan-3A, Spartan-3AN, Spartan-3A DSP, Virtex™-4, Virtex-5, Virtex-II and Virtex-II Pro	
Version of core	plb2fsl_bridge	v1.00a
Resources Used[1]		
	Min	Max
Slices	~90	~90
LUTs	~85	~89
FFs	~125	~125
Block RAMs	0	0
Special Features	None	
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs & application notes	N/A	
Additional Items	N/A	
Design Tool Requirements		
Xilinx Implementation Tools	ISE 9.2i or later	
Verification	ModelSim SE/EE 6.0c or later	
Simulation	ModelSim SE/EE 6.0c or later	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

1. Resources for Virtex-4 implementation.

Functional Description

The PLB to FSL Bridge translates PLB accesses to FSL master and slave requests.

PLB to FSL Bridge I/O Signals

The PLB to Bridge FSL I/O signals are listed and described in Table 1.

Table 1: **PLB to FSL Bridge I/O Signal Description**

Port	Signal Name	Interface	I/O	Initial State	Description
System Signals					
P1	SPLB_Clk	System	I	-	PLB clock
P2	SPLB_Rst	System	I	-	PLB reset, active high
PLB Interface Signals					
P3	PLB_ABus[0:31]	PLB	I	-	PLB address bus
P4	PLB_PAValid	PLB	I	-	PLB primary address valid
P5	PLB_masterID[0: C_SPLB_MID_WIDTH - 1]	PLB	I	-	PLB current master identifier
P6	PLB_RNW	PLB	I	-	PLB read not write
P7	PLB_BE[0: (C_SPLB_DWIDTH/8) - 1]	PLB	I	-	PLB byte enables
P8	PLB_size[0:3]	PLB	I	-	PLB size of requested transfer
P9	PLB_type[0:2]	PLB	I	-	PLB transfer type
P10	PLB_wrDBus[0: C_SPLB_DWIDTH - 1]	PLB	I	-	PLB write data bus
Unused PLB Interface Signals					
P11	PLB_UABus[0:31]	PLB	I	-	PLB upper address bits
P12	PLB_SAValid	PLB	I	-	PLB secondary address valid
P13	PLB_rdPrim	PLB	I	-	PLB secondary to primary read request indicator
P14	PLB_wrPrim	PLB	I	-	PLB secondary to primary write request indicator
P15	PLB_abort	PLB	I	-	PLB abort bus request
P16	PLB_busLock	PLB	I	-	PLB bus lock
P17	PLB_MSize[0:1]	PLB	I	-	PLB data bus width indicator
P18	PLB_lockErr	PLB	I	-	PLB lock error
P19	PLB_wrBurst	PLB	I	-	PLB burst write transfer
P20	PLB_rdBurst	PLB	I	-	PLB burst read transfer
P21	PLB_wrPendReq	PLB	I	-	PLB pending bus write request

Table 1: **PLB to FSL Bridge I/O Signal Description *(Contd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P22	PLB_rdPendReq	PLB	I	-	PLB pending bus read request
P23	PLB_wrPendPri[0:1]	PLB	I	-	PLB pending write request priority
P24	PLB_rdPendPri[0:1]	PLB	I	-	PLB pending read request priority
P25	PLB_reqPri[0:1]	PLB	I	-	PLB current request priority
P26	PLB_TAttribute[0:15]	PLB	I	-	PLB transfer attribute
PLB Slave Interface Signals					
P27	Sl_addrAck	PLB	O	0	Slave address acknowledge
P28	Sl_SSize[0:1]	PLB	O	0	Slave data bus size
P29	Sl_wait	PLB	O	0	Slave wait
P30	Sl_rearbitrate	PLB	O	0	Slave bus rearbitrate
P31	Sl_wrDAck	PLB	O	0	Slave write data acknowledge
P32	Sl_wrComp	PLB	O	0	Slave write transfer complete
P33	Sl_rdDBus[0: C_SPLB_DWIDTH - 1]	PLB	O	0	Slave read data bus
P34	Sl_rdDAck	PLB	O	0	Slave read data acknowledge
P35	Sl_rdComp	PLB	O	0	Slave read transfer complete
P36	Sl_MBusy[0: C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave busy
P37	Sl_MWrErr[0: C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave write error
P38	Sl_MRdErr[0: C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave read error
Unused PLB Slave Interface Signals					
P39	Sl_wrBTerm	PLB	O	0	Slave terminate write burst transfer
P40	Sl_rdWdAddr[0:3]	PLB	O	0	Slave read word address
P41	Sl_rdBTerm	PLB	O	0	Slave terminate read burst transfer
P42	Sl_MIRQ[0: C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Master interrupt request
FSL Master Interface Signals					
P43	FSL_M_Clk	MFSL	O	N/A	This port provides the output clock to a master interface of a FSL bus when implemented in the asynchronous mode. This is the same as SPLB_Clk

Table 1: **PLB to FSL Bridge I/O Signal Description *(Contd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P44	FSL_M_Data	MFSL	O	0	The data output to the master interface of a FSL bus
P45	FSL_M_Control	MFSL	O	0	Single bit control signal that is propagated along with the data. Transmission of the control bit occurs when C_USE_CONTROL is set to 1 (default). If the control bit is not used by the slave, C_USE_CONTROL can be set to 0 to save area
P46	FSL_M_Write	MFSL	O	0	Output signal that is asserted when the data shall be written to the FSL link
P47	FSL_M_Full	MFSL	I	N/A	Input signal from the master interface of a FSL bus indicating that the FIFO is full.
FSL Slave Interface Signals					
P48	FSL_S_Clk	SFSL	O	N/A	This port provides the output clock to a master interface of a FSL bus when implemented in the asynchronous mode. This is the same as SPLB_Clk
P49	FSL_S_Data	SFSL	I	N/A	The data input bus from the slave interface of a FSL bus
P50	FSL_S_Control	SFSL	I	N/A	Single bit control that is propagated along with the data when C_USE_CONTROL is set to 1
P51	FSL_S_Read	SFSL	O	0	Output signal that is asserted when the data is read from a FSL link
P52	FSL_S_Exists	SFSL	I	N/A	Input signal from FSL bus indicating that data is available

PLB to FSL Bridge Design Parameters

To allow the user to obtain a PLB to FSL Bridge that is uniquely tailored for the system, certain features can be parameterized in the PLB to FSL Bridge design. This allows the user to configure a design that utilizes the

resources required by the system only and that operates with the best possible performance. The features that can be parameterized in the PLB to FSL Bridge design are as shown in Table 2.

Table 2: **PLB to FSL Bridge Design Parameters**

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
System Parameter					
G1	Target FPGA family	C_FAMILY	spartan3e, spartan3, spartan3a, spartan3adsp, spartan3an, virtex2, virtex2pro, virtex4, virtex5	virtex4	string
PLB Parameters					
G2	PLB Base Address	C_BASEADDR	Valid Address[1]	None[3]	std_logic_vector
G3	PLB High Address	C_HIGHADDR	Valid Address[2]	None[3]	std_logic_vector
G4	PLB least significant address bus width	C_SPLB_AWIDTH	32	32	integer
G5	PLB data width	C_SPLB_DWIDTH	32, 64, 128	32	integer
G6	Selects point-to-point or shared bus topology	C_SPLB_P2P	0 = Shared Bus Topology 1 = Point-to-Point Bus Topology[4]	0	integer
G7	PLB Master ID Bus Width	C_SPLB_MID_WIDTH	$\log_2$(C_SPLB_NUM_MASTERS) with a minimum value of 1	1	integer
G8	Number of PLB Masters	C_SPLB_NUM_MASTERS	1 - 16	1	integer
G9	Support Bursts	C_SPLB_SUPPORT_BURSTS	0	0	integer
G10	Width of the Slave Data Bus	C_SPLB_NATIVE_DWIDTH	32	32	integer
PLB to FSL Bridge Parameters					
G11	The number of data bits in the FSL interfaces	C_FSL_DWIDTH	32	32	Integer
G12	If the control bit shall be used	C_USE_CONTROL	0 - 1	1	Integer

Notes:

1. The user must set the values. The C_BASEADDR must be a multiple of the range, where the range is C_HIGHADDR - C_BASEADDR + 1.
2. C_HIGHADDR - C_BASEADDR must be a power of 2 greater than equal to C_BASEADDR + 0xF.
3. No default value will be specified to insure that the actual value is set, i.e., if the value is not set, a compiler error will be generated.
4. Value of '1' is not supported in this core.

Allowable Parameter Combinations

The address range specified by C_BASEADDR and C_HIGHADDR must be a power of 2, and must be at least 0xF.

For example, if C_BASEADDR = 0xE0000000, C_HIGHADDR must be at least = 0xE000000F.

PLB to FSL Bridge Parameter - Port Dependencies

The dependencies between the PLB to FSL Bridge core design parameters and I/O signals are described in Table 3. In addition, when certain features is deselected, the related logic will no longer be a part of the design. The unused input and output signals are set to a specified value.

Table 3: **PLB to FSL Bridge Parameter-Port Dependencies**

Generic or Port	Name	Affects	Depends	Relationship Description
Design Parameters				
G5	C_SPLB_DWIDTH	P7, P10, P33	-	Affects the number of bits in data bus
G7	C_SPLB_MID_WIDTH	P5	G8	This value is calculated as: $\log_2$(C_SPLB_NUM_MASTERS) with a minimum value of 1
G8	C_SPLB_NUM_MASTERS	P36, P37, P38, P42	-	Affects the number of PLB masters
G11	C_FSL_DWIDTH	P44, P49	-	Affects the number of bits in data bus
I/O Signals				
P5	PLB_masterID[0: C_SPLB_MID_WIDTH - 1]	-	G7	Width of the PLB_masterID varies according to C_SPLB_MID_WIDTH
P7	PLB_BE[0: (C_SPLB_DWIDTH/8) -1]	-	G5	Width of the PLB_BE varies according to C_SPLB_DWIDTH
P10	PLB_wrDBus[0: C_SPLB_DWIDTH - 1]	-	G5	Width of the PLB_wrDBus varies according to C_SPLB_DWIDTH
P33	Sl_rdDBus[0: C_SPLB_DWIDTH - 1]	-	G5	Width of the Sl_rdDBus varies according to C_SPLB_DWIDTH
P36	Sl_MBusy[0: C_SPLB_NUM_MASTERS - 1]	-	G8	Width of the Sl_MBusy varies according to C_SPLB_NUM_MASTERS
P37	Sl_MWrErr[0: C_SPLB_NUM_MASTERS - 1]	-	G8	Width of the Sl_MWrErr varies according to C_SPLB_NUM_MASTERS
P38	Sl_MRdErr[0: C_SPLB_NUM_MASTERS - 1]	-	G8	Width of the Sl_MRdErr varies according to C_SPLB_NUM_MASTERS

Table 3: **PLB to FSL Bridge Parameter-Port Dependencies *(Contd)***

Generic or Port	Name	Affects	Depends	Relationship Description
P42	SI_MIRQ[0: C_SPLB_NUM_MASTERS - 1]	-	G8	Width of the SI_MIRQ varies according to C_SPLB_NUM_MASTERS
P44	FSL_M_Data		G11	Width of the FSL_M_Data varies according to C_FSL_DWIDTH
P49	FSL_S_Data		G11	Width of the FSL_S_Data varies according to C_FSL_DWIDTH

PLB to FSL Bridge Register Descriptions

Table 4 shows all the PLB to FSL Bridge registers and their addresses.

Table 4: **PLB to FSL Bridge Registers**

Base Address + Offset (hex)	Register Name	Access Type	Default Value (hex)	Description
C_BASEADDR + 0x0	WRDATA	Write	N/A	Write Data address. Write only.
C_BASEADDR + 0x4	WRCTRL	Write	N/A	Write Control address. Write only.
C_BASEADDR + 0x8	RDDATA	Read	N/A	Read Data address. Read only
C_BASEADDR + 0xC	RDCTRL	Read	N/A	Read Control address. Read only
C_BASEADDR + 0x10	STATUS	Read	0x1	Status flags for PLB to FSL Bridge. Read only.
C_BASEADDR + 0x14	ERROR	Read	0x0	Error flags, clear on read. Read only.
C_BASEADDR + 0x18	Reserved	-	-	Reserved for future use
C_BASEADDR + 0x1C	Reserved	-	-	Reserved for future use

PLB to FSL Bridge Write Data Register (WRDATA)

Writing to this register will result in a write on the Master FSL Interface if the FSL_M_Full flag is not asserted. The FSL_M_Control bit will be set to 0 when writing to this register. The register is write only and a read request issued to WRDATA will be ignored. Bit assignment in the WRDATA register is described in Table 6.

Table 5: **Write Data register**

WRDATA	
0	C_FSL_DWIDTH-1

Table 6: **PLB to FSL Bridge Write Data Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - C_FSL_DWIDTH - 1	WRDATA	Write	-	Write register to transfer data word to the Master FSL interface on the bridge

PLB to FSL Bridge Write Control Register (WRCTRL)

Writing to this register will result in a write on the Master FSL Interface if the FSL_M_Full flag is not asserted. The FSL_M_Control bit will be set to 1 if C_USE_CONTROL is enabled when writing to this register otherwise it will be 0. The register is write only and a read request issued to WRCTRL will be ignored. Bit assignment in the WRCTRL register is described in Table 8.

Table 7: **Write Control Register**

WRCTRL	
0	C_FSL_DWIDTH-1

Table 8: **PLB to FSL Bridge Write Control Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - C_FSL_DWIDTH - 1	WRCTRL	Write	-	Write register to transfer control word to the Master FSL interface on the bridge

PLB to FSL Bridge Read Data Register (RDDATA)

Reading from this register will result in a read on the Slave FSL Interface if the FSL_S_Exists flag is asserted. If C_USE_CONTROL is enabled and FSL_S_Control bit is set to 1 the Control bit Error bit in the Error register will be asserted. The register is read only and a write request issued to RDDATA will be ignored. Bit assignment in the RDDATA register is described in Table 10.

Table 9: **Read Data Register**

RDDATA	
0	C_FSL_DWIDTH-1

Table 10: **PLB to FSL Bridge Read Data Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - C_FSL_DWIDTH - 1	RDDATA	Read	-	Read register to get data word from the Slave FSL interface on the bridge

PLB to FSL Bridge Read Control Register (RDCTRL)

Reading from this register will result in a read on the Slave FSL Interface if the FSL_S_Exists flag is asserted. If C_USE_CONTROL is enabled and FSL_S_Control bit is set to 0 the Control bit Error bit in the Error register will be asserted. The register is read only and a write request issued to RDCTRL will be ignored. Bit assignment in the RDCTRL register is described in Table 12.

Table 11: **Read Control Register**

RDCTRL	
0	C_FSL_DWIDTH-1

Table 12: **PLB to FSL Bridge Read Control Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - C_FSL_DWIDTH - 1	RDCTRL	Read	-	Read register to get control word from the Slave FSL interface on the bridge

PLB to FSL Bridge Status Register (STATUS)

The PLB to FSL Bridge Status Register contains the current status of the Master and Slave FSL interfaces. The register is read only and a write request issued to STATUS will be ignored. Bit assignment in the STATUS register is described in Table 14.

Table 13: **Status Register**

Reserved		Ctrl	Full	Empty
0	28	29	30	31

Table 14: **PLB to FSL Bridge Status Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 28	Reserved			Reserved for future use
29	Slave FSL Control	Read	’0’	Indicates the current status of the Slave FSL control bit ’0’ = FSL_S_Control bit is ’0’ ’1’ = FSL_S_Control bit is ’1’
30	Full	Read	’0’	Indicates the current status of the Master FSL FIFO ’0’ = There is room for more data ’1’ = The FIFO is full, any attempts to write data will be ignored and generate an error
31	Empty	Read	’1’	Indicates the current status of the Slave FSL FIFO ’0’ = There is data available ’1’ = The FIFO is empty, any attempts to read data will be ignored and generate an error

PLB to FSL Bridge Error Register (ERROR)

The PLB to FSL Bridge Error Register contains the error flags for PLB accesses to/from the master and slave FSL interfaces. The error register will be cleared at read, this means that all bits are sticky and that they indicate any errors that occurred since last time the error register was read. The register is read only and a write request issued to ERROR will be ignored. Bit assignment in the ERROR register is described in Table 16.

Table 15: **Error Register**

Reserved		Ctrl	Full	Empty
0	28	29	30	31

Table 16: **PLB to FSL Bridge Error Register Bit Definitions**

Bit(s)	Name	Core Access	Reset Value	Description
0 - 28	Reserved			Reserved for future use
29	Control Error	Read	'0'	Indicates if there has been a mismatch between using RDDATA and RDCTRL with the FSL_S_Control bit since the error register was last read '0' = No mismatch has occurred '1' = One or more mismatches has occurred
30	Full Error	Read	'0'	Indicates if there has been any attempts to write to the WRDATA or WRCTRL registers while the Full flag was asserted since the error register was last read '0' = No error has occurred '1' = One or more attempts to write while FSL link was full
31	Empty Error	Read	'0'	Indicates if there has been any attempts to read from the RDDATA or RDCTRL registers while the Empty flag was asserted since the error register was last read '0' = No error has occurred '1' = One or more attempts to read while FSL link was empty

Design Implementation

Target Technology

The intended target technology is Spartan and Virtex FPGAs.

Reference Documents

- *IBM CoreConnect™128-Bit Processor Local Bus, Architectural Specification (v4.6).*

Revision History

Date	Version	Revision
07/04/2007	1.0	Initial Xilinx release.