PLBV46 to OPB Bridge (v1.00a)

DS403 December 13, 2007 **Product Specification**

Introduction

The Processor Local Bus Version 4.6 (PLBV46) to On-chip Peripheral Bus (OPBv20) Bridge translates PLBv46 transactions into OPB transactions. The system designer uses the bridge in systems where a PLBv46 master device requires access to legacy OPB peripherals.

Features

- Bridges transactions as a 32-bit PLBv46 slave and 32-bit OPBv20 master.
- PLBv46 Slave interface
  - Supports connections to a 32-, 64-, or 128-bit PLBv46 bus and transactions from 32-, 64- and 128-bit masters that can talk to 32-bit slaves.
  - Decodes up to four separate address ranges with programmable lower and upper address boundaries for each range
  - Single transfers of 1-4 bytes. Read data mirroring supports conversion cycles from larger masters.
  - Supports only fixed length, burst transactions of up to sixteen quad-words, double-words, words, (for appropriately sized masters.)
  - Cacheline transactions of 4 and 8 words
  - Supports up to 8 PLBv46 masters (number of PLBv46 masters configurable via a design parameter)
  - Supports low latency point-to-point topology
  - 16-word buffer to increase PLBv46 bus utilization via posted writes.
- OPB Master interface
  - Utilizes byte enable interface
  - The OPB master re-attempts all slave retried transactions until they complete

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Spartan™ 3, Virtex™-II Pro, Virtex-4, Virtex-5,	
Version of Core	plbv46_opb_ bridge	v1_00_a
Resources Used		
	Min	Max
Slices	180	199
LUTs	285	312
FFs	188	244
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	9.1i or later	
Verification	N/A	
Simulation	ModelSim SE/EE 6.1e or later	
Synthesis	XST	
Support		
Support provided by Xilinx, Inc.		

Features (contd)

- The PLBv46:OPB clock period ration may be 1:1 or 1:2 (with the added requirement that a rising edge of the PLBv46 clock must be coincident with the rising edge of the OPB clock.)

PLBv46 and OPB Transaction Behavior

This section describes important information about the behavior of the PLBv46 bridge with respect to the PLBv46 and OPB protocols.

PLBv46 Transaction Qualifiers and Arbitration Signals

- Error and busy flags support up to 8 PLBv46 masters
- Accepts only memory transfers (**PLB_type[0:2]** = 000). Other transfer types are ignored by not returning an Sl_addrAck and no error is reported [1].

PLBv46 Data Transfers

- Supports non-burst/non-cacheline transfers of 1-16 bytes. The slave interface mirrors data as appropriate for master issued conversion cycles when the number of byte enables asserted exceeds four.
- Supports cacheline transfers of 4, 8, or 16 words in lineword first order. Write addresses must always start at the first word of the line. Read address may be issued to any location in the line but the bridge will zero out the low order address bits to align the address to the line start address. Data returns to the master sequentially from the start of the line to the end.
- Supports fixed-length burst transfers (**PLB_BE(0:C_PLBV46_ DWIDTH/8 -1)** greater than 0) of words (**PLB_size[0:3]** = 1010) up to 16 words.
- Masters must respect address boundaries and should not make requests that will result in either read or write transactions that cross the memory address range C_RNGn_HIGHADDR value. Doing show will result in unpredictable behaviour. This is true even if two address ranges have been set up by the user to be back-to-back. As an example, a fixed length read burst of 16 words starting at C_RNG1_HIGHADDR-8 should not be done because the last 8-words are beyond the address range.

OPB Data Transfers

- Master interface only supports 32-bit, byte enable slaves. (No support for dynamic bus sizing signals.)
- Data is not mirrored over inactive byte lanes. If a byte enable bit is zero, the corresponding data byte lane has an undefined value
- Master output signals do not need AND-OR gating logic in the OPB bus because they are gated internally to improve bus timing. OR-gates are sufficient for the OPB bus logic connection
- Master abort cycles are not generated

[1] This may or may not result in the PLBv46 arbiter timing out.

- If **OPB_retry** is asserted instead of **OPB_xferAck** for an OPB write transaction**,** the transaction will be retried until successful. The OPB bus will be released as required by the OPB specification for one clock after each receipt of **OPB_retry**.
- If the OPB transaction is terminated with **OPB_timeout** or **OPB_errAck**, the PLBv46 bus will assert **Sl_MWrErr** or **Sl_MRdErr**.

Functional Description

The Processor Local Bus (PLBv46) to On-chip Peripheral Bus (OPBv20) Bridge translates PLBv46 transactions into OPB transactions. The bridge functions as a slave on the PLBv46 side and a master on the OPB side.

The PLBv46 to OPB Bridge design is shown in Figure 1 and described in the following sections.

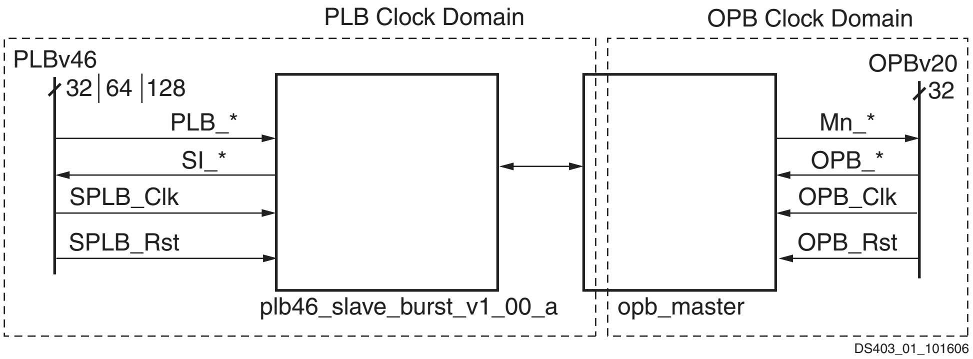


Figure 1: **High-Level Overview of the PLBv46 to OPB Bridge**

Clocking

The bridge provides for a PLBV46:OPB clock *period* ratio of 1:1 or 1:2. The bridge implementation requires that the clocks be generated by one DCM. This insures that the rising edges of the PLBv46 and OPB clocks are aligned and that the necessary and proper period constraint is applied to signals that cross time domain boundaries.

OPB Interface

All burst transfers greater than one word and all cacheline transfers are performed with the sequential address flag asserted (**Mn_seqAddr** = 1). The sequential address flag helps improve the performance of OPB slave peripherals.

The bridge performs all sequential bursts with bus lock asserted, as required by the OPB specification.

Slaves that generate an **OPB_retry** during an OPB master write or read, cause the OPB master to back off the bus for one cycle before attempting the transaction over again by requesting access to the bus. This process will be continued indefinitely until successful completion of the transaction. That means the PLBv46 bus performance will be negatively impacted by slaves that retry frequently.

OPB devices must return all read data requested or the bridge will continue attempting to get the data indefinitely.

Bridge to Bridge Communication - Deadlock Prevention

When a PLBv46 master is requesting a read on the OPB and an OPB master is requesting a read on the PLBv46, there is a possibility that the PLBv46 to OPB bridge can't access the OPB and the OPB to PLBv46 bridge can't access the PLBv46, thus resulting in deadlock.

The opb_plbv46_bridge_v1_00_a handles dead lock prevention.

Design Parameters

The plbv46_opb_bridge_v1_00_a provides for precise functionality and implementation tailoring via VHDL Generic parameters. These parameters are detailed in Table 1. The system design may elect to set certain parameters or utilize default settings as described in the table.

Table 1: **PLBV46_SLAVE_BURST Design Parameters**

Feature/Description	Parameter Name	Allowable Values	Default Values	VHDL Type
Decoder Address Range Definition				
Number of Address Ranges	C_ NUM_ADDR_RNG	1-4	1	integer
Address range definition base address	C_RNGn_BASEADDR (0 <= n <= 3)	0x00000000 to 0xFFFFFFFF	X"FFFFFFFF"	std_logic_vector
Address range definition high address	C_RNGn_HIGHADDR (0<=n<=3)	0x00000000 to 0xFFFFFFFF	X"00000000"	std_logic_vector
PLBv46 I/O Specification				
PLBv46 Master ID Bus Width	C_SPLB_MID_WIDTH	$\log_2$(**C_SPLB_NUM_MASTERS**) with a minimum value of 1	3	integer
Number of PLBv46 Masters	C_SPLB_NUM_MASTERS	1 to 8	8	integer
Size of the smallest master attached to the PLBv46	C_SPLB_SMALLEST_MASTER	32, 64, 128	32	integer
Width of the PLBv46 Least Significant Address Bus	C_SPLB_AWIDTH	32	32	integer
Width of the PLBv46 Data Bus	C_SPLB_DWIDTH	32, 64, 128	32	integer
Slave Attachment I/O Specification				
Selects point-to-point or shared PLBv46 topology.	C_SPLB_P2P	0 = Shared Bus Topology 1 = Point-to-Point Bus Topology	0	integer
BRIDGE CONFIGURATION				
Establishes the ratio of PLBv46 to OPB bus clock periods. The clocks must be synchronous with minimal phase difference.	C_BUS_CLOCK_PERIOD_RATIO	1=1:1, 2=1:2	1	integer

Table 1: **PLBV46_SLAVE_BURST Design Parameters**

Feature/Description	Parameter Name	Allowable Values	Default Values	VHDL Type
FPGA Family Type				
Xilinx FPGA Family	C_FAMILY	"spartan3", "virtex4", "virtex5"	virtex4	string

Notes:

1. This Parameter VHDL type is a custom type defined in the ipif_pkg.vhd.

Parameter Descriptions

Address Range Definition

The PLBv46 slave attachment within the plbv46_opb_bridge_v1_00_a implements a general purpose address decoding strategy involving, chip enable/chip select control signal generation. The nature of the bridge functionality does not require the chip enable capability of the slave attachment which is ordinary used for things like register addressing within a typical pcore. The bridge provides for address decoding (in non- point-to-point topologies) for up to four internal chip selects based on six base address and high address parameter pairs. The parameter C_NUM_ADDR_RNG determines which of the four pairs are relevant.

When operating in a shared bus environment (C_SPLB_P2P=0) the user must set the address range (or ranges) which the bridge recognizes for transactions to be carried over to the OPB bus.

It is not necessary to order address spaces in ascending order when setting the address range pairs. Each address space is processed independently from any of the other address space pairs.

C_NUM_ADDR_RNG

Specifies the number of valid address range pairs set via C_RNGn_BASEADDR and C_RNGn_HIGHADDR

C_RNGn_BASEADDR, C_RNGn_HIGHADDR

The address range for an address space definition recognized by the bridge is set by a pair of these parameters. Each address space is by definition a contiguous block of addresses as viewed from the host microprocessor's total addressable space but each pair need not be contiguous with the others. The size of the address space is the difference between these two parameter values and must be a power of two. These addresses are byte relative addresses.

The user must follow several rules when assigning values to the address pairs. These rules assure that the address range will be correctly decoded in the bridge’s slave attachment. First, the system designer must decide the required address range to be defined. The block size (in bytes) must be a power of 2 (i.e. 2, 4, 8,16,32,64,128,256 and so on). Secondly, the Base Address must start on an address boundary that is a multiple of the chosen block size. For example, an address space is needed that will include 2048 bytes (0x800 hex) of the system memory space. Valid Base Address entries are 0x00000000, 0x00000800, 0xFFFFF000, 0x90001000, etc. A value of 0x00000120 is not valid because it is not a multiple of 0x800 (2048). Thirdly, the High Address entry is equal to the assigned Base Address plus the block size minus 1. Continuing the example of a 2048 byte block size, a Base Address of 0x00000000 yields a High Address of 0x000007FF; a Base Address of 0x00000800 would require a corresponding High Address value of 0x00000FFF.

C_SPLB_P2P

This parameter is defined as an integer. Setting this parameter to 0 will configure the plbv46_slave_burst for a PLBv46 shared bus application. Setting this parameter to 1 will configure the plbv46_slave_burst for a PLBv46 point-to-point bus application. In a point-to-point configuration the slave attachment acknowledges all address cycles on the PLBv46 and only address decodes based on the number of CEs configured for the User IP. This reduces some FPGA resources. Latency is also reduced in a point-to-point configuration.

Notes:

1. If more than 1 address range is defined in a point-to-point configuration (i.e. when C_SPLB_P2P = 1) then the slave attachment will instantiate the address decode logic to distinguish multiple address ranges irrespective of the C_SPLB_P2P setting.
2. When setting C_SPLB_P2P = 1 the user must also set C_SPLB_MID_WIDTH = 1, and C_SPLB_NUM_MASTERS = 1.

C_SPLB_MID_WIDTH

This parameter is defined as an integer and has a minimum value of 1. It is equal to $\log_2$ of the number of PLBv46 Masters connected to the PLBv46 bus or 1, whichever is greater. It is used to size the PLB_masterID bus input from the PLBv46 Bus to the Slave Attachment.

For example, if eight PLBv46 Masters are connected to the PLBv46 Bus, then this parameter must be set to $\log_2(8)$ which is equal to 3. The PLBv46 Bus PLB_masterID bus will be sized to 3 bits wide. If only one master exists, then the parameter needs to be set to 1.

C_SPLB_NUM_MASTERS

This parameter is defined as an integer and is equal to the number of Masters connected to the PLBv46 bus. This parameter is used to size the Sl_MBusy and Sl_MErr slave reply buses to the PLBv46. For example, if eight PLBv46 Masters are connected to the PLBv46 Bus, then this parameter must be set to 8. The Sl_MBusy bus and Sl_MErr bus will be sized to 8 bits wide each.

C_SPLB_SMALLEST_MASTER

This parameter is defined as an integer and is equal to the native data width of the smallest Master connected to the PLBv46 bus that will be accessing the plbv46_slave_burst attachment. This generic is used to generate and optimize steering logic in the slave attachment.

C_SPLB_DWIDTH

This integer parameter is used by the PLBv46 Slave to size PLBv46 data bus related components within the Slave Attachment. This value should be set to match the actual width of the PLBv46 bus, 32, 64 or 128-Bits.

C_BUS_CLOCK_PERIOD_RATIO

The bridge support operation in either 1:1 or 1:2 (PLBv46:OPB) clock period ratio systems. For 1:1 ratio set this parameter to 1. For a 1:2 ratio set this parameter to 2.

C_FAMILY

This parameter is defined as a string. It specifies the target FPGA technology for implementation of the PLBv46 Slave. This parameter is required for proper selection of FPGA primitives. The configuration of these primitives can vary from one FPGA technology family to another.

Design Ports

Table 2: **plbv46_opb_bridge_v1_00_a Signal Ports**

Port	Signal Name	Interface	Direction	Default	
System Signals					
P1	SPLB_Clk	PLBV46	In		Slave PLBv46 Clock
P2	SPLB_Rst	PLBV46	In		Slave PLBv46 Reset
PLBv46 Bus Slave Signals					
P3	PLB_ABus(0:31)	PLBV46	In		Address bus
P4	PLB_UABus(0:31)	PLBV46	In		Upper address bus
P5	PLB_PAValid	PLBV46	In		Primary address valid
P6	PLB_SAValid	PLBV46	In		secondary address valid
P7	PLB_rdPrim	PLBV46	In		read primary
P8	PLB_wrPrim	PLBV46	In		write primary
P9	PLB_masterID(0:C_SPLB_MID_ WIDTH-1)	PLBV46	In		master identification
P10	PLB_abort	PLBV46	In		transaction abort
P11	PLB_busLock	PLBV46	In		bus lock
P12	PLB_RNW	PLBV46	In		read not write
P13	PLB_BE(0:(C_SPLB_ DWIDTH/8)-1)	PLBV46	In		byte enable
P14	PLB_MSize(0:1)	PLBV46	In		master size
P15	PLB_size(0:3)	PLBV46	In		size
P16	PLB_type(0:2)	PLBV46	In		transaction type
P17	PLB_lockErr	PLBV46	In		bus lock error
P18	PLB_wrDBus(0:C_ SPLB_DWIDTH-1)	PLBV46	In		write data bus
P19	PLB_wrBurst	PLBV46	In		write burst
P20	PLB_rdBurst	PLBV46	In		read burst
P21	PLB_wrPendReq	PLBV46	In		write pending request
P22	PLB_rdPendReq	PLBV46	In		read pending request
P23	PLB_wrPendPri(0:1)	PLBV46	In		write pending priority
P24	PLB_rdPendPri(0:1)	PLBV46	In		read pending priority
P25	PLB_reqPri(0:1)	PLBV46	In		request primary
P26	PLB_TAttribute(0:15)	PLBV46	In		transaction attribute
Slave Response Signals					
P27	Sl_addrAck	PLBV46	Out		slave address acknowledge

Table 2: **plbv46_opb_bridge_v1_00_a Signal Ports** ***(Contd)***

Port	Signal Name	Interface	Direction	Default	
P28	Sl_SSize(0:1)	PLBV46	Out		slave size
P29	Sl_wait	PLBV46	Out		slave wait
P30	Sl_rearbitrate	PLBV46	Out		rearbitrate
P31	Sl_wrDAck	PLBV46	Out		write data acknowledge
P32	Sl_wrComp	PLBV46	Out		write complete
P33	Sl_wrBTerm	PLBV46	Out		write burst terminate
P34	Sl_rdDBus(0:C_SPLB_ DWIDTH-1)	PLBV46	Out		read data bus
P35	Sl_rdWdAddr(0:3)	PLBV46	Out		read word address
P36	Sl_rdDAck	PLBV46	Out		read data acknowledge
P37	Sl_rdComp	PLBV46	Out		read complete
P38	Sl_rdBTerm	PLBV46	Out		read burst terminate
P39	Sl_MBusy(0:C_SPLB_NUM_MASTERS-1)	PLBV46	Out		slave master busy
P40	Sl_MWrErr(0:C_SPLB_NUM_ MASTERS-1)	PLBV46	Out		master write error
P41	Sl_MRdErr(0:C_SPLB_ NUM_MASTERS-1)	PLBV46	Out		master read error
P42	Sl_MIRQ(0:C_SPLB_ NUM_MASTERS-1)	PLBV46	Out		master interrupt request
		OPBv20 Master Signals			
P43	OPB_Clk	OPB	In		OPB bus clock
P44	OPB_Rst	OPB	In		OPB bus reset
P45	Mn_request	OPB	Out		Master transaction request
P46	Mn_busLock	OPB	Out		master bus lock
P47	Mn_select	OPB	Out		master select
P48	Mn_RNW	OPB	Out		master transaction read not write
P49	Mn_BE(0:32/8-1)	OPB	Out		master byte enable
P50	Mn_seqAddr	OPB	Out		master sequential addresses
P51	Mn_DBus(0:32-1)	OPB	Out		master data bus
P52	Mn_ABus(0:31)	OPB	Out		master address bus
P53	OPB_MGrant	OPB	In		Master grant
P54	OPB_xferAck	OPB	In		transfer acknowledge
P55	OPB_errAck	OPB	In		transfer error acknowledge

Table 2: **plbv46_opb_bridge_v1_00_a Signal Ports *(Contd)***

Port	Signal Name	Interface	Direction	Default	
P56	OPB_retry	OPB	In		transfer retry
P57	OPB_timeout	OPB	In		transfer timeout
P58	OPB_DBus(0:32 - 1)	OPB	In		data bus

Design Implementation

Target Technology

The intended target technology is Virtex-4, Virtex-5 and Spartan-3 FPGA families.

Device Utilization and Performance Benchmarks

Core Performance

Because the plbv46_opb_bridge is a module that will be used with other design pieces in the FPGA, the resource utilization and timing numbers reported in this section are estimates only. When the plbv46_opb_bridge is combined with other pieces of the FPGA design, the utilization of FPGA resources and timing of the design will vary from the results reported here.

For Spartan-3E systems the performance of the PLBv46 interface in 1:2 clock ratio mode should meet or exceed 90 Mhz. Similarly, for Virtex-5 systems the peformance should meet or exceed 120 Mhz. Note that in some system configurations (in either 1:1 or 1:2 clock ratio mode) the OPB bus could be the limiting factor thus preventing the PLBv46 interface from reaching full speed. Use of the core in 1:1 clock ratio mode is offered only as an option and no clock frequency performance numbers are provided for it.

The plbv46_opb_bridge resource utilization benchmarks for an xc5vlx50-1-ff676 FPGA for a variety of generic parameter combinations applied on top of a base parameter set are shown in Table 3.

Table 3: **FPGA Resource Utilization Benchmarks**

Parameter Values (For Example)							Device Resources		
C_NUM_ADDR_RNG	RNG0 size	RNG1 size	RNG2 size	RNG3 size	C_SPLB_P2P	C_BUS_CLOCK_PERIOD_RATIO	Slice Registers	Slice LUTs	Occupied Slices
X	X	X	X	X	1	1	188	308	199
1	0x20000000	X	X	X	0	1	234	285	184
2	0x20000000	0x20000000	X	X	0	1	237	291	195
3	0x20000000	0x20000000	0x20000000	X	0	1	240	291	180
4	0x20000000	0x20000000	0x20000000	0x20000000	0	1	243	293	199

Table 3: **FPGA Resource Utilization Benchmarks**

4	0x200	0x200	0x200	0x200	0	1	243	307	192
4	0x200	0x200	0x200	0x200	0	2	244	312	198

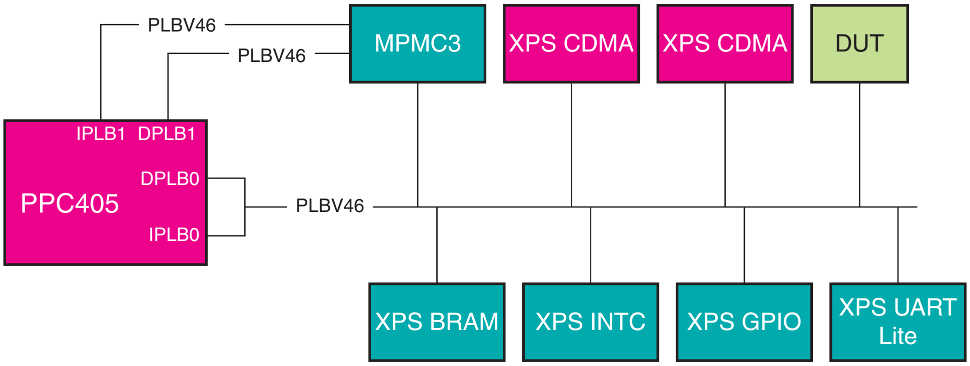
Notes: Generic parameters used:

3. C_SPLB_MID_WIDTH=1
4. C_SPLB_NUM_MASTER=1
5. C_SPLB_SMALLEST_MASTER=32
6. C_SPLB_DWIDTH=32
7. C_FAMILY="virtex5"

System Performance

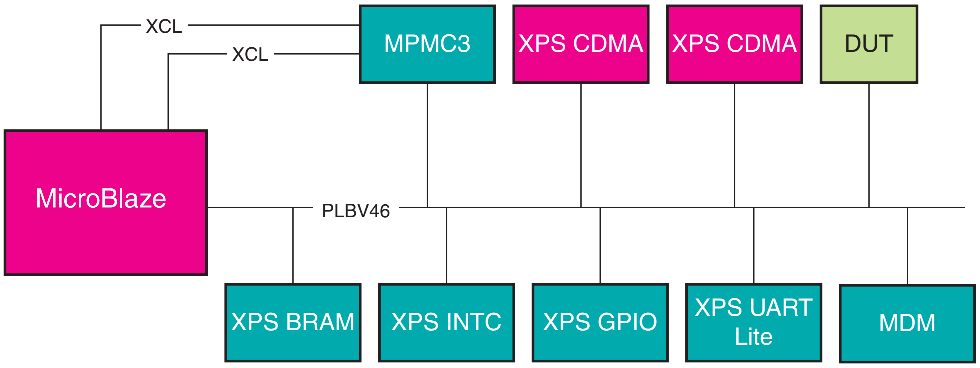
To measure the system performance (Fmax) of this core, this core was added to a Virtex-4 system, a Virtex-5 system, and a Spartan-3A system as the Device Under Test (DUT) as shown in Figure 2, , Figure 3 and Figure 4. Note that the DUT in this core is actually the PLBv46 OPB bridge and the OPB PLBv46 bridge with the OPB buses connected.

Because the PLBV46 to OPB Bridge core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When this core is combined with other designs in the system, the utilization of FPGA resources and timing of the core design will vary from the results reported here.



v4_fx_sys

Figure 2: **Virtex-4 FX System**



v5_lxt_sys

Figure 3: **Virtex-5 LX System**

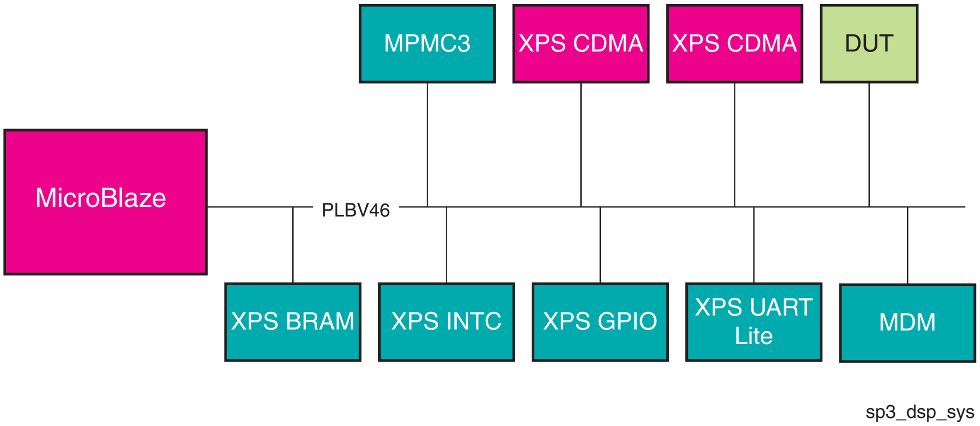


Figure 4: **Spartan-3A System**

The target FPGA was then filled with logic to drive the LUT and BRAM utilization to approximately 70% and the I/O utilization to approximately 80%. Using the default tool options and the slowest speed grade for the target FPGA, the resulting target FMax numbers are shown in Table 4.

Table 4: **PLBv46 to OPB Bridge System Performance**

Target FPGA	Target f_{MAX} (MHz)
S3A700 -4	90
V4FX60 -10	100
V5LXT50 -1	120

The target fMAX is influenced by the exact system and is provided for guidance. It is not a guaranteed value across all systems.

Reference Documents

The following documents contain reference information important to understanding the design of the PLBv46 to OPB bridge:

- *IBM CoreConnect 128-Bit Processor Local Bus: Architecture Specification*, Version 4.6
- *IBM CoreConnect 64-Bit On-Chip Peripheral Bus: Architecture Specifications*, Version 2.1
- *Xilinx DS562 PLBV46 Slave Burst (v1.00a)*, August 30, 2006
- *Xilinx PLBv46 Interconnect and Interfaces Simplifications and Feature Subset Specification* (Rev 0.6), August 15, 2006

Revision History

Date	Version	Revision
6/19/07	1.0	Initial Xilinx release.
10/3/2007	1.1	Added FMax Margin System Performance section.
12/13/2007	1.2	Added Virtex-II Pro support.