LogiCORE IP Processor System Reset Module (v3.00a)

DS406 July 23, 2010 **Product Specification**

Introduction

The Xilinx Processor System Reset Module design allows customers to tailor their designs to suit their application by setting certain parameters to enable/disable features. The parameterizable features of designs are discussed in the Design Parameters section.

Features

- Asynchronous external reset input is synchronized with clock
- Asynchronous auxiliary external reset input is synchronized with clock
- Both the external and auxiliary reset inputs are selectable active high or active low
- Selectable minimum pulse width for reset inputs to be recognized
- Selectable load equalizing
- DCM Locked input
- Power On Reset generation
- Parameterized Active Low Reset signal generation for core and for interconnect
- Sequencing of reset signals coming out of reset:
  - First - bus structures come out of reset
    - Interconnect, PLB and OPB Arbiter and bridges, for example
  - Second - Peripheral(s) come out of reset 16 clocks later
    - UART, SPI, IIC for example
  - Third - the CPU(s) come out of reset 16 clocks after the peripherals

LogiCORE IP Facts Table		
Core Specifics		
Supported Device Family[1]	Virtex®-4/4Q/4QV, Virtex-5/5FX, Virtex-6/6CX, Spartan®-6, Spartan-3, Spartan-3E, Spartan-3A/3A DSP, Automotive Spartan-3/3A/3E/3A DSP	
Supported User Interfaces	PLBv46	
Resources		
	Min	Max
LUTs	—	120
I/Os	22	66
FFs	—	120
Provided with Core		
Documentation	Product Specification	
Design Files	VHDL	
Example Design	Not Provided	
Test Bench	Not Provided	
Constraints File	Not Provided	
Simulation Model	Not Provided	
Tested Design Tools		
Design Entry Tools	Xilinx ISE® v12.2 and above	
Simulation	Mentor Graphic ModelSim v6.5c and above	
Synthesis Tools	XST 12.2 and above	
Support		
Provided by Xilinx, Inc.		

Notes:
1. For a complete listing of supported devices, see the release notes for this core.

Functional Description

The Processor Reset Module block diagram is shown in Figure 1.

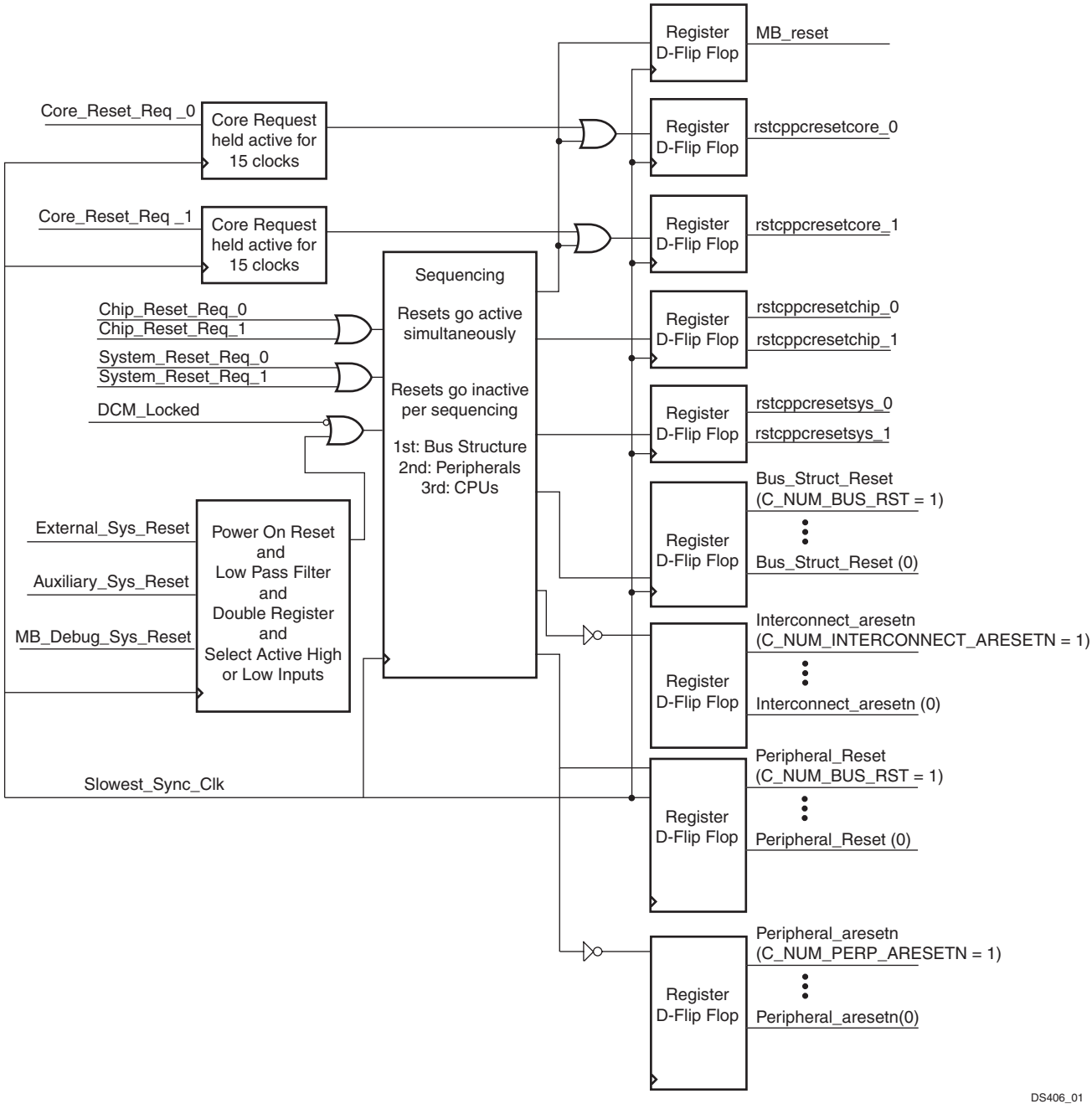

Figure 1: **Module Block Diagram for the Processor System Reset Module**

Processor System Reset Module Circuit Description

The Processor System Reset Module has eleven inputs and a minimum of nine outputs. Also, there are six generics that can be set by the user. Additional outputs can be generated through the use of the generics C_NUM_BUS_RST and C_NUM_PREP_RST.

Figure 2 shows the Processor System Reset Module timing when an Ext_Reset_In occurred. The timing diagram is identical for an occurrence of C_NUM_BUS_RST.

For this example C_NUM_BUS_RST is set to 5 and C_NUM_BUS_RST is set to '0', active low.

Generic and Signal Description

C_EXT_RST_WIDTH sets how wide, in number of Slowest_sync_clk clocks, a change on Ext_Reset_In must be before the change is detected and used by the Processor System Reset Module. For example, if C_EXT_RST_WIDTH is set to 5, then the Ext_Reset_In must become active and stay active for at least five clocks before a reset is initiated.

There is a one or two clock latency caused by the meta-stability circuit. Because the Ext_Reset_In does not have to be synchronous with the input clock, the exact number of clocks cannot be determined. The reset becomes active in six or seven clocks after the input has gone active and stayed active for five clocks.

After Ext_Reset_In has gone inactive for five clocks the sequencing to come out of reset begins. If, during the sequencing, Ext_Reset_In goes active for five or more clocks all outputs become active again.

C_AUX_RST_WIDTH sets the number of clocks wide a change on Aux_Reset_In must be before the change is detected and used by the Processor System Reset Module. Aux_Reset_In performs exactly the same as Ext_Reset_In.

C_EXT_RESET_HIGH is used to set the value for which Ext_Reset_In causes a reset. If this generic is set to a '1', when Ext_Reset_In is high on a rising edge of clock, a reset is initiated.

C_AUX_RESET_HIGH is used to set the value for which Aux_Reset_In causes a reset. If this generic is set to a '0', when Aux_Reset_In is low, a reset is initiated.

C_NUM_BUS_RST and C_NUM_INTERCONNECT_ARESETN are used to generate additional Bus_Struct_Reset and Interconnect Structure Reset signals. This helps with signal loading and routing. In general each bus may have its own Bus_Struct_Reset (Interconnect_aresetn in case of interconnect) signal. For example, if a system has one PLB and two OPBs then C_NUM_BUS_RST may be set to three. However, the C_NUM_BUS_RST may be set to one and the three reset inputs can be driven by the same output. The Bus_Struct_Reset output(s) should reset the arbiter(s) and bridges located on the bus. The same explanation applies to the number of Interconnect instances present in the system. Please note that the reset signal polarity for interconnect instances are active low when asserted.

C_NUM_PERP_RST and C_NUM_PERP_ARESETN are used to generate additional Peripheral_Reset (active high) and Peripheral_aresetn (active low) signals. This helps with signal loading and routing. In general every peripheral may have its own Peripheral_Reset signal (Peripheral_aresetn in case of peripherals connected to interconnect in a system). For example, if there is one ATM on the PLB and two UARTs, one 10/100 Ethernet controller and one IIC on the OPB, then C_NUM_PERP_RST may be set to five. However, the C_NUM_PERP_RST may be set to one and all peripheral resets can be driven by the same output. The same explanation applies to the number of peripherals connected to Interconnect instances present in the system. Please note that the reset signal polarity for peripherals connected to interconnects are active low when asserted.

MB_Debug_Sys_Rst is an input signal that will perform the same type of reset as Ext_Reset_In. The width of this signal complies to the same width requirement as for Ext_Reset_In set by the parameter C_EXT_RST_WIDTH.

MB_Debug_Sys_Rst is always active high, that is, it is not affected by the parameter C_EXT_RESET_HIGH. Normally this signal is connect to the Microprocessor Debug Module, MDM.

DCM_Locked is an input to the reset module. If the system does not use any DCMs this input should be tied high. If the system uses one DCM to generate system clocks the output from the DCM should be connected to the input on the reset module. If the system contains more than one DCM to generate system clocks, the DCM output that achieves lock last should be connected to the input.

The Slowest_Sync_Clk input should be connected to the slowest synchronous clock used in the system. This is typically the OPB clock, however, it could be any of the bus or CPU clocks. The Core_Reset_Req , Chip_Reset_Req, and System_Reset_Req inputs are signals generated by the PowerPC® processor core(s), each having its own set of signals denoted by "_0" or "_1" appended to the signal name. Each of these resets can be generated by a JTAG command or by the second expiration of the watchdog timer or by writing a non-zero value to the reset (RST) field of the Debug Control Register 0 (DBCR0). The Core_Reset_Req_0 and Core_Reset_Req_1 only activates the Rstcppcresetcore_0 or Rstcppcresetcore_1 respectively; no other logic is reset.

Chip_Reset_Req causes the Rstcppcresetcore, the Rstcppcresetchip, the MB_Reset, the Bus_Struct_Reset, the Peripheral_Reset, Interconnect_aresetn and Peripheral_aresetn to occur. System_Reset_Req causes all the above and Rstcppcresetsys.

The MB_Reset is generated whenever there is a Rstcppcresetchip generated.

A Chip_Reset_Req is stretched such that the outputs remain active for 48 clocks as shown in Figure 3. A Core_Reset_Req is stretched such that the output remains active for at least 15 clocks as shown in Figure 4. A System_Reset_Req is stretched such that the outputs remain active for at least 61 clocks as shown in Figure 5.

All outputs go active on the same edge of the clock. However, there is a sequencing that occurs when releasing the reset signal. The first reset signals to go inactive are the Bus_Struct_Reset and Interconnect_aresetn, the Rstcppcsysreset and the Rstcppcchipreset, 16 clocks later the Peripheral_Reset and Peripheral_aresetn will go inactive, 16 clocks later the Rstcppccorereset and the MB_Reset will go inactive. At this point all the resets are inactive and processing can begin.

There are two generics which decides the width of active low reset output signals. The parameter C_NUM_INTERCONNECT_ARESETN and C_NUM_PERP_ARESETN will decide the width of active low reset signals. The Interconnect_aresetn will provide the active low reset to interconnect and Peripheral_aresetn will provide the active low reset to peripherals. The active width of Interconnect_aresetn will be similar to the Bus_Struct_Reset signal width. The active width of Peripheral_aresetn will be similar to the Peripheral_Reset signal width. The active low resets are mainly targeted for AXI based peripherals or the peripherals which need active low reset input.

MB_Debug_Sys_Rst, Ext_Reset_In and Aux_Reset_In will cause Rstcppcresetsys, Rstcppcresetchip and Rstcppcresetcore being asserted.

The Power On Reset condition will cause all the reset outputs to become active within the first two clocks of a power up and remain active for 16 clocks. The resets will then begin the sequencing as shown in Figure 2.

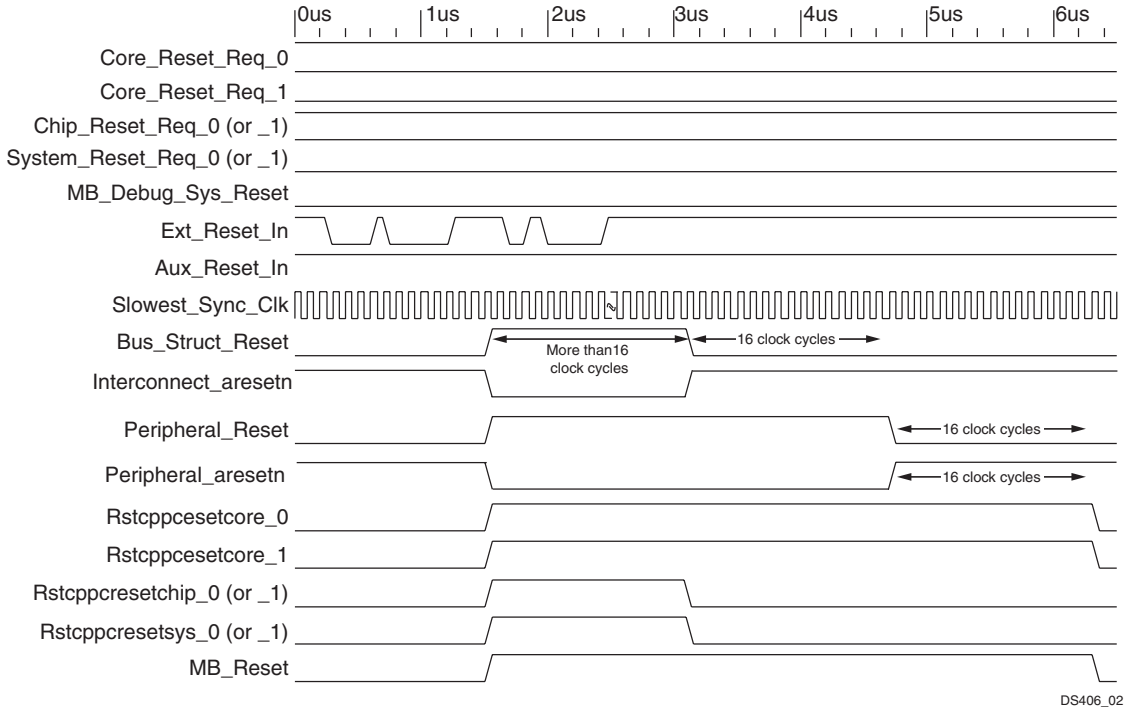

Figure 2: **Processor System Reset Module - Ext_Reset_In (active low)**

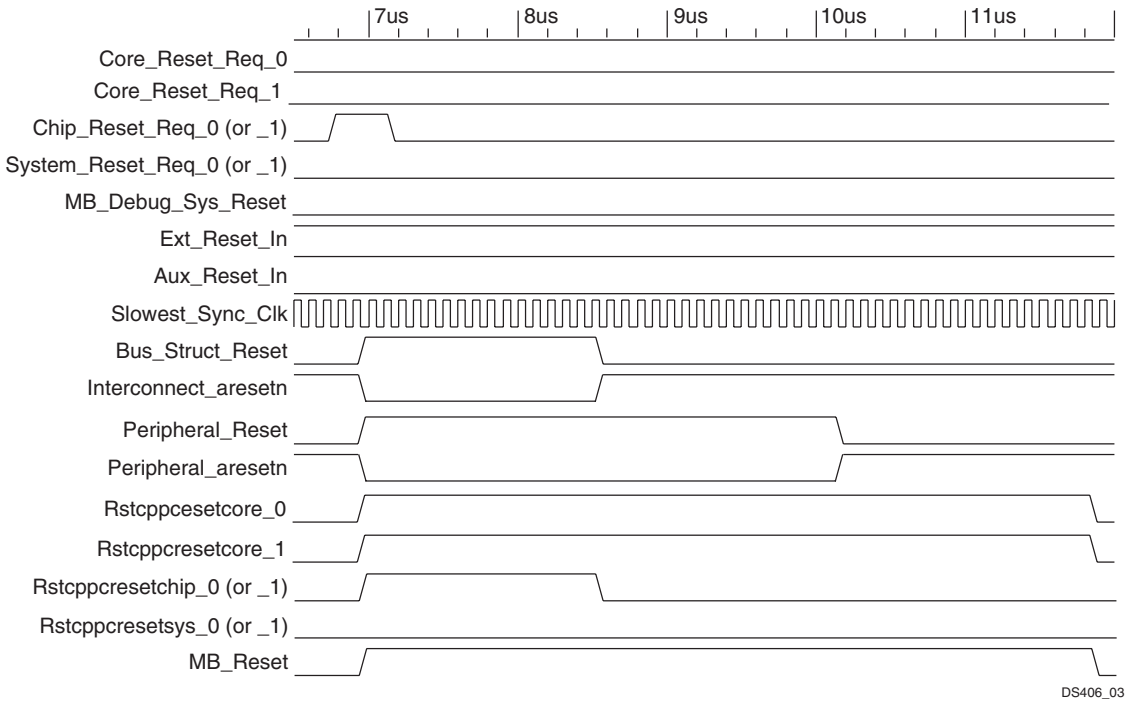

Figure 3: **Processor System Reset Module - Chip_Reset_Req**

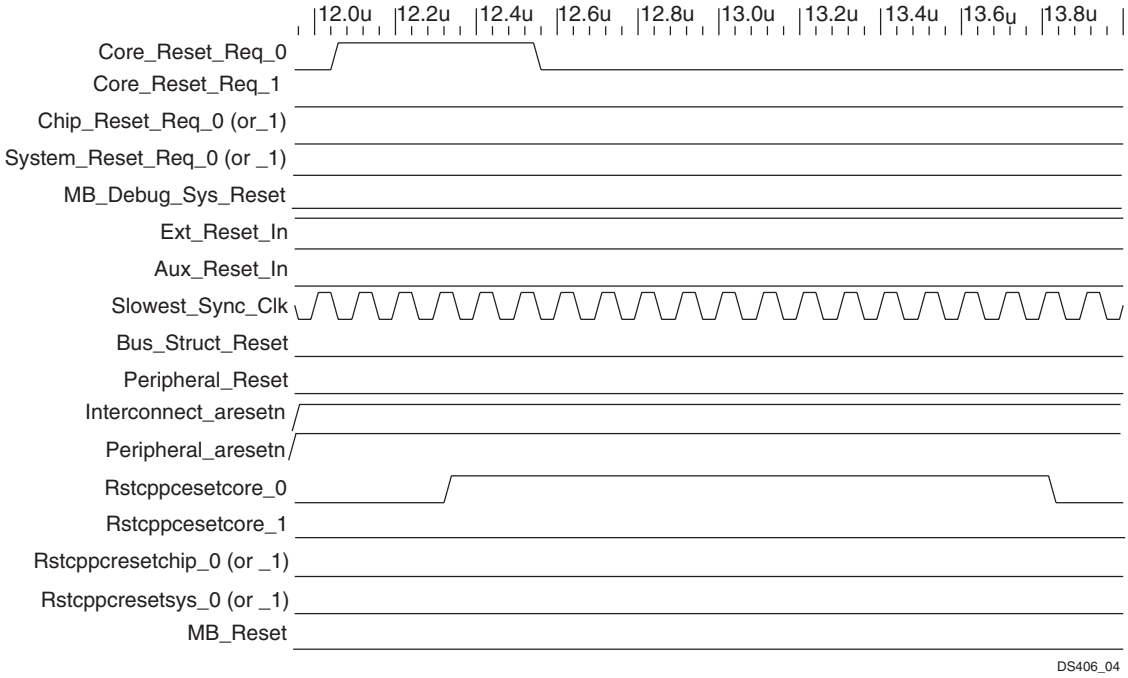

Figure 4: **Processor System Reset Module - Core_Reset_Req**

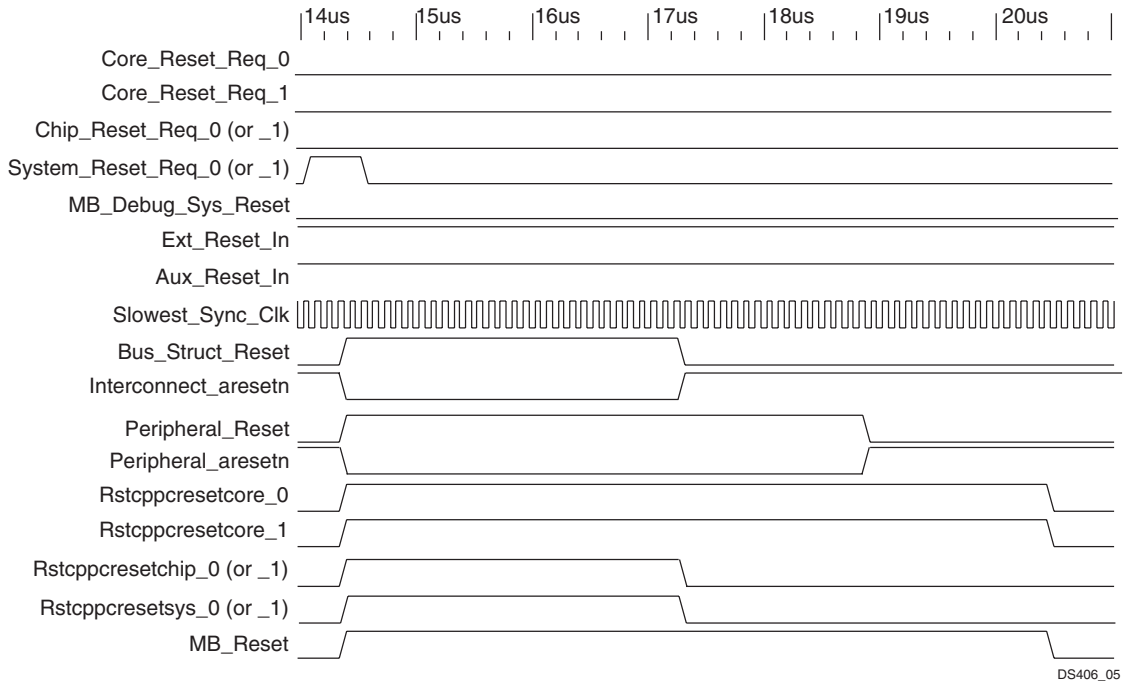

Figure 5: **Processor System Reset Module - System_Reset_Req**

Design Parameters

To allow users to obtain a Processor System Reset Module that is uniquely tailored for their system, certain features can be parameterized in the Processor System Reset Module design, thereby providing a design that utilizes only the resources required by their system and runs at the best possible performance. The features that can be parameterized in the Xilinx Processor System Reset Module design are shown in Table 1.

Table 1: **Processor System Reset Module Design Parameters**

Generic	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
Processor System Reset Module Features					
G1	Number of clocks before input change is recognized on the Ext_Reset_In and the MB_Debug_Sys_Rst inputs	C_EXT_RST_WIDTH(1)	1 - 16	4	integer
G2	Number of clocks before input change is recognized on the Aux_Reset_In input	C_AUX_RST_WIDTH(1)	1 - 16	4	integer
G3	Defines the active state of the Ext_Reset_In input	C_EXT_RESET_HIGH	'1' = Reset generated when external reset = '1' '0' = Reset generated when external reset = '0'	1	std_ logic
G4	Defines the active state of the Aux_Reset_In input	C_AUX_RESET_HIGH	'1' = Reset generated when external reset = '1' '0' = Reset generated when external reset = '0'	1	std_ logic
G5	Number of Bus_Struct_Reset registered outputs. In general, may equal number of instantiated buses.	C_NUM_BUS_RST	1 - 8	1	integer
G6	Number of Peripheral_Reset registered outputs. In general, may equal number of peripherals.	C_NUM_PERP_RST	1 - 16	1	integer
G7	Number of Interconnect_aresetn registered outputs. In general, may equal number of instantiated interconnects.	C_NUM_INTER CONNECT_ARESETN	1 - 8	1	integer
G8	Number of Peripheral_aresetn registered outputs. In general, may equal number of peripherals connected to interconnect.	C_NUM_PERP_ ARESETN	1 - 16	1	integer

Notes:

1. Though the core supports the external reset width for more than 16 cycles, it is recommended that the user should enter the reset widths between specified range only.

I/O Signals

The I/O signals for the Processor System Reset Module are listed in Table 2. The interfaces referenced in this table are shown in Figure 5 the Processor System Reset Module block diagram.

Table 2: **Processor System Reset Module I/O Signals**

Port	Signal Name	Interface	I/O	Description
System				
P1	Slowest_sync_clk	System	I	Slowest Synchronous Clock - Typically OPB clock
P2	Ext_Reset_In	System	I	External Reset Input - Active high or low based upon the generic C_EXT_RESET_HIGH
P3	MB_Debug_Sys_Rst	System	I	MDM reset input - Always active high, minimum width defined by parameter C_EXT_RST_WIDTH
P4	Aux_Reset_In	System	I	Auxiliary Reset Input - Active high or low based upon the generic C_AUX_RESET_HIGH
P5	Core_Reset_Req_0	System	I	PowerPC(0) processor requesting a core reset
P6	Core_Reset_Req_1	System	I	PowerPC(1) processor requesting a core reset
P7	Chip_Reset_Req_0	System	I	PowerPC(0) processor requesting a chip reset
P8	Chip_Reset_Req_1	System	I	PowerPC(1) processor requesting a chip reset
P9	System_Reset_Req_0	System	I	PowerPC(0) processor requesting a system reset
P10	System_Reset_Req_1	System	I	PowerPC(1) processor requesting a system reset
P11	Dcm_locked	System	I	DCM locked will cause all outputs to remain active until Dcm_locked goes high which will cause the resets to sequence to their inactive state.
P12	rstcppcresetcore_0	System	O	PowerPC(0) processor core reset - active high
P13	rstcppcresetcore_1	System	O	PowerPC(1) processor core reset - active high
P14	rstcppcresetchip_0	System	O	PowerPC(0) processor chip reset - active high
P15	rstcppcresetchip_1	System	O	PowerPC(1) processor chip reset - active high
P16	rstcppcresetsys_0	System	O	PowerPC(0) processor system reset - active high
P17	rstcppcresetsys_1	System	O	PowerPC(1) processor system reset - active high
P18	MB_Reset	System	O	MB Core Reset - active high
P19	Bus_Struct_Reset(0 to C_NUM_BUS_RST - 1)(1)	System	O	Bus Structures reset - for example, arbiters for PLB, OPB or Bridges ... etc. (active high)
P20	Peripheral_Reset(0 to C_NUM_PERP_RST - 1)(2)	System	O	Peripheral reset is for all peripherals attached to any bus that is synchronous with the Slowest_sync_clk. (active high)

Table 2: **Processor System Reset Module I/O Signals *(Cont'd)***

Port	Signal Name	Interface	I/O	Description
P21	Interconnect_aresetn (0 to C_NUM_INTERCONNECT_ARESETN - 1)(1)	System	O	Interconnect_aresetn reset - for example, interconnects with active low reset inputs
P20	Peripheral_aresetn (0 to C_NUM_PERP_ARESETN - 1)(2)	System	O	Peripheral_aresetn is for all peripherals attached to interconnect that is synchronous with the Slowest_sync_clk. (active low)

Notes:

1. To help equalize loading on this signal, there can be from 1 to 8 copies generated with each copy being individually registered through a D-flip flop. In general each unique bus should receive a different copy of this signal.
2. To help equalize loading on this signal, there can be from 1 to 16 copies generated with each copy being individually registered through a D-flip flop. In general each peripheral should receive a different copy of this signal.

Port Dependencies

The width of some of the Processor System Reset Module signals depends on parameters set by generic inputs to the design. The dependencies between the Processor System Reset Module design parameters and I/O signals are shown in Table 3.

Table 3: **ParameterPort Dependencies**

Generic or Port	Name	Affects	Depends	Relationship Description
Design Parameters				
G5	C_NUM_BUS_RST	P19	-	The number of bus structure reset outputs is set by this generic
G6	C_NUM_PERP_RST	P20	-	The number of peripheral reset outputs is set by this generic
G7	C_NUM_INTERCONNECT_ARESETN	P21	-	The number of interconnect instances active low reset outputs is set by this generic
G8	C_NUM_PERP_ARESETN	P22	-	The number of peripherals connected to interconnects reset outputs is set by this generic
I/O Signals				
P19	Bus_Struct_Reset(0 to C_NUM_BUS_RST - 1)	-	G5	Width varies with the size of the C_NUM_BUS_RST.
P20	Peripheral_Reset(0 to C_NUM_PERP_RST - 1)	-	G6	Width varies with the size of the C_NUM_PERP_RST.
P21	Interconnect_aresetn (0 to C_NUM_INTERCONNECT_ARESETN - 1)	-	G7	Width varies with the size of the C_NUM_INTERCONNECT_ARESETN.
P20	Peripheral_aresetn (0 to C_NUM_PERP_ARESETN - 1)	-	G8	Width varies with the size of the C_NUM_PERP_ARESETN.

Design Implementation

Target Technology

The target technology is an FPGA listed in the Supported Device Family field in the LogiCORE IP Facts Table.

Device Utilization and Performance Benchmarks

N/A

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx ISE Design Suite Embedded Edition software under the terms of the Xilinx End User License. The core is generated using the Xilinx ISE Embedded Edition software (EDK).

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

Reference Documents

N/A

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
5/25/07	1.0	Initial Xilinx release.
12/06/07	1.1	Added Virtex® II P support
04/24/09	1.2	Replaced references to supported device families and tool name(s) with hyperlinks to PDF files; Updated trademark information.
06/01/09	1.3	Updated figure 2. Added note in the Table 1 regarding the usage of reset width.
04/19/10	1.4	Updated figure 1. Added two generics and two active low reset signals. Updated the version of the core.
7/23/10	1.5	Updated to 12.2; converted to new DS template; added Order Information section.

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