LogiCORE IP 10-Gigabit Ethernet MAC v11.2

DS813 October 19, 2011 **Product Specification**

Introduction

The LogiCORE™ IP 10-Gigabit Ethernet MAC core is a single-speed, full-duplex 10 Gb/s Ethernet Media Access Controller (MAC) solution enabling the design of high-speed Ethernet systems and subsystems.

Features

- Designed to 10-Gigabit Ethernet specification *IEEE 802.3-2008*
- Choice of external XGMII or internal FPGA interface to PHY layer (internal interface only on Spartan®-6 devices)
- AXI4-Stream protocol support on client transmit and receive interfaces.
- Cut-through operation with minimum buffering for maximum flexibility in client-side interfacing
- Supports Deficit Idle Count for maximum data throughput; maintains minimum IFG under all conditions and provides line rate performance
- Supports Deficit Idle Count with In-Band FCS and without In-Band FCS for all devices
- Configured and monitored through a AXI4-Lite Management Interface
- Comprehensive statistics gathering with statistic vector outputs
- Supports flow-control in both directions
- MDIO STA master interface to manage PHY layers
- Extremely customizable; trade resource usage against functionality
- Available under Xilinx End User License Agreement
- Delivered through the Xilinx® CORE Generator™ software
- Supports VLAN, jumbo frames, and WAN mode (WAN mode not supported on Spartan-6 devices.)
- Custom Preamble mode
- Supports feature of transmitting and receiving packets programmed up to MTU (Maximum Transmission Unit) programmed on both sides respectively.

LogiCORE IP Facts Table					
Core Specifics					
Supported Device Family(1)	Virtex-7, Kintex™-7, Virtex-6, Spartan-6(2)				
Supported User Interfaces	AXI4-Lite, AXI4-Stream				
	Resources(3)				**Frequency**
Devices	**Slices**	**LUTs**	**FFs**	**BUFGs**	**Max. Freq.**
Virtex-7 Kintex-7	See Table 18				156.25 MHz
Virtex-6	See Table 19				
Spartan-6	See Table 20				
Provided with Core					
Documentation	Product Specification User Guide				
Design Files	NGC netlist				
Example Design	VHDL and Verilog				
Test Bench	VHDL and Verilog				
Constraints File	UCF				
Simulation Model	VHDL/Verilog				
Tested Design Tools					
Design Entry Tools	ISE software v13.3				
Simulation(4)	Mentor Graphics ModelSim Cadence Incisive Enterprise Simulator (IES) Synopsys VCS and VCS MX				
Synthesis Tools	XST 13.3				
Support					
Provided by Xilinx, Inc.					

1. For a complete listing of supported devices, see the release notes for this core. Speed grades are -1 for Virtex-6 and -3 for Spartan-6 devices.
2. External XGMII interface and WAN mode not supported on Spartan-6 devices.
3. Numbers are approximate for default configuration in Virtex-6 devices. See Table 18, Table 19 and Table 20 for a complete description of device utilization by configuration and device family.
4. For the supported versions of the tools, see the ISE Design Suite 13: Release Notes Guide.

Applications

Figure 1 shows a typical Ethernet system architecture and the 10-Gigabit Ethernet MAC core within it. The MAC and all the blocks to the right are defined in Ethernet IEEE specifications.

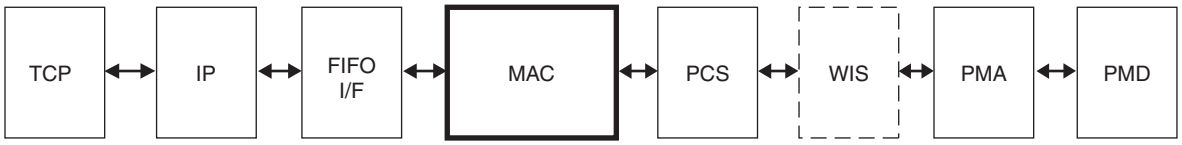

Figure 1: **Typical Ethernet System Architecture**

Figure 2 shows the 10-Gigabit Ethernet MAC core connected to a physical layer (PHY) device, for example, an optical module using the XGMII interface.

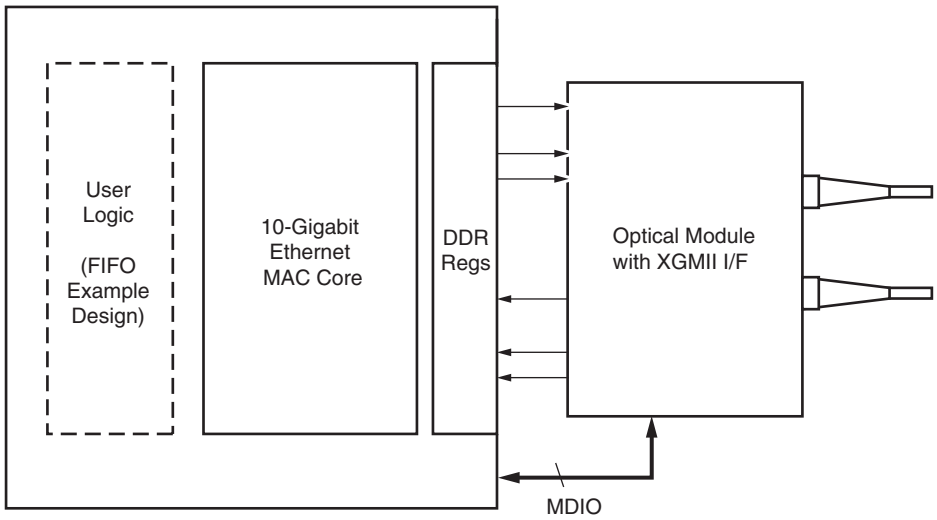

Figure 2: **10-Gigabit Ethernet MAC Core Connected to PHY with XGMII Interface**

The 10-Gigabit Ethernet MAC core is designed to be attached to the Xilinx IP XAUI core, the Xilinx IP RXAUI core, and the Xilinx IP 10G Ethernet PCS/PMA. Figure 3 illustrates the 10-Gigabit Ethernet MAC and XAUI cores in a system using an XPAK optical module.

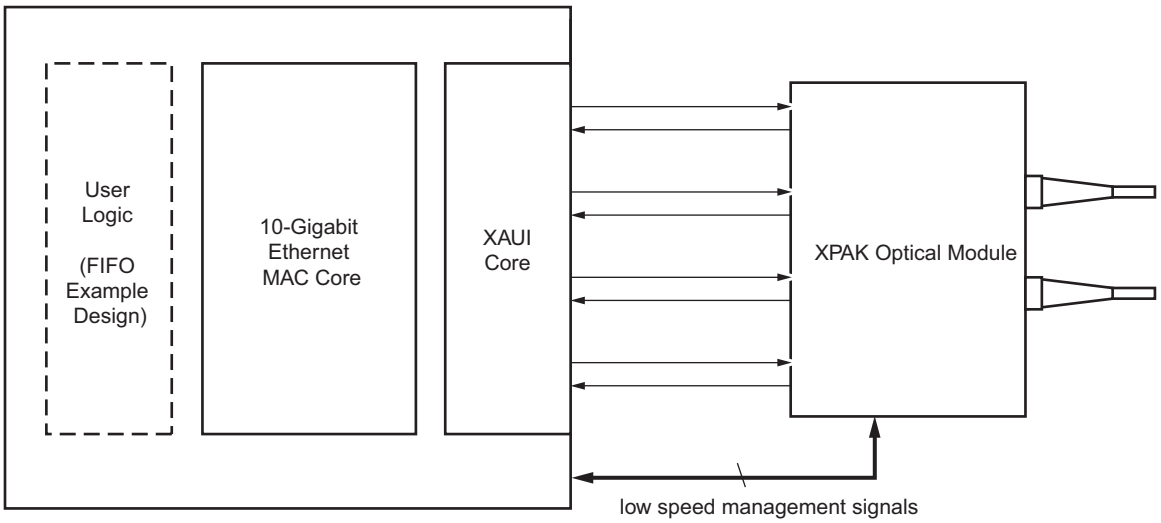

Figure 3: **10-Gigabit Ethernet MAC Core Used with Xilinx XAUI Core**

Functional Description

Figure 4 illustrates a block diagram of the 10-Gigabit Ethernet MAC core implementation. The major functional blocks of the core include the following:

- AXI4-Stream client-side interface: Designed for simple attachment of user logic
- Transmitter
- Receiver
- Flow Control block: Implements both Receive Flow Control and Transmit Flow Control
- Reconciliation Sublayer (RS): Processes XGMII Local Fault and Remote Fault messages and handles DDR conversion
- AXI4-Lite management interface and MDIO (optional)
- Statistics counters (optional)
- XGMII interface: Connection to the physical layer device or logic

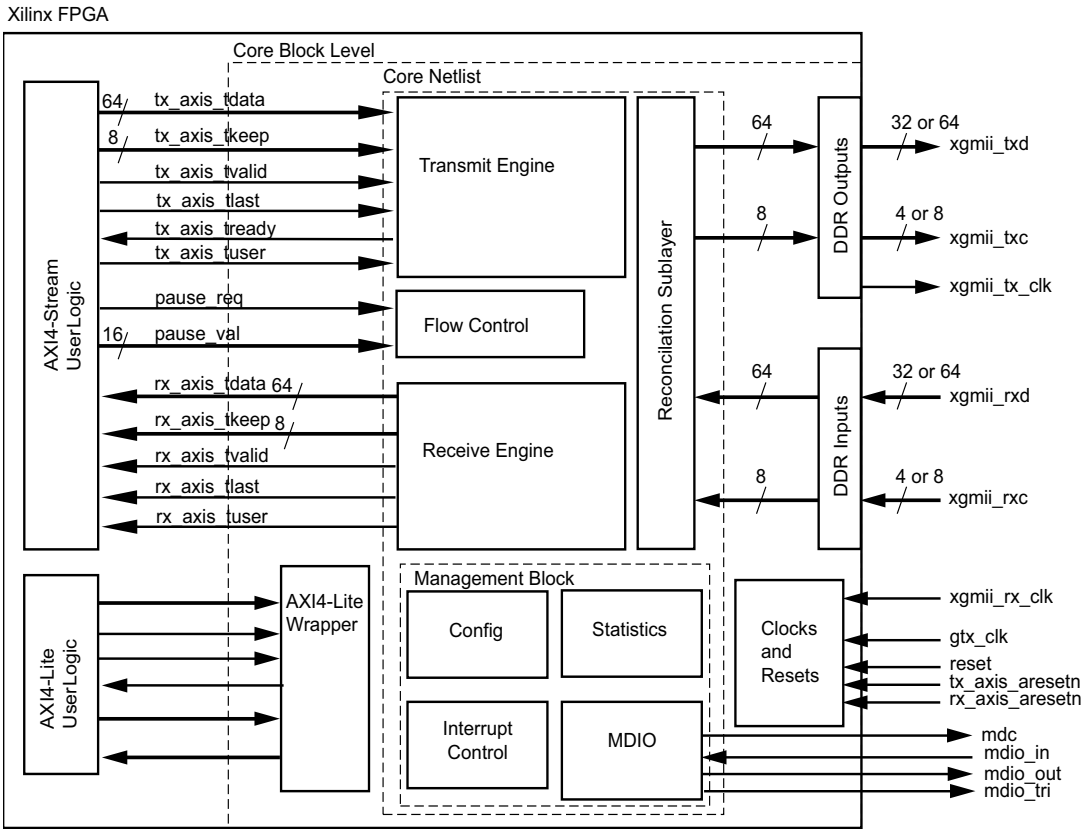

Figure 4: **Implementation of the 10-Gigabit Ethernet MAC Core**

Core Interfaces

AXI4-Stream Interface: Transmit

The client-side interface on the transmit side of XGMAC supports the AXI4-Stream specification. It has a 64-bit datapath with eight control bits to delineate bytes within the 64-bit port. Additionally, there are signals to handshake the transfer of data into the core. An example design which includes source code for a FIFO with an AXI4-Stream interface is provided with the core generated by CORE Generator software. Table 1 defines the signals.

Table 1: **Transmit AXI4-Stream Interface Port Description**

Name	Direction	Description
tx_axis_aresetn	IN	AXI4-Stream Active low reset for Transmit path XGMAC.
tx_axis_tdata[63:0]	IN	AXI4-Stream Data to XGMAC.
tx_axis_tkeep[7:0]	IN	AXI4-Stream Data Control to XGMAC.
tx_axis_tvalid	IN	AXI4-Stream Data Valid input to XGMAC.
tx_axis_tuser	IN	AXI4-Stream User signal used to indicate explicit underrun
tx_ifg_delay[7:0]	IN	Out-of-band signal used to configure Inter-frame gap adjustment between transmitted packets.
tx_axis_tlast	IN	AXI4-Stream signal to XGMAC indicating End of Ethernet Packet.
tx_axis_tready	OUT	AXI4-Stream acknowledge signal from XGMAC to indicate to start the Data transfer.

AXI4-Stream Interface: Receive

The client-side interface on receive side of XGMAC supports the AXI4-Stream specification. It has a 64-bit datapath with eight control bits to delineate bytes within the 64-bit port. Additionally, there are signals to indicate to the user logic the validity of the previous frame received. Table 2 defines the signals.

Table 2: **Receive AXI4-Stream Interface Port Description**

Name	Direction	Description
rx_axis_aresetn	IN	AXI4-Stream Active low reset for Receive path XGMAC.
rx_axis_tdata[63:0]	OUT	AXI4-Stream Data from XGMAC to upper layer.
rx_axis_tkeep[7:0]	OUT	AXI4-Stream Data Control from XGMAC to upper layer.
rx_axis_tvalid	OUT	AXI4-Stream Data Valid from XGMAC.
rx_axis_tuser	OUT	AXI4-Stream User Sideband Interface from XGMAC. '1' indicates that a good packet has been received. '0' indicates that a bad packet has been received.
rx_axis_tlast	OUT	AXI4-Stream signal from XGMAC indicating an end of packet.

Flow Control Interface

The flow control interface is used to initiate the transmission of flow control frames from the core. The ports associated with this interface are shown in Table 3.

Table 3: **Flow Control Interface Port Description**

Name	Direction	Description
pause_req	Input	Request that a flow control frame is emitted from the MAC core.
pause_val[15:0]	Input	Pause value field for flow control frame to be sent when pause_req asserted.

XGMII Interface or 64-bit SDR PHY Interface

The PHY interface can be a 32-bit DDR XGMII interface or a 64-bit SDR interface, depending on the customization of the core. This interface is used to connect to the physical layer, whether this is a separate device or implemented in the FPGA beside the MAC core. Table 4 and Table 5 show the ports associated with this interface.

Table 4: **32-bit XGMII PHY Interface Port Descriptions**

Name	Direction	Description
xgmii_tx_clk	Output	Forwarded clock to PHY device.
xgmii_txd[31:0]	Output	Transmit data to PHY; double data rate (DDR) source centred on xgmii_tx_clk.
xgmii_txc[3:0]	Output	Transmit control to PHY; DDR source-centred on xgmii_tx_clk.
xgmii_rx_clk	Input	Inbound clock from PHY device.
xgmii_rxd[31:0]	Input	Received data from PHY; DDR source-centred on xgmii_rx_clk.
xgmii_rxc[3:0]	Input	Received control from PHY; DDR source-centred on xgmii_rx_clk.

Table 5: **64-bit SDR PHY Interface Port Descriptions**

Name	Direction	Description
xgmii_txd[63:0]	Output	Transmit data to PHY. Synchronous to rising edge of tx_clk.
xgmii_txc[7:0]	Output	Transmit control to PHY. Synchronous to rising edge of tx_clk.
xgmii_rx_clk	Input	Inbound clock from PHY.
xgmii_rxd[63:0]	Input	Received data from PHY. Synchronous to rising edge of xgmii_rx_clk.
xgmii_rxc[7:0]	Input	Received control from PHY. Synchronous to rising edge of xgmii_rx_clk.

Management Interface

Configuration of the core, access to the statistics block, access to the MDIO port, and access to the interrupt block can be provided through the Management Interface. The AXI4-Lite Wrapper allows the MAC netlist to be connected to an AXI4-Lite Interface and drives the Ethernet MAC netlist through a processor independent IPIF.

Table 6 defines the ports associated with the Management Interface. The Management Interface can be omitted at core customization. In this case, the available configuration signals would be used. See Configuration and Status Signals.

Table 6: **AXI4-Lite Interface Port Description**

Name	Direction	Description
s_axi_aclk	IN	AXI4-Lite clock. Range between 10 MHz and 156.25 MHz
s_axi_aresetn	IN	Asynchronous active low reset
s_axi_awaddr[31:0]	IN	Write address Bus
s_axi_awvalid	IN	Write address valid
s_axi_awready	OUT	Write address acknowledge
s_axi_wdata[31:0]	IN	Write data bus
s_axi_wvalid	IN	Write data valid
s_axi_wready	OUT	Write data acknowledge
s_axi_bresp[1:0]	OUT	Write transaction response
s_axi_bvalid	OUT	Write response valid
s_axi_bready	IN	Write response acknowledge
s_axi_araddr[31:0]	IN	Read address Bus
s_axi_arvalid	IN	Read address valid
s_axi_arready	OUT	Read address acknowledge
s_axi_rdata[31:0]	OUT	Read data output
s_axi_rresp[1:0]	OUT	Read data response
s_axi_rvalid	OUT	Read data/response valid
s_axi_rready	IN	Read data acknowledge

Statistic Counters

During operation, the MAC core collects statistics on the success and failure of various operations for processing by network management entities elsewhere in the system. These statistics are accessed through the Management Interface. A list of statistics is shown in Table 7.

Table 7: **Statistics Counters**

1	Received bytes
2	Transmitted bytes
3	Undersize frames received
4	Fragment frames received
5	64 byte frames received OK
6	65-127 byte frames received OK
7	128-255 byte frames received OK
8	256-511 byte frames received OK
9	512-1023 byte frames received OK
10	1024-MaxFrameSize byte frames received OK
11	Oversize frames received OK
12	64 byte frames transmitted OK
13	65-127 byte frames transmitted OK
14	128-255 byte frames transmitted OK
15	256-511 byte frames transmitted OK
16	512-1023 byte frames transmitted OK
17	1024-MaxFrameSize byte frames transmitted OK
18	Oversize frames transmitted OK
19	Frames received OK
20	Frame Check Sequence errors
21	Broadcast frames received OK
22	Multicast frames received OK
23	Control frames received OK
24	Length/Type out of range
25	VLAN tagged frames received OK
26	PAUSE frames received OK
27	Control frames received with unsupported opcode
28	Frames transmitted OK
29	Broadcast frames transmitted OK
30	Multicast frames transmitted OK
31	Underrun errors
32	Control frames transmitted OK
33	VLAN tagged frames transmitted OK
34	PAUSE frames transmitted OK

The statistic counters are an optional block of the 10-Gigabit Ethernet MAC core.

Configuration Registers

After the core is powered up and reset, the user application can reconfigure some of the core parameters from their default values, such as flow control operation and WAN mode. Configuration registers can be written and read at any time; however, changes can only take effect during the next interframe gap period. Exceptions to this include the soft reset registers which take effect immediately.

Configuration of the 10-Gigabit Ethernet MAC core is performed through a bank of registers accessed through the Management Interface. The configuration registers in this bank are shown Table 8. Their addresses and contents are described in the *LogiCORE IP 10-Gigabit Ethernet MAC v 11.1 User Guide* (UG773).

Table 8: **Configuration Registers**

1	Receiver Configuration Word 0
2	Receiver Configuration Word 1
3	Transmitter Configuration
4	Flow Control Configuration
5	Reconciliation Sublayer Configuration
6	Receiver MTU Configuration word
7	Transmitter MTU Configuration word
8	Version Register
9	Capability Register

MDIO STA Master

The MDIO STA master interface implemented in the 10-Gigabit Ethernet MAC core is an STA entity (as defined by *IEEE Std.802.3-2008* that can initiate transactions to one or more attached physical layer MDIO Managed Devices (MMDs). The MDIO registers are shown in Table 9. Their addresses and contents are described in the *LogiCORE IP 10-Gigabit Ethernet MAC v 11.1 User Guide* (UG773).

Table 9: **MDIO Registers**

1	MDIO Configuration Word 0
2	MDIO Configuration Word 1
3	MDIO Transmit Data Word
4	MDIO Receive Data Word

If the Management Interface is omitted from the core, the MDIO interface is also omitted.

Interrupt Block

An Interrupt function is provided in the 10-Gigabit Ethernet MAC core to assert an interrupt when a pending MDIO transaction is completed. Interrupt registers are shown in Table 10. Their addresses and contents are described in the *LogiCORE IP 10-Gigabit Ethernet MAC v 11.1 User Guide* (UG773).

Table 10: **Interrupt Registers**

1	Interrupt Status Register
2	Interrupt Pending Register
3	Interrupt Enable Register
4	Interrupt Acknowledge Register

Configuration and Status Signals

If the Management Interface is omitted at core customization time, a configuration vector for each transmitter and receiver interface and a status vector is exposed by the core. This allows you to configure the core by statically or dynamically driving the constituent bits of these ports. Table 11 and Table 12 describe the configuration signals for transmitter and receiver and Table 13 describes the status signals. For more information about the use of the configuration vector, see the *10-Gigabit Ethernet MAC User Guide*.

Table 11: **Transmitter Configuration Signals**

Name	Direction	Description
configuration_vector_tx[79:0]	Input	Bit 0: Transmitter reset Bit 1: Transmitter Enable Bit 2: Transmitter VLAN Enable Bit 3: Transmitter In Band FCS Enable Bit 4: Transmitter Jumbo Frame Enable Bit 5: Transmit Flow Control enable Bit 6: Reserved Bit 7: Tx preserve preamble enable Bit 8: Transmitter IFG Adjust enable Bit 9: Transmitter LAN/WAN Bit 10: Transmit Deficit Idle Count Bit 11 to 13: Reserved Bit 14: Transmitter Max Frame Enable Bit 15: Reserved Bit 31 to 16: Transmitter Max Frame Length[15:0] Bit 79 to 32: Transmitter Pause Frame Source Address

Table 12: **Receiver Configuration Signals**

Name	Direction	Description
configuration_vector_rx[79:0]	Input	Bit 0: Receiver reset Bit 1: Receiver Enable Bit 2: Receiver VLAN Enable Bit 3: Receiver In Band FCS Enable Bit 4: Receiver Jumbo Frame Enable Bit 5: Receive Flow Control enable Bit 6: Reserved Bit 7: Rx preserve preamble enable Bit 8: Receiver Length/Type Check Disable Bit 9: Control Frame Length Check Disable Bit 10: RS fault inhibit Bit 11 to 13: Reserved Bit 14: Receiver Max Frame Enable Bit 15: Reserved Bit 31 to 16: Receiver Max Frame Length[15:0] Bit 79 to 32: Receiver Pause Frame Source Address

Table 13: **Status Signals**

Name	Direction	Description
status_vector	Output	Bit 0: Local fault received Bit 1: Remote fault received

Statistic Vectors

In addition to the statistic counters described in Management Interface, there are two statistics vector outputs on the core netlist that are used to signal the core state. These vectors are actually used as the inputs of the counter logic internal to the core. So if you omit the statistic counters at the CORE Generator software customization stage, a relevant subset can be implemented in user logic. Table 14 identifies the signals. The contents of the vectors are defined in Table 15 and Table 16.

Table 14: **Statistic Vector Signals**

Name	Direction	Description
tx_statistics_vector[25:0]	Output	Aggregated statistics flags for transmitted frame
tx_statistics_valid	Output	Valid strobe for tx_statistics_vector
rx_statistics_vector[29:0]	Output	Aggregated statistics flags for received frames
rx_statistics_valid	Output	Valid strobe for rx_statistics_vector

Table 15: **Transmit Statistics Vector Contents**

tx_statistics_vector bits	Name
25	PAUSE_FRAME_TRANSMITTED
24 to 21	BYTES_VALID
20	VLAN_FRAME
19 to 5	FRAME_LENGTH_COUNT
4	CONTROL_FRAME
3	UNDERRUN_FRAME
2	MULTICAST_FRAME
1	BROADCAST_FRAME
0	SUCCESSFUL_FRAME

Table 16: **Receive Statistics Vector Contents**

rx_statistics_vector bits	Name
29	LEN_TYPE_RANGE
28	BAD_OPCODE
27	FLOW_CONTROL_FRAME
26 to 23	BYTES_VALID
22	VLAN_FRAME
21	OUT_OF_BOUNDS
20	CONTROL_FRAME
19 to 5	FRAME_LENGTH_COUNT
4	MULTICAST_FRAME
3	BROADCAST_FRAME
2	FCS_ERROR
1	BAD_FRAME
0	GOOD_FRAME

Clocks and Resets

Table 17 describes the clock and reset ports present on the supplied example design. In the source code of the example design, other system clocks are derived from the `gtx_clk` and `xgmii_rx_clk` signals for use in the core logic. This clock arrangement can be customized in the user application as required.

Table 17: **Clock and Reset Ports**

Name	Direction	Description
gtx_clk	Input	Global transmit clock; all other transmit clocks are derived from this clock
xgmii_rx_clk	Input	XGMII receive clock; all receive clocks are derived from this clock
reset	Input	Asynchronous reset
rx_axis_aresetn	Input	AXI4-Stream Active low reset for Receive path XGMAC.
tx_axis_aresetn	Input	AXI4-Stream Active low reset for Transmit path XGMAC.

Verification

The 10-Gigabit Ethernet MAC core has been verified in simulation.

Simulation

A highly parameterizable transaction-based simulation test suite has been used to verify the core. Tests included:

- Configuration register access through Management Interface
- Local Fault and Remote Fault handling
- Frame transmission
- Frame reception
- CRC validity
- Handling of CRC errors
- Statistic counter access through Management Interface and validity of counts
- Statistic vector validity
- Initiating MDIO transactions through Management Interface
- Use of custom preamble field
- Variable Frame Length and MTU

Hardware Verification

The core has been used in a number of hardware test platforms at Xilinx, including the following:

- The core has been used in a test platform design with the Xilinx 10-Gigabit Ethernet XAUI LogiCORE IP. This design comprises the MAC, XAUI, a *ping* loopback FIFO and a test pattern generator all under embedded PowerPC® processor control.
- This design has been used for conformance and interoperability testing at the University of New Hampshire Interoperability Lab.

Device Utilization

Virtex-7 and Kintex-7 FPGAs

Table 18: **Device Utilization for the 10-Gigabit Ethernet MAC Core (Virtex-7 and Kintex-7 FPGAs)**

Parameter Values				Resource Usage			
Device Family	Physical Interface	Management Interface	Statistic Counters	Slices	LUTs	FFs	BUFGs
virtex7	XGMII	TRUE	TRUE	2193	3868	4251	2
			FALSE	1528	3003	3120	2
		FALSE	FALSE	1496	2736	2921	2
	Internal	TRUE	TRUE	2280	3881	4396	2
			FALSE	1563	2977	3120	2
		FALSE	FALSE	1510	2752	3066	2
kintex7	XGMII	TRUE	TRUE	2022	4082	4252	2
			FALSE	1619	3097	3334	2
		FALSE	FALSE	1352	2879	2921	2
	Internal	TRUE	TRUE	2006	3918	4037	2
			FALSE	1595	3111	3262	2
		FALSE	FALSE	1383	2895	2850	2

Virtex-6 FPGAs

Table 19 provides approximate utilization figures for various core options when a single instance of the core is instantiated in a Virtex®-6 device.

Utilization figures are obtained by implementing the block-level wrapper for the core. This wrapper is part of the example design and connects the core to the selected physical interface.

Table 19: **Device Utilization for the 10-Gigabit Ethernet MAC Core (Virtex-6 FPGAs)**

Parameter Values				Resource Usage			
Device Family	Physical Interface	Management Interface	Statistic Counters	Slices	LUTs	FFs	BUFGs
virtex6	XGMII	TRUE	TRUE	2005	3912	4037	2
			FALSE	1628	3030	3190	2
		FALSE	FALSE	1422	2777	2780	2
	Internal	TRUE	TRUE	1993	4047	4107	2
			FALSE	1525	3152	3191	2
		FALSE	FALSE	1394	2816	2778	2

Spartan-6 FPGAs

Table 20 provides approximate utilization figures for various core options when a single instance of the core is instantiated in a Spartan-6 device.

Utilization figures are obtained by implementing the block-level wrapper for the core. This wrapper is part of the example design and connects the core to the selected physical interface.

Table 20: **Device Utilization for the 10-Gigabit Ethernet MAC Core (Spartan-6 FPGAs)**

Parameter Values				Resource Usage			
Device Family	**Physical Interface**	**Management Interface**	**Statistic Counters**	**Slices**	**LUTs**	**FFs**	**BUFGs**
spartan6	Internal	TRUE	TRUE	2032	3871	4183	1
			FALSE	1563	2955	3263	1
		FALSE	FALSE	1346	2703	2777	1

References

[1] *IEEE Standard 802.3-2008*, "Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications."

Support

Visit www.xilinx.com/support/ for technical support. Xilinx provides technical support for this LogiCORE IP product when used as described in product documentation.

Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not listed in the documentation or if customized beyond that allowed in the product documentation, or if any changes are made in sections of the design marked as *DO NOT MODIFY*.

Ordering Information

This Xilinx LogiCORE IP module is provided under the Xilinx End User License Agreement. Two free evaluation licenses are provided: The Simulation Only license is provided with the CORE Generator software, and the Full System Hardware Evaluation license, which lets you test your designs in hardware for a limited period of time, can be downloaded from the 10GEMAC product page.

For full access to all core functionality, both in simulation and in hardware, you must purchase the core. The Xilinx CORE Generator system is bundled with the Xilinx ISE® Design Suite software at no additional charge.

Contact your local Xilinx sales representative for pricing and availability of Xilinx LogiCORE IP modules and software. Information about additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

List of Acronyms

Acronym	Description
AXI	Advanced eXtensible Interface
CRC	Cyclic Redundancy Check
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DCM	Digital Clock Manager
DDR	Double Data Rate
EDIF	Electronic Design Interchange Format
FCS	Frame Check Sequence
FF	Flip-Flop
FIFO	First In First Out
FPGA	Field Programmable Gate Array
Gb/s	Gigabits per second
IES	Incisive Enterprise Simulator
IFG	Interframe GAP
IP	Intellectual Property
ISE	Integrated Software Environment
LUT	Lookup Table
MAC	Media Access Controller
MDIO	Management Data Input/Output
MHz	Mega Hertz
MMD	MDIO Managed Devices
MTU	Maximum Transmission Unit
NDA	Non-Disclosure Agreement
NGC	Native Generic Circuit
PHY	physical-side interface
RAM	Random Access Memory
RS	Reconciliation Sublayer
SDR	Single Data Rate
STA	Station Management Entity
UCF	User Constraints File
VCS	Verilog Compiled Simulator (Synopsys)
VHDL	VHSIC Hardware Description Language (VHSIC an acronym for Very High-Speed Integrated Circuits)
VLAN	Virtual LAN (Local Area Network)
WAN	Wide Area Network
XAUI	eXtended Attachment Unit Interface
XGMII	10-Gigabit Media Independent Interface
XPAK	Expansion Pack
XST	Xilinx Synthesis Technology

Revision History

Date	Version	Revision
03/01/10	1.1	Initial Release
10/19/11	1.2	Update for 13.3. Updated Device Utilization, page 12.

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