LogiCORE IP Utility Differential Signaling Buffer (v1.01a)

DS647 January 18, 2012 **Product Specification**

Introduction

The LogiCORE™ IP Utility Differential Signaling Buffer core generates corresponding buffer to bring off-chip differential signals into internal circuit or out from internal circuits. The core is intended as interconnect logic between off-chip differential signals and internal circuit.

Features

- Configurable size of the signal width
- Configurable differential signaling buffer type

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Zynq -7000, Artix™-7, Virtex -7, Kintex™-7, Virtex-6, Virtex-5, Spartan -6, Virtex-4, Spartan-3
Supported User Interfaces	N/A
Resources	
See Table 4	
Provided with Core	
Documentation	Product Specification
Design Files	VHDL
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	UCF
Simulation Model	VHDL
Supported S/W Driver	N/A
Tested Design Tools	
Design Entry Tools	ISE 13.4
Simulation(2)	ModelSim
Synthesis Tools(2)	XST
Support	
Provided by Xilinx @ www.xilinx.com/support	

1. For a complete listing of supported devices, see the release notes for this core.
2. For a listing of the supported tool versions, see the ISE Design Suite 13: Release Note Guide.

Functional Description

The Utility Differential Signaling Buffer core generates corresponding buffers to bring off-chip differential signals into or out from internal circuits. Figure 1 illustrates the Utility Differential Signaling Buffer in a system.

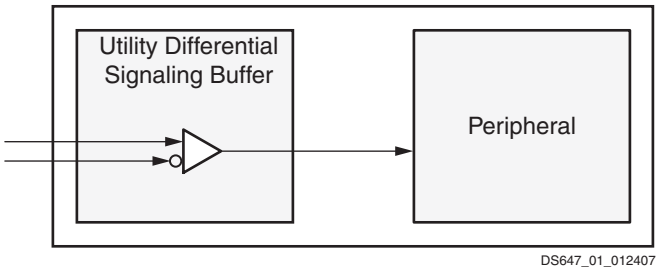

Figure 1: **Utility Differential Signaling Buffer in a System**

I/O Signals

The Utility Differential Signaling Buffer I/O signals are listed and described inTable 1.

Table 1: **I/O Signals**

Signal	Interface	I/O	Default Value
IBUF_DS_P	None	I	Positive (master) port of the differential input signal: used only for IBUFDS or IBUFGDS.
IBUF_DS_N	None	I	Negative (slave) port of the differential input signal: used only for IBUFDS or IBUFGDS.
IBUF_OUT	None	O	Single ended output signal: used only for IBUFDS or IBUFGDS.
OBUF_IN	None	I	Single ended input signal: used only for OBUFDS.
OBUF_DS_P	None	O	Positive (master) port of the differential output signal, used only for OBUFDS.
OBUF_DS_N	None	O	Negative (slave) port of the differential output signal: used only for OBUFDS.
IOBUF_DS_P	None	I/O	Positive (master) port of the differential input signal: used only for IOBUFDS.
IOBUF_DS_N	None	I/O	Negative (slave) port of the differential input signal: used only for IOBUFDS.
IOBUF_IO_T	None	I	3-state enable input: used only for IOBUFDS.
IOBUF_IO_I	None	I	3-state buffer input: used only for IOBUFDS.
IOBUF_IO_O	None	O	3-state buffer output: used only for IOBUFDS.

Design Parameters

The Utility Differential Signaling Buffer parameters are listed and described in Table 2.

Table 2: **Utility Differential Signaling Buffer Parameters**

Parameter	Description	Type
C_SIZE	The vector size of differential signal (valid value is 1 to 128).	integer
C_BUF_TYPE	The differential signaling buffer to be instantiated (valid values are IBUFDS, IBUFGDS, OBUFDS, IOBUFDS, IBUFDSGTXE, and IBUFDSGTE).	string

Parameter - Port Dependencies

The parameter and port dependencies are listed and described in Table 3.

Table 3: **Utility Differential Signaling Buffer Parameters - Port Dependencies**

Name	Affects	Depends	Relational Description
Design Parameters			
C_SIZE	All signals	0 to C_SIZE-1	Scale width of all port signals
Port Signals			
IBUF_*	All signals	C_BUF_TYPE	Valid for C_BUF_TYPE=IBUFDS or IBUFGDS, or IBUFDSGTXE, or IBUFDSGTE and not used for other cases
OBUF_*		C_BUF_TYPE	Valid for C_BUF_TYPE=OBUFDS, not used for other cases
IOBUF_*		C_BUF_TYPE	Valid for C_BUF_TYPE=IOBUFDS, not used for other cases

Figure 2 shows three instantiation cases for the core.

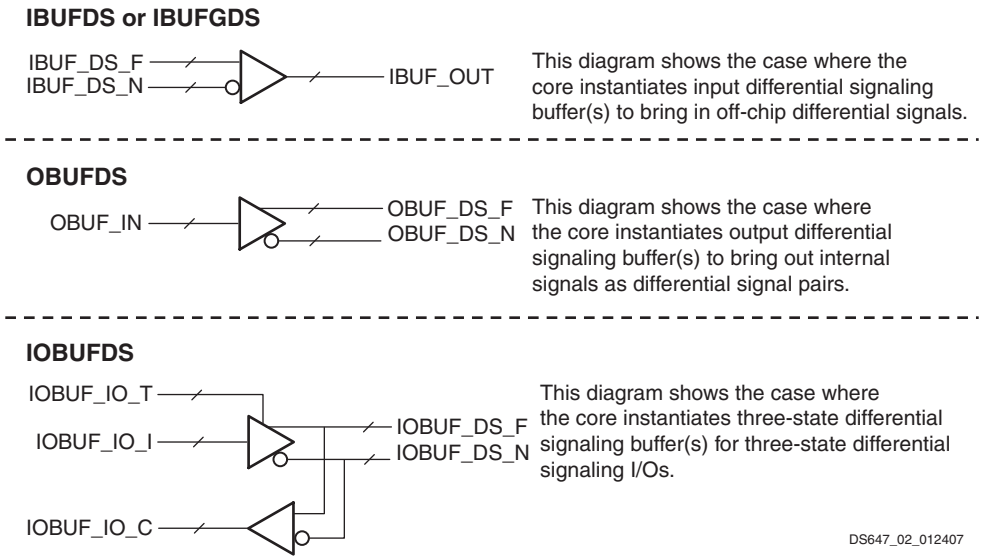

Figure 2: **Utility Vector Logic Block Diagram**

Design Implementation

Design Tools

The Utility Differential Signaling Buffer design is handwritten. Xilinx® XST is the synthesis tool used for synthesizing the core.

Target Technology

The target technology is the 7 Series, Zynq™-7000, Virtex® and Spartan® family FPGAs.

Device Utilization and Performance Benchmarks

Table 4: **Utility Differential Signaling Buffer Resource Utilization**

Parameter		Resources					
		IBUFDS	IBUFGDS	OBUFDS	IOBUFDS	IBUFDSGTXE	IBUFDSGTE
C_SIZE=n	C_BUF_TYPE=IBUFDS	n	0	0	0	0	0
	C_BUF_TYPE=IBUFGDS	0	n	0	0	0	0
	C_BUF_TYPE=OBUFDS	0	0	n	0	0	0
	C_BUF_TYPE=IOBUFDS	0	0	0	n	0	0
	C_BUF_TYPE=IBUFDSGTXE	0	0	0	0	n	0
	C_BUF_TYPE=IBUFDSGTE	0	0	0	0	0	n

Support

Xilinx provides technical support for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx ISE® Design Suite Embedded Edition software under the terms of the Xilinx End User License. The core is generated using the Xilinx Integrated Software Environment (ISE®) Embedded Edition software (EDK). For more information, visit the Utility Differential Signaling Buffer product page.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE IP modules and software. Information about additional Xilinx LogiCORE IP modules is available on the Xilinx IP Center.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
9/25/07	1.0	Initial Xilinx release.
7/25/08	1.2	Added QPro Virtex-4 Hi-Rel and QPro Virtex-4 Rad Tolerant FPGA support.
9/16/09	1.3	Created v1.01a for EDK_L 11.3 release, incorporated CR530738.
01/18/12	1.4	GTXE support added. Xilinx release 13.4.

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