Utility Vector Logic for Vivado (v2.0)

DS913 (v2.0) November 2, 2015 **Product Specification**

Summary

The utility vector logic core takes two vector operands and bit-wise applies a logic function to generate a single vector result. This core is intended as glue logic between peripherals.

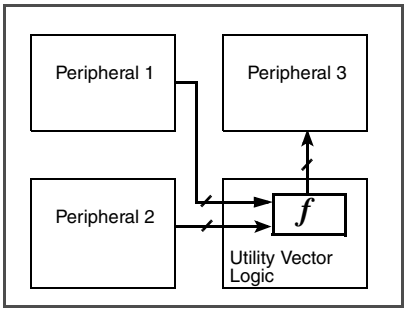

Figure 1: **Utility Vector Logic in a System**

Features

The vector logic has the following features:

- Configurable size of the vectors
- Configurable logical operation on vectors

LogiCORE™ IP Facts		
Core Specifics		
Supported Device Families	Kintex®-7, Zynq®-7000 AP SoC, Zynq UltraScale+™	
Version of Core	util_vector_logic	v2.0
Resources Used		
	Min	Max
Slices	1	16[1]
LUTs	1	32(1)
FFs	0	0
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	

LogiCORE™ IP Facts	
Design Tool Requirements	
Xilinx Implementation Tools	Xilinx Design Tools: See the *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing* (UG973)
Verification	
Simulation	
Synthesis	
Support	
Support provided by Xilinx®, Inc.	

1. For C_SIZE=32. The count increases with C_SIZE

Utility Vector Logic Parameters

Table 1: **Utility Vector Logic Parameters**

Parameter	Description	Type
C_OPERATION	The vector operation to perform. The supported operations are: and, or, xor, and not.	String
C_SIZE	The size of the vectors. Notice that the width of Op1, Op2 and Res must be equal. The minimum value of this parameter is 1.	Integer

Allowable Parameter Combinations

There are no restrictions on allowed parameter combinations for this core.

Utility Vector Logic I/O Signals

Table 2: **Summary of vector logic I/O**

Signal	Interface	I/O	Description
Op1	None	I	Operand 1 vector [0 : C_SIZE-1]
Op2	None	I	Operand 2 vector [0 : C_SIZE-1]. Unused when C_OPERATION = not
Res	None	O	Result vector [0 : C_SIZE-1]

Parameter-Port Dependencies

Table 3: **Port and Parameter Dependencies**

Name	Affects	Depends	Relationship Description
Design Parameters			
C_SIZE	Op1	0 to C_SIZE-1	Scale width of input bus
C_SIZE	Op2	0 to C_SIZE-1	Scale width of input bus
C_SIZE	Res	0 to C_SIZE-1	Scale width of output bus
Port Signals			
Op1		C_SIZE	Scale width of input bus
Op2		C_SIZE	Scale width of input bus
Res		C_SIZE	Scale width of output bus

Utility Vector Logic Register Descriptions

There are no registers in this core.

Utility Vector Logic Interrupt Descriptions

There are no interrupts associated with this core.

Utility Vector Logic Block Diagram

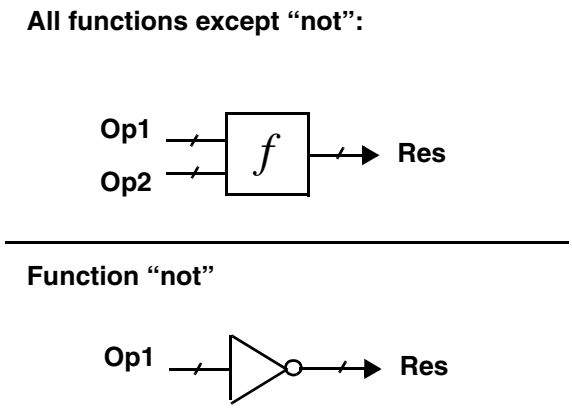

Figure 3: **Utility Vector Logic Block Diagram**

Design Implementation

Design Tools

The utility vector logic IP is used in a block design created with the Vivado® Design Suite IP integrator.

Vivado synthesis is the tool used for synthesizing the utility vector logic.

Target Technology

The targeted devices are Vivado Design Suite supported device families.

Device Utilization and Performance Benchmarks

Table 4: **Utility Vector Logic Resource Utilization**

Parameter value		Device Resources		
C_OPERATION	C_SIZE	Slices	Slice Flip-Flops	Slice LUTs
and	8	4	0	8
xor	12	6	0	12

There are no performance benchmarks available.

Specification Exceptions

Not applicable.

Reference Documents

None.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Revision History

Date	Version	Revision
11/02/15	2.0	Initial version to document IP core (v2.0)

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